What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ZNEO
Core Size	16-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	60
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z16f3211fi20eg

Revision History

Each instance in this document's revision history reflects a change from its previous edition. For more details, refer to the corresponding page(s) or appropriate links furnished in the table below.

Date	Revision Level	Section	Description	Page No.
Nov 2013	12	Signal Descriptions	Corrected active status of RD, WR and $\overline{CS}$ signals.	12
Jul 2013	11	Analog Functions	Updated the Analog Functions Block Diagram.	242
Aug 2011	10	Multi-Channel PWM Timer	Per CR#13095, corrected PWMEN description in PWM Control 0 Register (PWMCTL0) table; corrected description in PWM Deadband Register (PWMDB) table and added footnote; added same footnote to PWM Minimum Pulse Width Filter (PWMMPF), PWM Fault Mask Register (PWMFM), and PWM Fault Control Register (PWMFCTL) tables.	125, 127–129, 131
Jun 2011	09	Electrical Characteristics	Corrected V_{COFF} input offset value in Comparator Electrical Characteristics table	347
Aug 2010	08	N/A	Removed ISO information.	ii
		All	Updated logos.	All
		Table 191	Changed the Minimum, Typical and Maximum values for V_{REF} (Externally supplied Voltage Reference only).	346
Jan 2009	07	Timer 0–2 Control 0 Register	Table 62: added "Only Counter Mode should be used with this feature" to Bit 4 description.	109
		Analog Functions	ADC Overview, updated fast conversion time to 2.5 µs.	243
		Electrical Characteristics	Updated Table 185.	337
		Internal Precision Oscillator	Removed reference to 32 kHz.	336

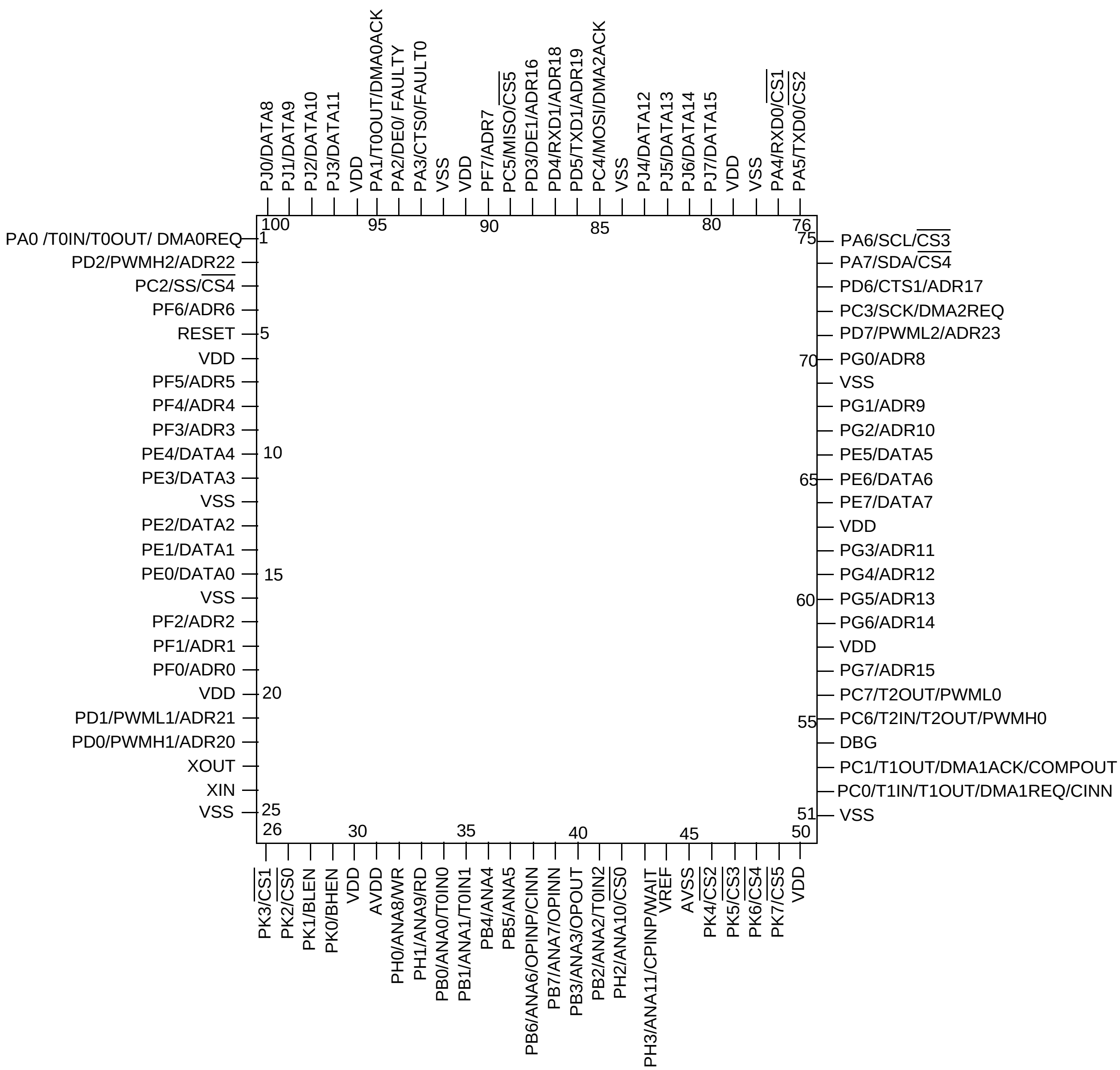

Figure 5. ZNEO Z16F Series, 100-Pin Low-Profile Quad Flat Package (LQFP)

Table 6. Register File Address Map (Continued)

Address (Hex)	**Register Description**	**Mnemonic**	Reset (Hex)	**Page No**
FF_E07B	Chip Select 4 Control Low	EXTCS4L		46
FF_E07C	Chip Select 5 Control High	EXTCS5H		43
FF_E07D	Chip Select 5 Control Low	EXTCS5L		46
FF_E07E-FF_E07F	Reserved	—	—	—
On Chip Debugger = FF_E080				
FF_E080	Debug Receive Data	DBGRXD	XX	315
FF_E081	Debug Transmit Data	DBGTXD	XX	315
FF_E082-FF_E083	Debug Baud Rate	DBGBR	XXXX	316
FF_E084	Debug Line Control	DBGLCR	XX	316
FF_E085	Debug Status	DBGSTAT	XX	318
FF_E086	Debug Control	DBGCTL	XX	319
Hardware Breakpoints = FF_E090				
FF_E090-FF_E093	Hardware Breakpoint 0	HWBP0	00000000	324
FF_E094-FF_E097	Hardware Breakpoint 1	HWBP1	00000000	324
FF_E098-FF_E09B	Hardware Breakpoint 2	HWBP2	00000000	324
FF_E09C-FF_E09F	Hardware Breakpoint 3	HWBP3	00000000	324
Oscillator Control Base Address = FF_E0A0				
FF_E0A0	Oscillator Control	OSCCTL	A0	334
FF_E0A1	Oscillator Divide	OSCDIV	00	335
GPIO Base Address = FF_E100				
GPIO Port A Base Address = FF_E100				
FF_E100	Port A Input Data	PAIN	XX	71
FF_E101	Port A Output Data	PAOUT	00	72
FF_E102	Port A Data Direction	PADD	00	73
FF_E103	Port A High Drive Enable	PAHDE	00	74
FF_E104	Port A Alternate Function High	PAAFH	00	75
FF_E105	Port A Alternate Function Low	PAAFL	00	75
FF_E106	Port A Output Control	PAOC	00	76
FF_E107	Port A Pull-Up Enable	PAPUE	00	76
FF_E108	Port A Stop Mode Recovery Enable	PASMRE	00	77
FF_E109-FF_E10B	Port A Reserved	—	—	—

XX = Undefined.

ISA-Compatible Mode

Configuring the external interface for ISA Mode adjusts the Read timing to follow the ISA Mode commonly employed in PC and related applications. In ISA Mode, assertion of the Read signal ($\overline{RD}$) is delayed one-half system clock. Also, an extra wait state is added during read operations.

External Interface Control Register Definitions

The following section describes the various control registers.

External Interface Control Register

The External Interface Control Register, shown in Table 9, enables the interface and sets the internal memory size.

Table 9. External Interface Control Register (EXTCT)

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	BUSSEL		MEMSIZE		RESERVED			
RESET	00		00		0000			
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FF_E070h							

Bit	Description
[7:6] BUSSEL	**Bus Select External Interface Enable** 00 = No External Bus. 01 = 8-bit External Bus Interface is enabled (Port E). 1X = 16-bit External Bus Interface is enabled (Port J and Port E).
[5:4] MEMSIZE	**Select Internal Memory Size** 00 = 128 KB of internal memory. 01 = 64 KB of internal memory. 10 = 32 KB of internal memory. 11 = No Internal Memory.
[3:0]	**Reserved** These bits are reserved and must be programmed to 0000.

System Reset

During a System Reset, the ZNEO Z16F Series device is held in Reset for 66 cycles of the IPO. At the beginning of Reset, all GPIO pins are configured as inputs. All GPIO programmable pull-ups are disabled.

At the start of a System Reset, the motor control PWM outputs are forced to high-impedance momentarily. When the option bits that control the off-state have been properly evaluated, the PWM outputs are forced to the programmed off-state.

During Reset, the ZNEO CPU and on-chip peripherals are nonactive; however, the IPO and WDT oscillator continue to run. During the first 50 clock cycles, the internal option bit registers are initialized, after which the system clock for the core and peripherals begins operating. The ZNEO CPU and on-chip peripherals remain nonactive through the next 16 cycles of the system clock, after which the internal reset signal is deasserted.

On Reset, control registers within the register file that have a defined reset value are loaded with their reset values. Other control registers (including the Flags) and general-purpose RAM are undefined following Reset. The ZNEO CPU fetches the Reset vector at program memory address `0004h` and loads that value into the program counter. Program execution begins at the Reset vector address.

Table 19 lists the System Reset sources as a function of the operating mode. The following text provides more detailed information about the individual Reset sources. Note that a POR/VBO event always has priority over all other possible reset sources to ensure that a full System Reset occurs.

Table 19. System Reset Sources and Resulting Reset Action

Operating Mode	System Reset Source	Action
NORMAL or HALT modes	POR/VBO	System Reset
	WDT time-out when configured for Reset	System Reset
	$\overline{\text{RESET}}$ pin assertion	System Reset
	Write RSTSCR[0] to 1	System Reset
	Fault detect logic reset	System Reset
Stop Mode	POR/VBO	System Reset
	$\overline{\text{RESET}}$ pin assertion	System Reset
	Fault detect logic reset	System Reset

Power-On Reset

Each device in the ZNEO Z16F Series contains an internal POR circuit. The POR circuit monitors the supply voltage and holds the device in the Reset state until the supply voltage reaches a safe operating level. After the supply voltage exceeds the POR voltage threshold

Bit	Description (Continued)
[3:1] PWMD	**PWM Delay Value** This field is a programmable delay to control the number of additional system clock cycles following a PWM or Reload compare before the timer output or the timer output complement is switched to the active state. This field ensures a time gap between deassertion of one PWM output to the assertion of its complement. No delay. 2 cycles delay. 4 cycles delay. 8 cycles delay. 16 cycles delay. 32 cycles delay. 64 cycles delay. 128 cycles delay.
[0] INCAP	**Input Capture Event** 0 = Previous timer interrupt is not a result of a timer input capture event. 1 = Previous timer interrupt is a result of a timer input capture event.

Timer 0–2 Control 1 Register

The Timer 0–2 Control 1 (TxCTL1) Register enables/disables the timer, sets the prescaler value and determines the timer operating mode.

Table 63. Timer 0–2 Control 1 Register (TxCTL1)

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	TEN	TPOL	PRES			TMODE		
RESET	0	0	000			000		
R/W	R/W	R/W	R/W			R/W		
Addr	FF–E307h, FF–E317h, FF–E327h							

Bit	Description
[7] TEN	0 = Timer is disabled. 1 = Timer is enabled. **Note:** the TEN bit is cleared automatically when the timer stops.

PWM High and Low Byte Registers

The PWM High and Low Byte (PWMH and PWML) registers, shown in Table 64 and Table 65) contain the current 12-bit PWM count value. Reads from PWMH stores the value in PWML to a temporary holding register. A read from PWML always returns this temporary register value. It is not recommended to write to the PWM High and Low Byte registers when the PWM is enabled. There are no temporary holding registers for write operations, so simultaneous 12-bit writes are not possible. When either the PWM High and Low Byte registers are written during counting, the 8-bit written value is placed in the counter (High or Low Byte) at the next clock edge. The counter continues counting from the new value.

Table 64. PWM High Byte Register (PWMH)

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	Reserved				PWMH			
RESET	0h				0h			
R/W	R/W				R/W			
Addr	FF_E38Ch							

Bit	Description
[7:4]	**Reserved** These bits are reserved and must be programmed to 0000.
[3:0] PWMH	**PWM High and Low Bytes** The upper byte of two bytes {PWMH[3:0], PWML[7:0]} that contain the current 12-bit PWM count value.

Table 65. PWM Low Byte Register (PWML)

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	PWML							
RESET	01h							
R/W	R/W							
Addr	FF_E38DH							

Bit	Description
[7:0] PWML	**PWM High and Low Bytes** The lower byte of two bytes {PWMH[3:0], PWML[7:0]} that contain the current 12-bit PWM count value.

Bit	Description (Continued)
[3] ADCTRIG	**ADC Trigger Enable** 0 = No ADC trigger pulses. 1 = ADC trigger enabled.
[2]	**Reserved** This bit is reserved and must be programmed to 0.
[1] READY	**Values Ready for Next Reload Event** 0 = PWM values (prescale, period and duty cycle) are not ready. Do not use values in holding registers at next PWM reload event. 1 = PWM values (prescale, period and duty cycle) are ready. Transfer all values from temporary holding registers to working registers at next PWM reload event.
[0] PWMEN	**PWM Enable** 0 = PWM is disabled and enabled PWM output pins are forced to default off-state. PWM master counter is stopped. Certain control registers may only be written in this state. 1 = PWM is enabled and PWM output pins are enabled as outputs.

PWM Control 1 Register

The PWM Control 1 (PWMCTL1) Register controls portions of PWM operation.

Table 71. PWM Control 1 Register (PWMCTL1)

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	RLFREQ[1:0]		INDEN	POL45	POL23	POL10	PRES[1:0]	
RESET	00		0	0	0	0	00	
R/W	R/W		R/W	R/W	R/W	R/W	R/W	
Addr	FF_E381h							

Bit	Description
[7:6] RLFREQ[1:0]	**Reload Event Frequency** This bit field is buffered. Changes to the reload event frequency takes effect at the end of the current PWM period. Reads always return the bit values from the temporary holding register. 00 = PWM reload event occurs at the end of every PWM period. 01 = PWM reload event occurs once every two PWM periods. 10 = PWM reload event occurs once every four PWM periods. 11 = PWM reload event occurs once every eight PWM periods.
[5] INDEN	**Independent PWM Mode Enable** 0 = PWM outputs operate as three complementary pairs. 1 = PWM outputs operate as six independent channels.

PWM Fault Control Register

The PWM Fault Control (PWMFCTL) Register, shown in Table 76, determines how the PWM recovers from a fault condition. Settings in this register select either an automatic or a software-controlled PWM restart.

Table 76. PWM Fault Control Register (PWMFCTL)

Bits	7	6	5	4	3	2	1	0
Field	Reserved	DBGRST	CMP1INT	CMP1RST	CMPINT	CMPRST	Fault0INT	Fault0RST
RESET	0	0	0	0	0	0		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FF_E388h							

Bit	Description
[7]	**Reserved** This bit is reserved and must be programmed to 0.
[6] DBGRST	**Debug Restart** 0 = Automatic recovery. PWM resumes control of outputs when all fault sources have deasstered and a new PWM period begins. 1 = Software controlled recovery. PWM resumes control of outputs only after all fault sources have deasserted and all fault flags are cleared and a PWM reload occurs.
[5] CMP1INT	**Comparator 1 Interrupt** 0 = Interrupt on comparator assertion disabled. 1 = Interrupt on comparator assertion enabled.
[4] CMP1RST	**Comparator 1 Restart** 0 = Automatic recovery. PWM resumes control of outputs when all fault sources have deasstered. **Software Controlled Recovery** 1 = PWM resumes control of outputs only after all fault sources have deasserted and all fault flags are cleared and a PWM reload occurs.
[3 CMP0INT	**Comparator 0 Interrupt** 0 = Interrupt on comparator 0 assertion disabled. 1 = Interrupt on comparator 0 assertion enabled.
[2] CMP0RST	**Comparator 0 Restart** 0 = Automatic recovery. PWM resumes control of outputs when all fault sources have deasstered. **Software Controlled Recovery** 1 = PWM resumes control of outputs only after all fault sources have deasserted and all fault flags are cleared and a PWM reload occurs.

Note: This register can only be written when PWMEN is cleared.

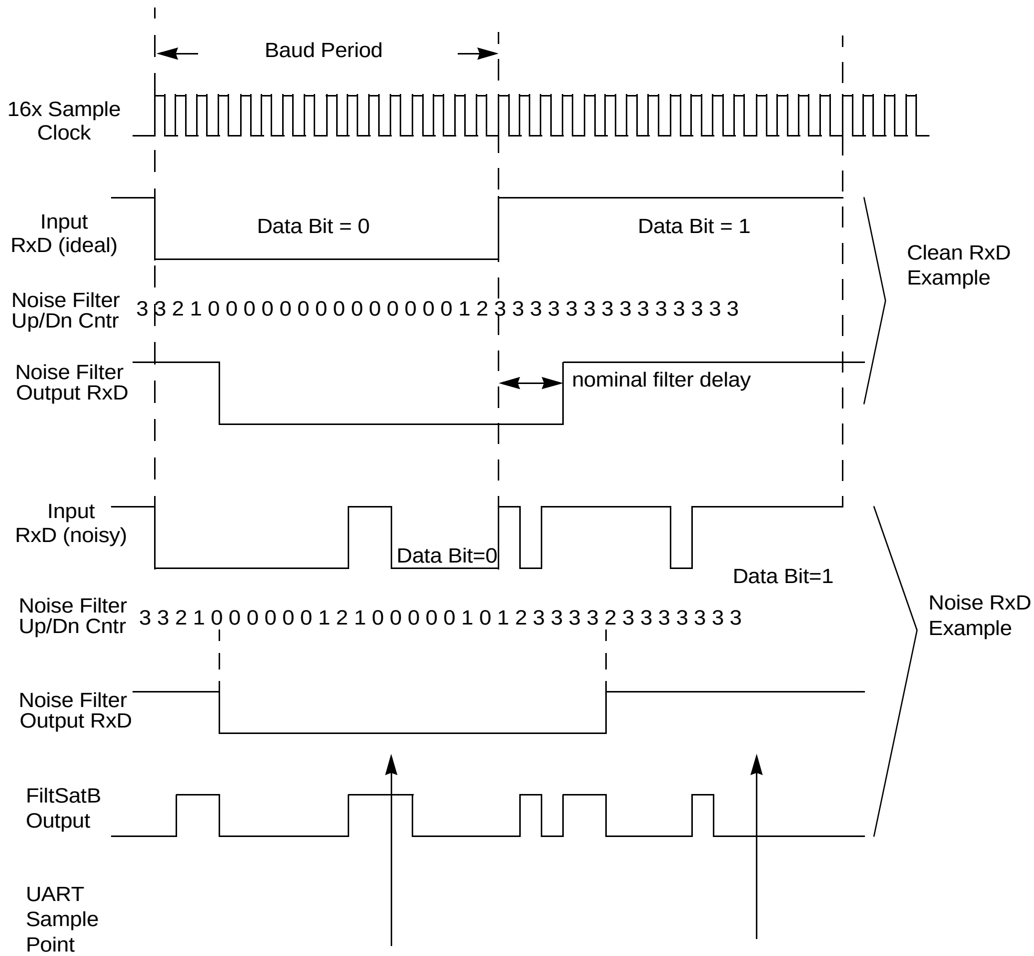

Figure 31. Noise Filter Operation

LIN-UART Control Register Definitions

The LIN-UART control registers support the LIN-UART, the associated Infrared encoder/decoder and the noise filter. For detailed information about the infrared operation, see the Infrared Encoder/Decoder chapter on page 172.

LIN-UART Transmit Data Register

Data bytes written to the LIN-UART Transmit Data Register, shown in Table 80, are shifted out on the TXD pin. The Write-only LIN-UART Transmit Data Register shares a Register File address with the Read-only LIN-UART Receive Data register.

ESPI Control Register Definitions

ESPI Data Register

The ESPI Data Register, shown in Table 102, addresses both the outgoing Transmit Data register and the incoming Receive Data register. Reads from the ESPI Data register return the contents of the Receive Data register. The Receive Data register is updated with the contents of the shift register at the end of each transfer. Writes to the ESPI Data register load the Transmit Data register unless TDRE = 0. Data is shifted out starting with bit 7. The last bit received resides in bit position 0.

With the ESPI configured as a Master, writing a data byte to this register initiates the data transmission. With the ESPI configured as a Slave, writing a data byte to this register loads the shift register in preparation for the next data transfer with the external Master. In either the Master or Slave modes, if TDRE = 0, writes to this register are ignored.

When the character length is less than 8 bits (as set by the NUMBITS field in the ESPI Mode register), the transmit character must be left justified in the ESPI Data register. A received character of less than 8 bits is right justified (last bit received is in bit position 0). For example, if the ESPI is configured for 4-bit characters, the transmit characters must be written to ESPIDATA[7:4] and the received characters are read from ESPIDATA[3:0].

Table 102. ESPI Data Register (ESPIDATA)

Bits	7	6	5	4	3	2	1	0
Field	DATA							
RESET	X	X	X	X	X	X	X	X
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FF_E260h							

Bit	Description
[7:0] DATA	**Data** Transmit and/or receive data. Writes to the ESPIDATA Register load the shift register. Reads from the ESPIDATA Register return the value of the Receive Data Register.

ESPI Transmit Data Command Register

The ESPI Transmit Data Command Register, shown in Table 103, provides control of the $\overline{SS}$ pin when it is configured as an output (Master Mode). The TEOF and SSV bits are controlled by the DMA interface as well as by a bus write to this register.

Following completion of the Stop Mode Recovery, the ZNEO CPU responds to the system exception request by fetching the System Exception vector and executing code from the vector address.

WDT Reset in Normal Operation

If configured to generate a Reset when a time-out occurs, the WDT forces the device into the Reset state. The WDT status bit in the Reset Status and Control Register is set to 1. For more information about Reset and the WDT status bit, see the Reset and Stop Mode Recovery chapter on page 56. Following a Reset sequence, the WDT Counter is initialized with its reset value.

WDT Reset in Stop Mode

If enabled in Stop Mode and configured to generate a Reset when a time-out occurs and the device is in Stop Mode, the WDT initiates a Stop Mode Recovery. Both the WDT status bit and the Stop bit in the Reset Status and Control Register register are set to 1 following WDT time-out in Stop Mode. For detailed information, see the Reset and Stop Mode Recovery chapter on page 56.

Watchdog Timer Reload Unlock Sequence

Writing the unlock sequence to the Watchdog Timer Reload High (WDTH) register address unlocks the two Watchdog Timer Reload registers (WDTH and WDTL) to allow changes to the time-out period. These write operations to the WDTH Register address produce no effect on the bits in the WDTH Register. The locking mechanism prevents spurious writes to the reload registers.

The following sequence is required to unlock the Watchdog Timer Reload registers (WDTH and WDTL) for write access:

1. Write `55h` to the Watchdog Timer Reload High register (WDTH).
2. Write `AAh` to the Watchdog Timer reload high register (WDTH).
3. Write the appropriate value to the Watchdog Timer reload high register (WDTH).
4. Write the appropriate value to the Watchdog Timer reload low register (WDTL).

All steps of the WDT reload unlock sequence must be written in the order presented above. The values in the Watchdog Timer Reload registers are loaded into the counter every time a WDT instruction is executed.

Bit	Description (Continued)
[6] LPOPT	**Low Power Option** 0 = The part will come up in low power mode. The Clock is divided by 8 and Flash memory will only be accessed the last half of the last cycle of the divide. This reduces Flash power consumption. 1 = The part will come up normally.
[5:0]	**Reserved** These option bits are reserved for future use and must always be 1. This setting is the default for unprogrammed (erased) Flash.

Information Area

Data in the information area of memory cannot be altered directly. If you wish to alter the factory settings, it must be done by writing to the Register Address identified. The part defaults to the factory settings after reset and the registers must be rewritten to have the user settings in effect. Read the information area address to determine the factory settings.

IPO Trim Registers (Information Area Address 0021h and 0022h)

Tables 165 and 166 define the IPO Trim settings, which are altered after reset by accessing the IPOTRIM1 and IPOTRIM2 registers.

Table 165. IPO Trim 1 (IPOTRIM1)

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	IPO TEMP TRIM						IPO TRIM	
RESET	L	L	L	L	L	L	L	L
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FFFF_FF25h							
Note: L = Loaded at Reset. R/W = Read/Write. This register is loaded from Information area on Reset.								

Table 166. IPO Trim 2 (IPOTRIM2)

Bits	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	IPO TRIM							
RESET	L	L	L	L	L	L	L	L
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FFFF_FF26							
Note: L = Loaded at Reset. R/W = Read/Write. This register is loaded from Information area on Reset.								

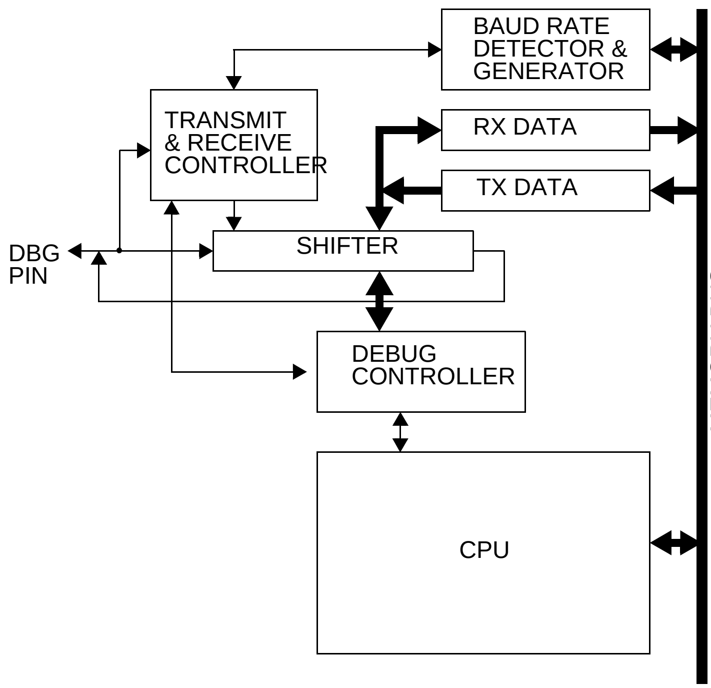

Figure 62. On-Chip Debugger Block Diagram

Operation

> **!** **Caution:** For effective operation of the device, all power pins (V_{DD} and AV_{DD}) must be supplied with power and all ground pins (V_{SS} and AV_{SS}) must be properly grounded. The DBG pin must be connected to V_{DD} through an external pull-up resistor to ensure proper operation.

On-Chip Debug Enable

The DBG pin is mainly used for debugging. The OCD is always enabled by default following reset. Disable the OCD after startup and use the DBG pin as a UART or a GPIO pin if the DBGUART option bit has been cleared.

To use the DBG pin as a UART or GPIO pin, the OCD must be disabled. The OCD is disabled by clearing the OCDEN bit in the Debug Control Register (DBGCTL). The OCD cannot be disabled if the OCDLOCK bit in the DBGCTL Register is set.

Control Register Definitions

Receive Data Register

The Receive Data Register (DBGRXD), shown in Table 170, holds data received by the serial UART.

Table 170. Receive Data Register (DBGRXD)

Bits	7	6	5	4	3	2	1	0
Field	RXDATA							
RESET	XX							
R/W	R/W							
Addr	FF_E080							

Bit	Description
[7:0] RXDATA	**Receive Data** In UART Mode, data received on the serial interface is transferred from the shift register into this register. This register is written to simulate data received if the DBG pin is being used by the OCD.

Transmit Data Register

The Transmit Data Register (DBGTXD), shown in Table 171, holds data to be transmitted by the serial UART.

Table 171. Transmit Data Register (DBGTXD)

Bits	7	6	5	4	3	2	1	0
Field	TXDATA							
RESET	XX							
R/W	R/W							
Addr	FF_E081							

Bit	Description
[7:0] TXDATA	**Transmit Data** In UART Mode, data written to this register is transmitted on the serial interface. This register is read to simulate data transmitted if the DBG pin is being used by the OCD.

Trace Address Register

The Trace Address Register (TRACEADDR), shown in Table 180, points to the next data trace location.

Table 180. Trace Address (TRACEADDR)

Bits	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Field	Reserved								TRACEADDR[23:16]							
RESET	00h								XXH							
R/W	R								R/W							
Addr	FF_E014															
Bits	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Field	TRACEADDR[15:2]														00	
RESET	XXXXH														00	
R/W	R/W														R	
Addr	FF_E016															

Bit	Description
[31:24]	**Reserved** This bit is reserved and must be programmed to 00000000.
[23:16] TRACEADDR[23:16]	**Trace Address** These bits form a 24-bit address used by the trace logic to store the next PC value to memory.
[15:2] TRACEADDR[15:2]	
[1:0] 00	These read-only bits are unused.

Figure 73 displays the typical current consumption while operating at 3.3 V at 30 ºC versus the system clock frequency.

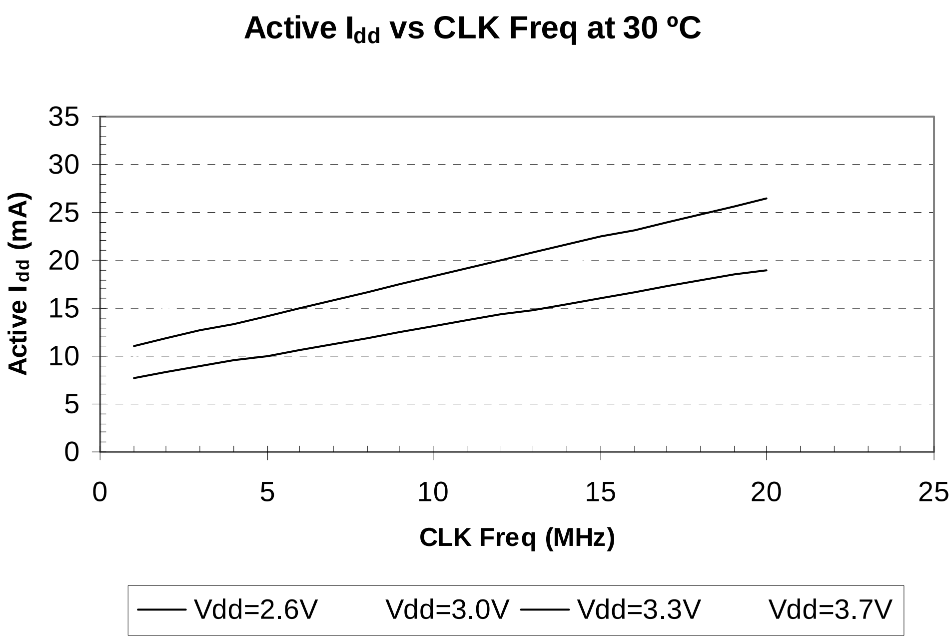

Figure 73. Typical I_{DD} Versus System Clock Frequency

I^2C Timing

Figure 79 and Table 199 provide timing information for I^2C pins.

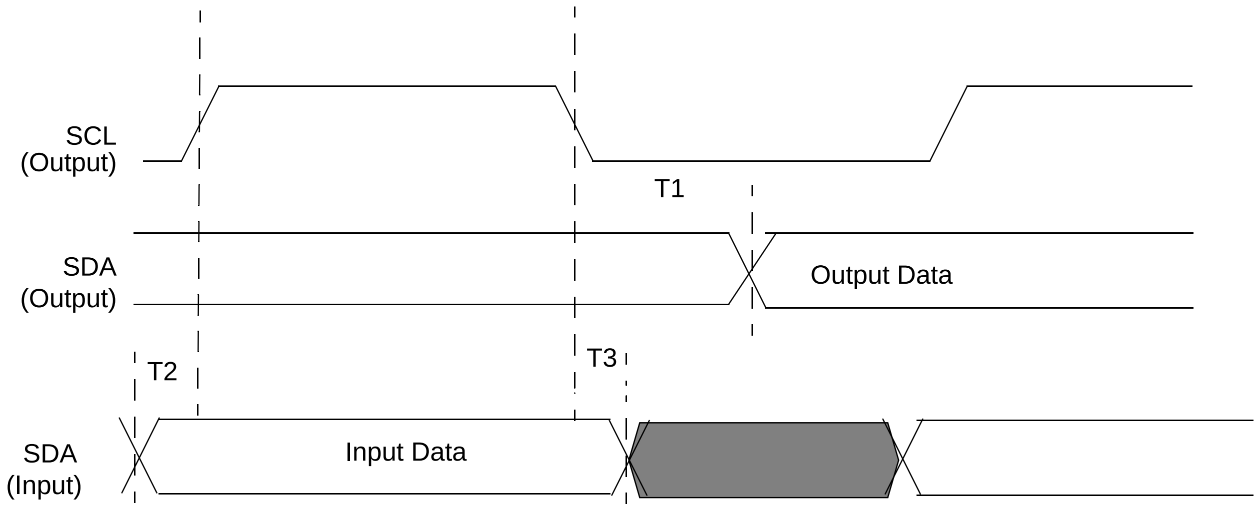

Figure 79. I^2C Timing

Table 199. I^2C Timing

Parameter	Description	Delay (ns)	
		Min	Max
I^2C			
T_1	SCL Fall to SDA output delay	SCL period/4	
T_2	SDA Input to SCL rising edge Setup Time	0	
T_3	SDA Input to SCL falling edge Hold Time	0	

UART Timing

Figure 80 and Table 200 provide timing information for the UART pins in situations in which the Clear To Send input pin ($\overline{CTS}$) is used for flow control. In this example, it is assumed that the Driver Enable polarity has been configured to be Active Low and is represented here by $\overline{DE}$. The $\overline{CTS}$ to $\overline{DE}$ assertion delay (T1) assumes the UART Transmit Data register has been loaded with data prior to $\overline{CTS}$ assertion.

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