Zilog - Z16F6411FI20EG Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ZNEO
Core Size	16-Bit
Speed	20MHz
Connectivity	EBI/EMI, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	60
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-BQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z16f6411fi20eg

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Brackets

The square brackets, [ ], indicate a register or bus.

Example. For the register R1[7:0], R1 is an 8-bit register, R1[7] is the most significant bit, and R1[0] is the least significant bit.

Braces

The curly braces { }, indicate a single register or bus created by concatenating some combination of smaller registers, buses, or individual bits.

Example. The 12-bit register address {0h, RP[7:4], R1[3:0]} is composed of a 4-bit hexadecimal value (0h) and two 4-bit register values taken from the register pointer (RP) and working register R1. 0h is the most significant nibble (4-bit value) of the 12-bit register, and R1[3:0] is the least significant nibble of the 12-bit register.

Parentheses

The parentheses ( ), indicate an indirect register address lookup.

Example. (R1) is the memory location referenced by the address contained in the working register R1.

Parentheses/Bracket Combinations

The parentheses ( ), indicate an indirect register address lookup and the square brackets [ ], indicate a register or bus.

Example. Assume PC[15:0] contains the value 1234h. (PC[15:0]) refers to the contents of the memory location at the address 1234h.

Use of the Words Set, Reset, and Clear

The word set implies that a register bit or a condition contains a logical 1. The words reset or clear imply that a register bit or a condition contains a logical 0. When either of these terms is followed by a number, the word logical may not be included; however, it is implied.

Notation for Bits and Similar Registers

A field of bits within a register is designated as: Register[*n*:*n*].

Example. ADDR[15:0] refers to bit 15 through bit 0 of the address.

Table 6. Register File Address Map (Continued)

Address (Hex)	Register Description	Mnemonic	Reset (Hex)	Page No
FF_E399	PWM 2 High Side Duty Cycle Low Byte	PWMH2DL	00	125
FF_E39A	PWM 2 Low Side Duty Cycle High Byte	PWML2DH	00	124
FF_E39B	PWM 2 Low Side Duty Cycle Low Byte	PWML2DL	00	125
FF_E39C-FF_E3BF	Reserved for PWM	—	—	—
DMA Block Base Address = FF_E400				
DMA Request Selection Control				
FF_E400	DMA0 Request Select	DMA0REQSEL	00	282
FF_E401	DMA1 Request Select	DMA1REQSEL	00	282
FF_E402	DMA2 Request Select	DMA2REQSEL	00	282
FF_E403	DMA3 Request Select	DMA3REQSEL	00	282
FF_E404-F	Reserved	—	—	—
DMA Channel 0 Base Address = FF_E410				
FF_E410	DMA0 Control 0	DMA0CTL0	00	285
FF_E411	DMA0 Control 1	DMA0CTL1	00	285
FF_E412	DMA0 Transfer Length High	DMA0TXLNH	00	286
FF_E413	DMA0 Transfer Length Low	DMA0TXLNL	00	287
FF_E414	Reserved	—	—	—
FF_E415	DMA0 Destination Address Upper	DMA0DARU	00	287
FF_E416	DMA0 Destination Address High	DMA0DARH	00	287
FF_E417	DMA0 Destination Address Low	DMA0DARL	00	287
FF_E418	Reserved	—	—	—
FF_E419	DMA0 Source Address Upper	DMA0SARU	00	288
FF_E41A	DMA0 Source Address High	DMA0SARH	00	288
FF_E41B	DMA0 Source Address Low	DMA0SARL	00	288
FF_E41C	Reserved	—	—	—
FF_E41D	DMA0 List Address Upper	DMA0LARU	00	289
FF_E41E	DMA0 List Address High	DMA0LARH	00	289
FF_E41F	DMA0 List Address Low	DMA0LARL	00	289

XX = Undefined.

tem clock cycles, the device progresses through the System Reset sequence. While the $\overline{\text{RESET}}$ input pin is asserted Low, the ZNEO Z16F Series device continues to be held in the Reset state. If the $\overline{\text{RESET}}$ pin is held Low beyond the System Reset time-out, the device exits the Reset state 16 system clock cycles following $\overline{\text{RESET}}$ pin deassertion. If the $\overline{\text{RESET}}$ pin is released before the System Reset time-out, the $\overline{\text{RESET}}$ pin is driven Low by the chip until the completion of the time-out as described in the next section. In Stop Mode, the digital filter is bypassed as the system clock is disabled.

Following a System Reset initiated by the external $\overline{\text{RESET}}$ pin, the EXT status bit in the Reset Status and Control Register is set to 1.

External Reset Indicator

During System Reset, the $\overline{\text{RESET}}$ pin functions as an open drain (active Low) RESET Mode indicator in addition to the input functionality. This Reset output feature allows a ZNEO Z16F Series device to Reset other components to which it is connected, even if the Reset is caused by internal sources such as POR, VBO or WDT events and as an indication of when the reset sequence completes.

After an internal reset event occurs, the internal circuitry begins driving the $\overline{\text{RESET}}$ pin Low. The $\overline{\text{RESET}}$ pin is held Low by the internal circuitry until the appropriate delay listed in Table 18 on page 56 has elapsed.

User Reset

A System Reset is initiated by setting RSTSCR[0]. If the Write was caused by the OCD, the OCD is not Reset.

Fault Detect Logic Reset

Fault detect circuitry exists to detect *illegal* state changes which is caused by transient power or electrostatic discharge events. When such a fault is detected, a system reset is forced. Following the system reset, the FLTD bit in the Reset Status and Control Register is set.

Stop Mode Recovery

Stop Mode is entered by execution of a Stop instruction by the ZNEO CPU. For detailed information about Stop Mode, see the Low-Power Modes chapter on page 64. During Stop Mode Recovery, the device is held in Reset for 66 cycles of the internal precision oscillator.

Stop Mode Recovery only affects the contents of the the Reset Status and Control Register (see page 62) and the Oscillator Control Register (see page 333). Stop Mode Recovery does not affect any other values in the register file, including the stack pointer, register pointer, flags, peripheral control registers and general-purpose RAM.

The ZNEO CPU fetches the Reset vector at program memory addresses 0004h-0007h and loads that value into the program counter. Program execution begins at the Reset vector address. Following Stop Mode Recovery, the Stop bit in the Reset Status and Control Register is set to 1. Table 20 lists the Stop Mode Recovery sources and resulting actions. The following text provides more detailed information about each of the Stop Mode Recovery sources.

Table 20. Stop Mode Recovery Sources and Resulting Action

Operating Mode	Stop Mode Recovery Source	Action
Stop Mode	WDT time-out when configured for Reset	Stop Mode Recovery
	WDT time-out when configured for System Exception	Stop Mode Recovery followed by WDT System Exception
	Data transition on any GPIO Port pin enabled as a Stop Mode Recovery source	Stop Mode Recovery

Stop Mode Recovery Using WDT Time-Out

If the WDT times out during Stop Mode, the device undergoes a Stop Mode Recovery sequence. In the Reset Status and Control Register, the WDT and Stop bits are set to 1. If the WDT is configured to generate a System Exception on time-out, the ZNEO CPU services the WDT System Exception following the normal Stop Mode Recovery sequence.

Stop Mode Recovery Using a GPIO Port Pin Transition

Each of the GPIO port pins is configured as a Stop Mode Recovery input source. If any GPIO pin enabled as a Stop Mode Recovery source, a change in the input pin value (from High to Low or from Low to High) initiates Stop Mode Recovery. The GPIO Stop Mode Recovery signals are filtered to reject pulses less than 10 ns (typical) in duration. In the Reset Status and Control Register, the Stop bit is set to 1.

Caution: Short pulses on the port pin initiates Stop Mode Recovery without initiating an interrupt (if enabled for that pin).

$$\text{roundup}(\text{PWMMPF}) = T_{\text{minPulseOut}} / (T_{\text{systemClock}} \cdot \text{PWMprescaler})$$

where *minPulseOut* is the shortest allowed pulse width on the PWM outputs (in seconds).

Synchronization of PWM and ADC

The ADC on the ZNeo is synchronized with the PWM period. Enabling the PWM ADC trigger causes the PWM to generate an ADC conversion signal at the end of each PWM period. Additionally, in CENTER-ALIGNED Mode, the PWM generates a trigger at the center of the period. Setting the ADCTRIG bit in the PWM Control 0 Register (PWMCTL0) enables the ADC synchronization.

Synchronized Current-Sense Sample and Hold

The PWM controls the current-sense input sample and hold amplifier. The signal controlling the sample/hold is configured to always sample or automatically hold when any or all of the PWM High or Low outputs are in the on state. The current-sense sample and hold is controlled by the Current-Sense Sample and Hold Control Register (CSSHR0 and CSSHR1).

PWM Timer and Fault Interrupts

The PWM generates interrupts to the ZNEO CPU during any of the following events:

- PWM Reload, in which the interrupt is generated at the end of a PWM period when a PWM register reload occurs
- PWM Fault, in which a fault condition is indicated by asserting any FAULT pins or by the assertion of the comparator

Fault Detection and Protection

The ZNEO contains hardware and software fault controls, which allow rapid deassertion of all enabled PWM output signals. A logic Low on an external fault pin ($\overline{\text{FAULT0}}$ or FAULT1) or the assertion of the over current comparator forces the PWM outputs to the predefined off-state.

Similar deassertion of the PWM outputs is accomplished in software by writing to the PWMOFF bit in the PWM Control 0 Register. The PWM counter continues to operate while the outputs are deasserted (inactive) due to one of these fault conditions.

The fault inputs are individually enabled through the PWM Fault Control Register. If a fault condition is detected and the source is enabled, the fault interrupt is generated. The

PWM Fault Status Register (PWMFSTAT) is read to determine which fault source caused the interrupt.

When a fault is detected and the PWM outputs are disabled, modulator control of the PWM outputs are reenabled either by the software or by the fault input signal deasserting. Selection of the reenable method is made using the PWM Fault Control Register (PWMFCTL). Configuration of the fault modes and reenable methods allow pulse-by-pulse limiting and hard shutdown. When configured in Automatic Restart Mode, the PWM outputs are reengaged at beginning of the next PWM cycle (master timer value is equal to 0) if all fault signals are deasserted. In software controlled restart, all fault inputs must be deasserted and the fault flags must be cleared.

The fault input pin is Schmitt-triggered. The input signal from the pin as well as the comparators pass though an analog filter to reject high-frequency noise.

The logic path from the fault sources to the PWM output is asynchronous ensuring that the fault inputs forces the PWM outputs to their off-state even if the system clock is stopped.

PWM Operation in CPU Halt Mode

When the ZNEO CPU is operating in Halt Mode, the PWM continues to operate if it is enabled. To minimize current in Halt Mode, the PWM must be disabled by clearing the PWMEN bit to 0.

PWM Operation in CPU Stop Mode

When the ZNEO CPU is operating in Stop Mode, the PWM is disabled as the system clock ceases to operate in Stop Mode. The PWM output remains in the same state as they were prior to entering the Stop Mode. In normal operation, the PWM outputs must be disabled by software prior to the CPU entering the Stop Mode. A fault condition detected in Stop Mode forces the PWM outputs to the predefined off-state.

Observing the State of PWM Output Channels

The logic value of the PWM outputs is sampled by reading the PWMIN Register. If a PWM channel pair is disabled (option bit is not set), the associated PWM outputs are forced to high impedance and are used as general purpose inputs.

PWM Control Register Definitions

The following sections describe the various PWM control registers.

Table 69. PWM 0–2 H/L Duty Cycle Low Byte Register (PWMH*x*DL, PWML*x*DL)

Bits	7	6	5	4	3	2	1	0
Field	DUTYL							
RESET	XXH							
R/W	R/W							
Addr	FF_E391h, FF_E393h, FF_E395h, FF_E397h, FF_E399h, FF_E39Bh							

Bit	Description
[7:0] DUTYL	**PWM Duty Cycle High and Low Bytes** The lower byte of two bytes {DUTYH[7:0], DUTYL[7:0]} that form a 14-bit signed value; bits 5 and 6 of the High byte are always 0. The value is compared to the current 12-bit PWM count.

PWM Control 0 Register

The PWM Control 0 Register (PWMCTL0) controls PWM operation.

Table 70. PWM Control 0 Register (PWMCTL0)

Bits	7	6	5	4	3	2	1	0
Field	PWMOFF	OUTCTL	ALIGN	Reserved	ADCTRIG	Reserved	READY	PWMEN
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FF_E380h							

Bit	Description
[7] PWMOFF	**Place PWM Outputs in Off State** 0 = Disable modulator control of PWM pins. Outputs are in predefined off state; not dependent on the Reload event. 1 = Reenable modulator control of PWM pins at next PWM Reload event.
[6] OUTCTL	**PWM Output Control** 0 = PWM outputs are controlled by the pulse-width modulator. 1 = PWM outputs selectively disabled (set to off-state) according to values in the OUT*x* bits of the PWMOUT Register.
[5] ALIGN	**PWM Edge Alignment** 0 = PWM outputs are edge aligned. 1 = PWM outputs are center aligned.
[4]	**Reserved** This bit is reserved and must be programmed to 0.

1. Check the LIN-UART Status 0 Register to determine whether the source of the interrupt is error, break, or received data.
2. If the interrupt was due to data available, read the data from the LIN-UART Receive Data Register. If operating in MULTIPROCESSOR (9-Bit) Mode, further actions are required depending on the Multiprocessor Mode bits MPMD[1:0].
3. Execute the IRET instruction to return from the ISR and await more data.

Clear To Send Operation

The clear to send ($\overline{\text{CTS}}$) pin, if enabled by the CTSE bit of the LIN-UART Control 0 Register, performs flow control on the outgoing transmit data stream. The $\overline{\text{CTS}}$ input pin is sampled one system clock before beginning any new character transmission. To delay transmission of the next data character, an external receiver must deassert $\overline{\text{CTS}}$ at least one system clock cycle before a new data transmission begins. For multiple character transmissions, this operation is typically performed during the Stop bit transmission. If $\overline{\text{CTS}}$ deasserts in the middle of a character transmission, the current character is sent completely.

External Driver Enable

The LIN-UART provides a Driver Enable (DE) signal for off-chip bus transceivers. This feature reduces the software overhead associated with using a GPIO pin to control the transceiver when communicating on a multi-transceiver bus such as RS-485.

Driver Enable is a programmable polarity signal which envelopes the entire transmitted data frame including parity and stop bits as illustrated in Figure 27. The DE signal asserts when a byte is written to the LIN-UART Transmit Data Register. The DE signal asserts at least one bit period and no greater than two bit periods before the Start bit is transmitted. This allows a set-up time to enable the transceiver. The DE signal deasserts one system clock period after the last Stop bit is transmitted. This one system clock delay allows both time for data to clear the transceiver before disabling it, as well as the ability to determine if another character follows the current character. In the event of back to back characters (new data must be written to the Transmit Data Register before the previous character is completely transmitted) the DE signal is not deasserted between characters. The DEPOL bit in the LIN-UART Control Register 1 sets the polarity of the DE signal.

LIN Control Register (LIN-UART Control 1 Register with MSEL = 010b)

When MSEL = 010b, this register, shown in Table 92, provides control for the LIN Mode of operation.

Table 92. LIN Control Register (UxCTL1 with MSEL = 010b)

Bits	7	6	5	4	3	2	1	0
Field	LMST	LSLV	ABEN	ABIEN	LINSTATE[1:0]		TxBreakLength	
RESET	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	FF–E203h, FF–E213h with MSEL = 010b							

Bit	Description
[7] LMST	**LIN Master Mode** 0 = LIN Master Mode not selected. 1 = LIN Master Mode selected (if MPEN, PEN, LSLV = 0)
[6] LSLV	**LIN Slave Mode** 0 = LIN Slave Mode not selected. 1 = LIN Slave Mode selected (if MPEN, PEN, LMST = 0)
[5] ABEN	**Autobaud Enable** 0 = Autobaud not enabled. 1 = Autobaud enabled if in LIN Slave Mode.
[4] ABIEN	**Autobaud Interrupt Enable** 0 = Interrupt following autobaud does not occur. 1 = Interrupt following autobaud enabled if in LIN Slave Mode. When the autobaud character is received, a receive interrupt is generated and the ATB bit is set in the Status 0 Register.
[3:2] LINSTATE[1:0]	**LIN State Machine** The LinState is controlled by both hardware and software. Software force a state change at any time if necessary. In normal operation, software moves the state in and out of Sleep state. For a LIN Slave, software changes the state from Sleep to Wait for Break after which hardware cycles through the Wait for Break, Autobaud and Active states. Software changes the state from one of the active states to Sleep state if the LIN bus goes into Sleep Mode. For a LIN Master, software changes state from Sleep to Active where it remains until software sets it back to the Sleep state. After configuration software does not alter the LinState field during operation. 00 = Sleep State (either LMST or LSLV is set) 01 = Wait for Break state (only valid for LSLV = 1) 10 = Autobaud state (only valid for LSLV = 1) 11 = Active state (either LMST or LSLV is set)

Watchdog Timer

The Watchdog Timer (WDT) helps protect against corrupt or unreliable software, power faults and other system-level problems which places the ZNEO® Z16F Series device into unsuitable operating states.

The WDT includes the following features:

- On-chip RC oscillator
- A selectable time-out response: short reset or system exception
- 16-bit programmable time-out value

Operation

The WDT is a retriggerable one-shot timer that resets or interrupts the ZNEO Z16F Series device, when the WDT reaches its terminal count. The WDT uses its own dedicated on-chip RC oscillator as its clock source. The WDT has only two modes of operation—on and off. After enabled, it always counts and must be refreshed to prevent a time-out. An enable is performed by executing the WDT instruction or by setting the WDT_AO option bit. The WDT_AO bit enables the WDT to operate all of the time, even if a WDT instruction has not been executed.

To minimize power consumption, the RC oscillator is disabled. The RC oscillator is disabled by clearing the WDTEN bit in the Oscillator Control Register. If the RC oscillator is disabled, the WDT will not operate.

The WDT is a 16-bit reloadable downcounter that uses two 8-bit registers in the ZNEO CPU register space to set the reload value. The nominal WDT time-out period is illustrated by the following equation:

$$\text{WDT Time-out Period (ms)} = \frac{\text{WDT Reload Value}}{10}$$

In the equation above, the WDT reload value is the decimal value of the 16-bit value yielded by {WDTH[7:0], WDTL[7:0]} and the typical Watchdog Timer RC oscillator frequency is 10kHz. Table 123 provides approximate time-out delays for the minimum, default and maximum WDT reload values.

Table 138. ZNEO Z16F Series Information Area Map

Program Memory Address (Hex)	Function
000000h–00003Fh	Reserved.
000040h–000053h	Part Number: 20-character ASCII alphanumeric code, left-justified and padded with zeros.
000054h–00007Fh	Reserved.

Operation

The Flash Controller provides the proper signals and timing for the Word programming, Page Erase and Mass erase functions within Flash memory. The Flash Controller contains a protection mechanism, using the Flash Command Register (FCMD), to prevent accidental programming or erasure. The following subsections provide details about the various operations (Lock, Unlock, Sector Protect, Byte Programming, Page Erase and Mass Erase).

Timing Using the Flash Frequency Register

Before performing a program or erase operation on the Flash memory, you must first configure the Flash Frequency Register. The Flash Frequency Register allows programming and erasure of the Flash with system clock frequencies ranging from 32 kHz through 20 MHz (the valid range is limited to the device operating frequencies).

The 16-bit Flash Frequency Register must be written with the system clock frequency in kHz before a program or erase operation is initiated. This value is calculated using the following equation:

$$\text{FFREQ}[15:0] = \frac{\text{System Clock Frequency (Hz)}}{1000}$$

Caution: Flash programming and erasure is not supported for system clock frequencies below 32 kHz, above 20 MHz, or outside of the device operating frequency range. The Flash Frequency Register must be loaded with the correct value to ensure proper Flash programming and erase operations.

- When the upper eight bits of the transfer length equal zero and the lower eight bits of the transfer length is equal to the DMAxLAR[23:16] and the DMA is in DIRECT Mode
- If a buffer has been terminated by a Request EOF

For additional information about interrupts, see the Interrupt Controller chapter on page 80.

DMA Request Select Register

The DMA Request Select Register, shown in Table 148, governs the state of the DMA Channel.

Table 148. DMA Select Register (DAMxREQSEL)

Bits	7	6	5	4	3	2	1	0
Field	CHANSTATE				REQSEL			
RESET	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Addr	FFE400h, FFE401h, FFE402h, FFE403h							

Bit	Description
[7:4] CHANSTATE	**Channel State** 0000 = DMA Off 0001 = DIRECT Mode, Waiting for End of Frame signal 0010 = LINKED LIST Mode, Waiting for End of Frame signal 0011 = Reserved 0100 = DIRECT Mode, First byte transfer, send command 0101 = LINKED LIST Mode, First byte transfer, send command 0110 = DIRECT Mode, Transfer of buffer in progress 0111 = LINKED LIST Mode, Transfer of buffer in progress 1000 = DIRECT Mode, Close Descriptor 1001 = LINKED LIST Mode, New List 1010 = LINKED LIST Mode, Close Descriptor 1011-1111 = Reserved

Table 161. Option Bits At Program Memory Address 0000h

Bits	7	6	5	4	3	2	1	0
Field	OSC_SEL[1:0]		WDT_RES	WDT_AO	VBO_AO	DBGUART	FWP	RP
RESET	U	U	U	U	U	U	U	U
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Addr	Program Memory 0000h							

Note: U = Unchanged by Reset. R/W = Read/Write.

Bit	Description
[7:6] OSC_SEL[1:0]	**Oscillator Mode Selection** 00 = On-chip oscillator configured for use with external RC networks (<4MHz). 01 = Minimum power for use with very low frequency crystals (32kHz to 1.0MHz). 10 = Medium power for use with medium frequency crystals or ceramic resonators (0.5MHz to 10.0MHz). 11 = Maximum power for use with high frequency crystals (8.0MHz to 20.0MHz). This setting is the default for unprogrammed (erased) Flash.
[5] WDT_RES	**WDT Reset** 0 = WDT time-out generates an interrupt request. Interrupts must be globally enabled for the ZNEO CPU to acknowledge the interrupt request. 1 = WDT time-out causes a Short Reset. This setting is the default for unprogrammed (erased) Flash.
[4] WDT_AO	**WDT Always On** 0 = WDT is automatically enabled after reset. The WDT oscillator is disabled by clearing the WDTEN bit in the OSCCTL Register. 1 = WDT is enabled upon execution of the WDT instruction. The WDT oscillator is disabled by clearing the WDTEN bit in the OSCCTL Register.
[3] VBO_AO	**Voltage Brown-Out Protection Always On** 0 = Voltage Brown-Out protection is disabled in Stop Mode to reduce total power consumption. 1 = Voltage Brown-Out protection is always enabled, including during Stop Mode. This setting is the default for unprogrammed (erased) Flash.
[2] DBGUART	**Debug UART Enable** 0 = The Debug UART option is enabled. 1 = The Debug UART option is disabled.

Bit	Description (Continued)
[2] TXCOL	**Transmit Collision** This bit is set when a Transmit Collision occurs. This bit is cleared by writing a one to this bit. 0 = No collision has been detected. 1 = Transmit Collision has been detected.
[1] RXBUSY	**Receiver Busy** This bit is set when the receiver is receiving the data. Multi-master systems uses this bit to ensure the line is idle before sending the data. 0 = Receiver is idle. 1 = Receiver is receiving data.
[0] TXBUSY	**Transmitter Busy** This bit is set when the transmitter is sending the data. This bit is used to determine when to turn off a transceiver for RS-485 applications. 0 = Transmitter is idle. 1 = Transmitter is sending the data.

Control Register

The Control Register (DBGCTL), shown in Table 175, sets the mode of the serial interface.

Table 175. Control Register (DBGCTL)

Bits	7	6	5	4	3	2	1	0
Field	OCDLOCK	OCDEN	Reserved		CRCEN	UARTEN	ABCHAR	ABSRCH
RESET	1	1	00		1	0	0	1
R/W	R/W	R/W	R		R/W	R/W	R/W	R/W
Addr	FF_E086							

Bit	Description
[7] OCDLOCK	**On-Chip Debug Lock** This bit locks the Debug Control register so it cannot be written by the CPU. This bit is automatically set if the DBGUART option bit is in its default erased state (one). 0 = Debug Control register unlocked. 1 = Debug Control register locked.
[6] OCDEN	**On-Chip Debug Enable** This bit is set when the OCD is enabled. When this bit is set, received data is interpreted as debug command. To use the DBG pin as a UART or GPIO pin, this bit must be cleared to 0 by software. This bit cannot be written by the CPU if OCDLOCK is set. 0 = OCD is disabled. 1 = OCD is enabled.

Table 183. Oscillator Control Register (OSCCTL)

Bits	7	6	5	4	3	2	1	0
Field	INTEN	XTLEN	WDTEN	POFEN	WDFEN	FLPEN	SCKSEL	
RESET	1	0	1	0	0	0*	00	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Addr	FF_E0A0h							

Note: *The reset value is 1 if the option bit LPOPT is 0.

Bit	Description
[7] INTEN	**Internal Precision Oscillator Enable** 0 = Internal precision oscillator is disabled. 1 = Internal precision oscillator is enabled.
[6] XTLEN	**Crystal Oscillator Enable** 0 = Crystal oscillator is disabled. 1 = Crystal oscillator is enabled.
[5] WDTEN	**WDT Oscillator Enable** 0 = WDT oscillator is disabled. 1 = WDT oscillator is enabled.
[4] POFEN	**Primary Oscillator Failure Detection Enable** 0 = Failure detection and recovery of primary oscillator is disabled. This bit is cleared automatically if a primary oscillator failure is detected. 1 = Failure detection and recovery of primary oscillator is enabled.
[3] WDFEN	**WDT Oscillator Failure Detection Enable** 0 = Failure detection of WDT oscillator is disabled.This bit is cleared automatically if a WDT oscillator failure is detected. 1 = Failure detection of WDT oscillator is enabled.
[2] FLPEN	**Flash Low Power Mode Enable** 0 = Flash Low Power Mode is disabled. 1 = Flash Low Power Mode is enabled. The Flash will be powered down during idle periods of the clock and powered up during Flash reads. This bit must only be set if the frequency of the primary oscillator source is 8 MHz or lower. The reset value of this bit is controlled by the LPOPT option bit during reset.
[1:0] SCKSEL	**System Clock Oscillator Select** 00 = Internal precision oscillator functions as system clock at 5.6 MHz. 01 = Crystal oscillator or external clock driver functions as system clock. 10 = Reserved. 11 = Watchdog Timer oscillator functions as system clock.

Electrical Characteristics

All data in this chapter is prequalification and precharacterization and is subject to change.

Absolute Maximum Ratings

Stress greater than those listed in Table 185 may cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability. For improved reliability, unused inputs must be tied to one of the supply voltages (V_{DD} or V_{SS}).

Table 185. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units	Notes
Ambient temperature under bias	–40	+125	C	
Storage temperature	–65	+150	C	
Voltage on any pin with respect to V_{SS}	–0.3	+5.5	V	1
Voltage on V_{DD} pin with respect to V_{SS}	–0.3	+3.6	V	2
Maximum current on input and/or inactive output pin	–5	+5	µA	
Maximum output current from active output pin	–25	+25	mA	
100-Pin LQFP Maximum Ratings at –40°C to 70°C				
Total power dissipation		1325	mW	
Maximum current into V_{DD} or out of V_{SS}		368	mA	
100-Pin LQFP Maximum Ratings at 70°C to 125°C				
Total power dissipation		482	mW	
Maximum current into V_{DD} or out of V_{SS}		134	mA	
80-Pin QFP Maximum Ratings at –40°C to 70°C				
Total power dissipation		550	mW	
Maximum current into V_{DD} or out of V_{SS}		150	mA	
80-Pin QFP Maximum Ratings at 70°C to 125°C				
Total power dissipation		200	mW	

Notes:
1. This voltage applies to 5 V tolerant pins which are Port A, C, D, E, F and G pins (except pins PC0 and PC1).
2. This voltage applies to V_{DD}, AV_{DD}, pins supporting analog input (Ports B and H), Pins PC0 and PC1, RESET, DBG and X_{IN} pins which are non 5 V tolerant pins.

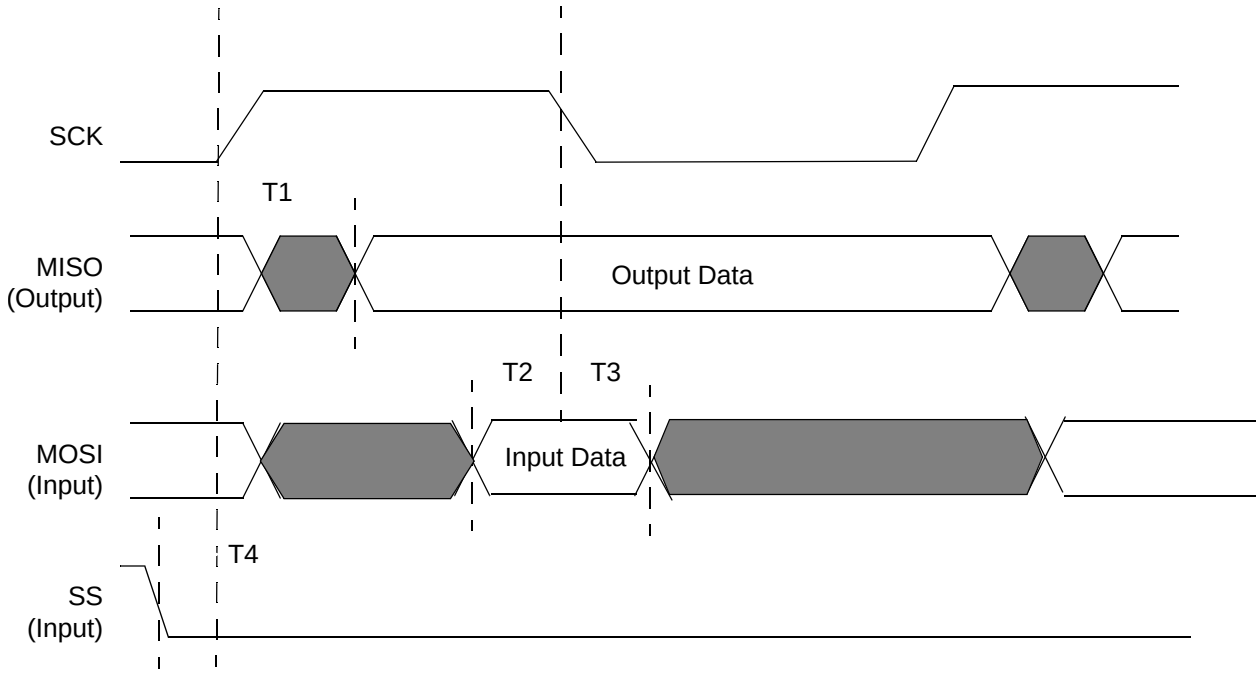

Figure 78. SPI Slave Mode Timing

Table 198. SPI Slave Mode Timing

		Delay (ns)	
Parameter	**Description**	**Min**	**Max**
SPI Slave			
T_1	SCK (transmit edge) to MISO output Valid Delay	2 * X_{IN} period	3 * X_{IN} period + 20 ns
T_2	MOSI input to SCK (receive edge) Setup Time	0	
T_3	MOSI input to SCK (receive edge) Hold Time	3 * X_{IN} period	
T_4	SS input assertion to SCK setup	1 * X_{IN} period	

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