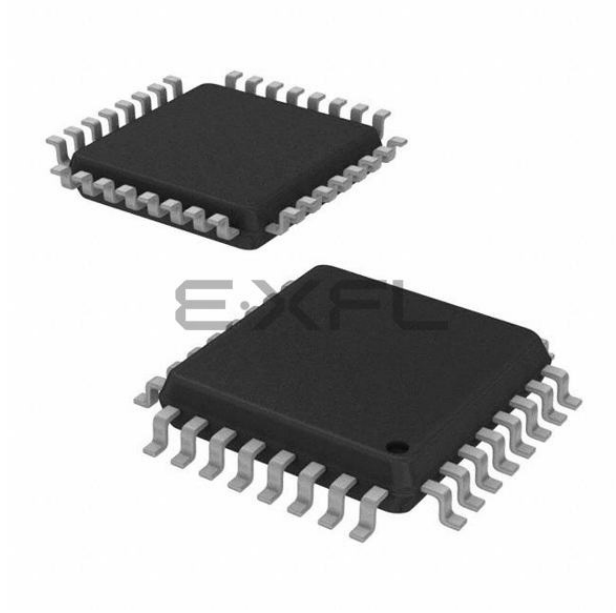

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	20MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	LVD, PWM, WDT
Number of I/O	28
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 16x12b; D/A 2x6b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mke02z16vlc2

1 Ordering parts

1.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to **nxp.com** and perform a part number search for the following device numbers: KE02Z.

2 Part identification

2.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

2.2 Format

Part numbers for this device have the following format:

Q KE## A FFF R T PP CC N

2.3 Fields

This table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Prequalification
KE##	Kinetis family	• KE02
A	Key attribute	• Z = M0+ core
FFF	Program flash memory size	• 16 = 16 KB • 32 = 32 KB • 64 = 64 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main

Table continues on the next page...

Field	Description	Values
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LC = 32 LQFP (7 mm x 7 mm) • LD = 44 LQFP (10 mm x 10 mm) • QH = 64 QFP (14 mm x 14 mm) • LH = 64 LQFP (10 mm x 10 mm)
CC	Maximum CPU frequency (MHz)	• 2 = 20 MHz
N	Packaging type	• R = Tape and reel • (Blank) = Trays

2.4 Example

This is an example part number:

MKE02Z64VQH2

3 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 1. Parameter classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–6000	+6000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 125°C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78D, *IC Latch-up Test*.
   - Test was performed at 125 °C case temperature (Class II).
   - I/O pins pass ±100 mA I-test with I_{DD} current limit at 800 mA.
   - I/O pins pass +60/-100 mA I-test with I_{DD} current limit at 1000 mA.
   - Supply groups pass 1.5 V_{ccmax}.
   - $\overline{\text{RESET}}$ pin was only tested with negative I-test due to product conditioning requirement.

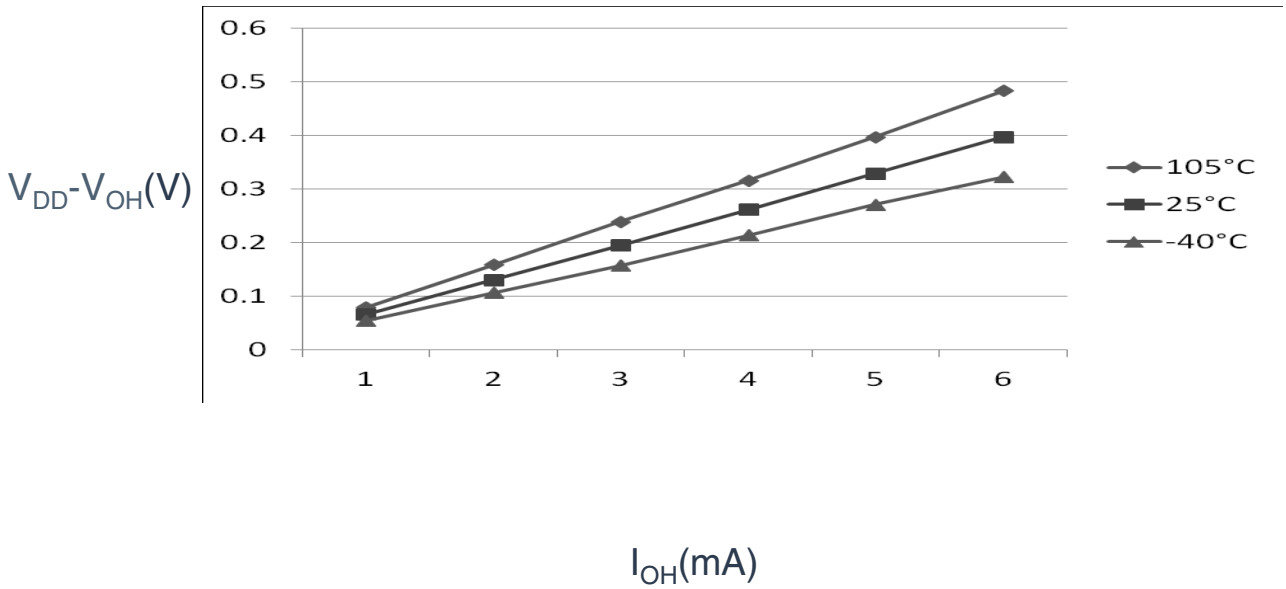

Figure 1. Typical V_{DD}-V_{OH} Vs. I_{OH} (standard drive strength) (V_{DD} = 5 V)

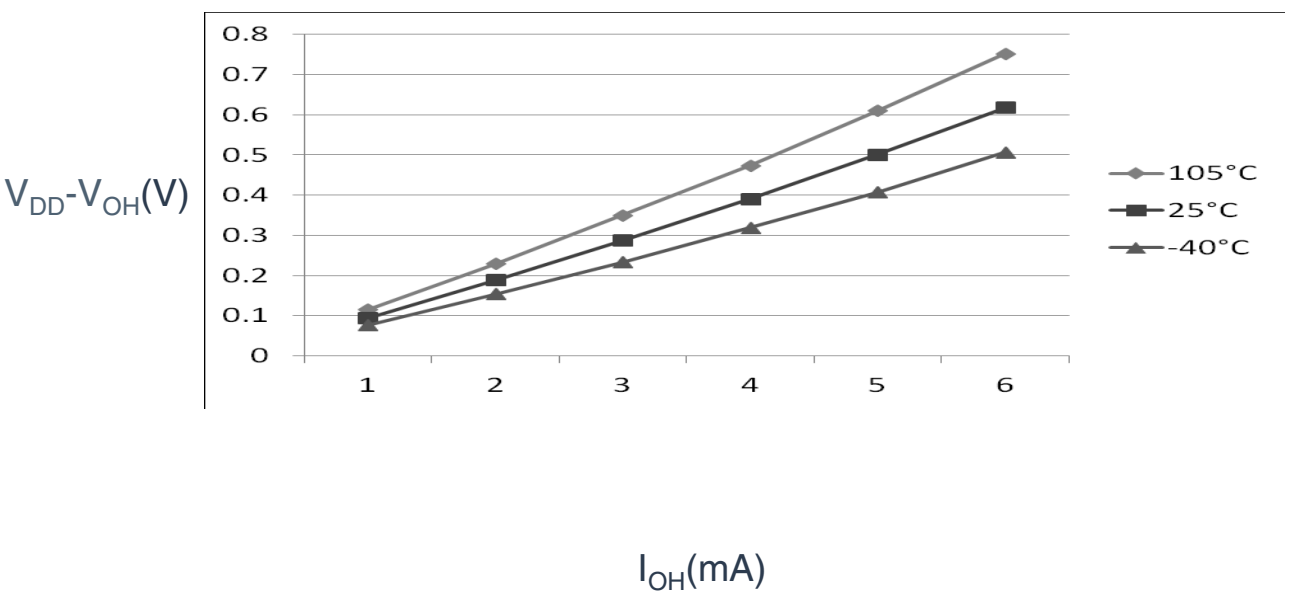

Figure 2. Typical V_{DD}-V_{OH} Vs. I_{OH} (standard drive strength) (V_{DD} = 3 V)

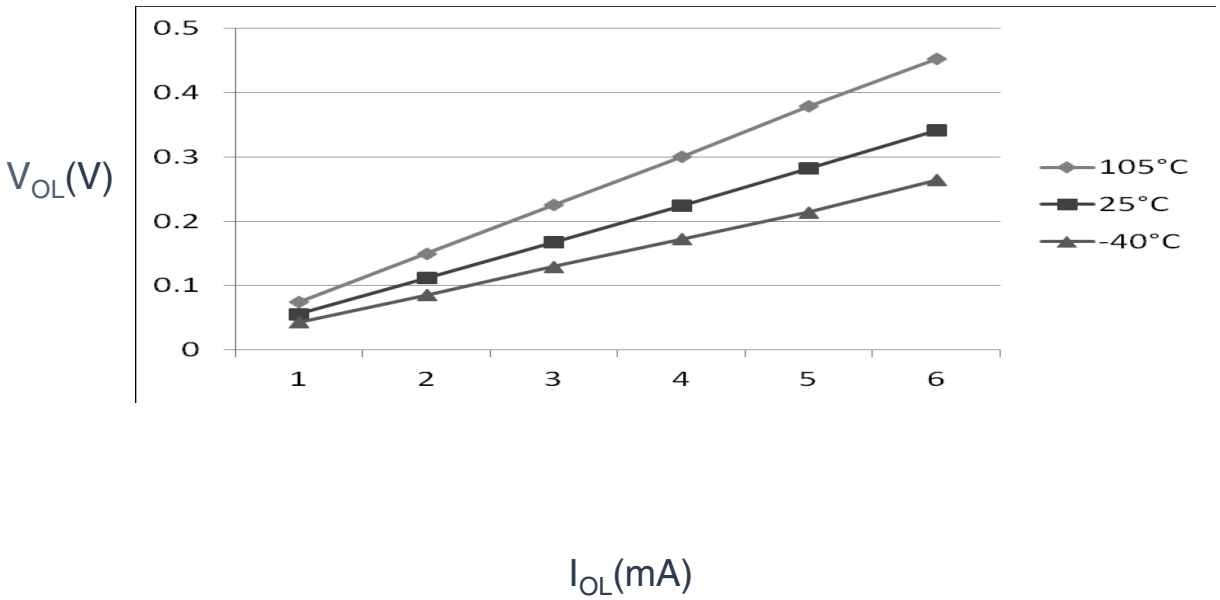

Figure 5. Typical V_{OL} Vs. I_{OL} (standard drive strength) (V_{DD} = 5 V)

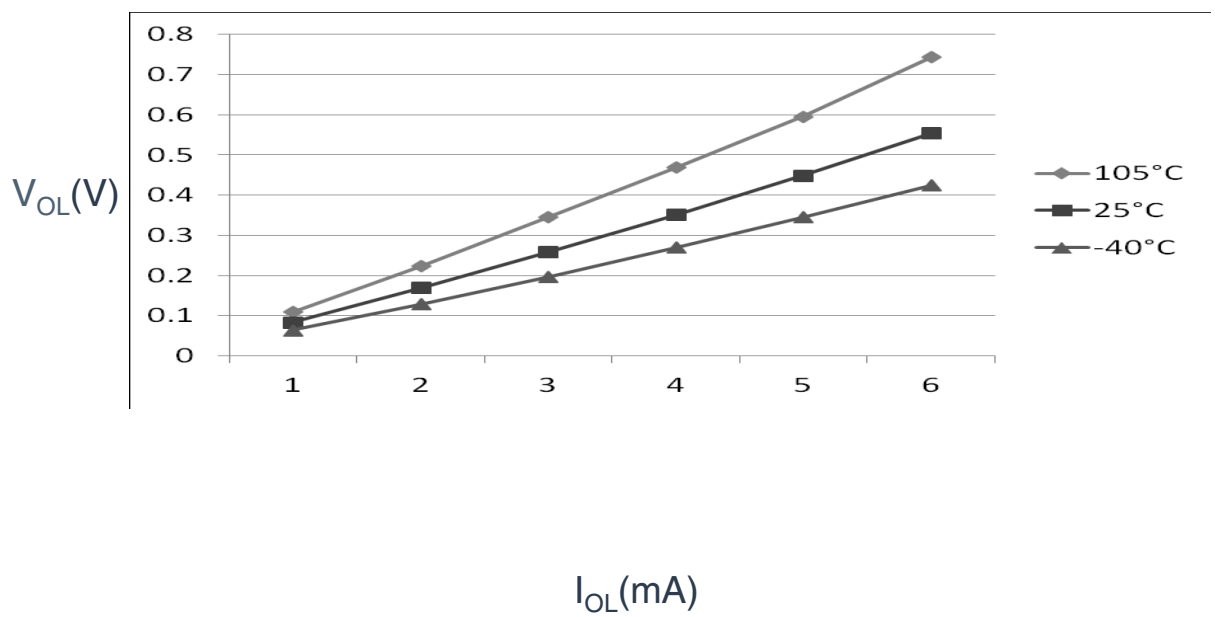

Figure 6. Typical V_{OL} Vs. I_{OL} (standard drive strength) (V_{DD} = 3 V)

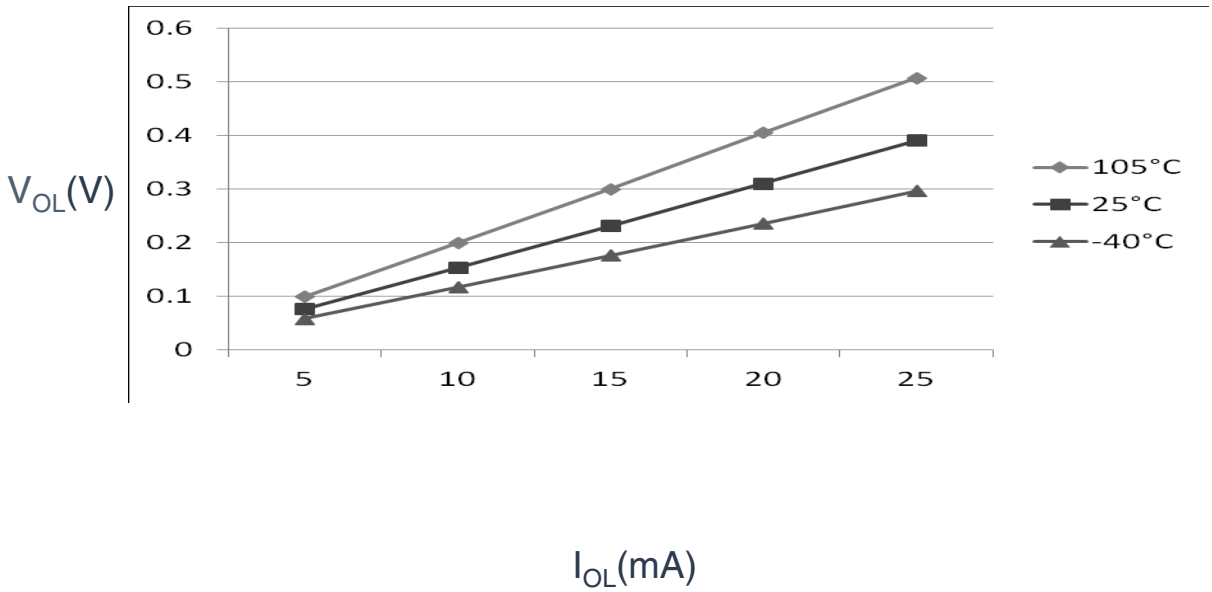

Figure 7. Typical V_{OL} Vs. I_{OL} (high drive strength) (V_{DD} = 5 V)

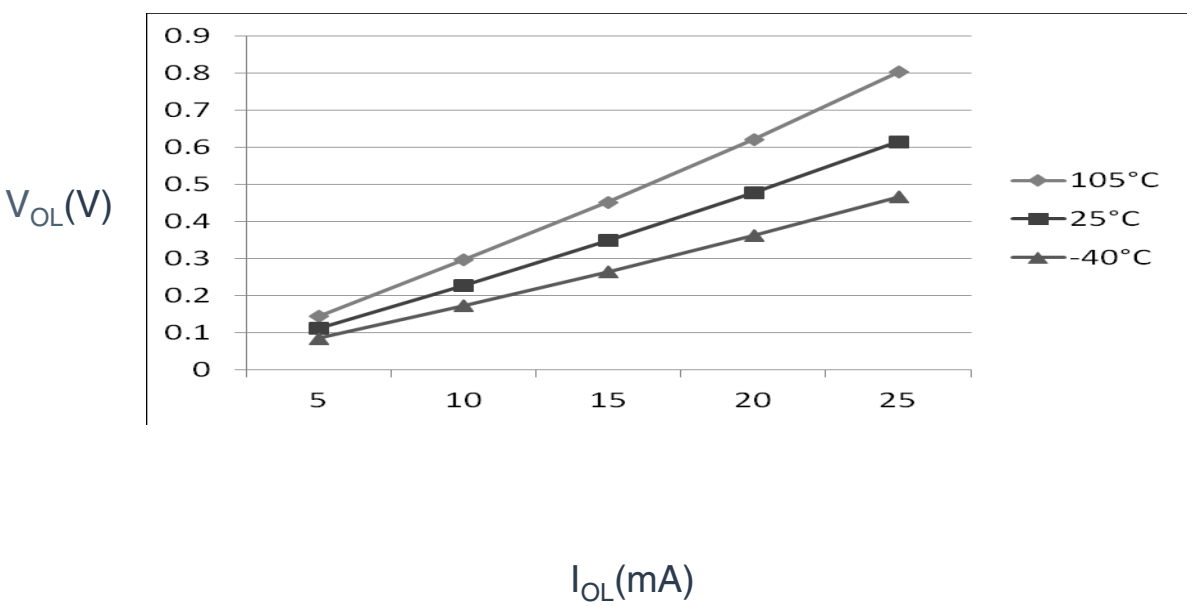

Figure 8. Typical V_{OL} Vs. I_{OL} (high drive strength) (V_{DD} = 3 V)

5.1.2 Supply current characteristics

This section includes information about power supply current in various operating modes.

Table 5. Supply current characteristics

C	Parameter	Symbol	Core/Bus Freq	V_{DD} (V)	Typical[1]	Max[2]	Unit	Temp
C	Run supply current FEI mode, all modules clocks enabled; run from flash	RI_{DD}	20/20 MHz	5	6.7	—	mA	–40 to 105 °C
C			10/10 MHz		4.5	—		
			1/1 MHz		1.5	—		
C			20/20 MHz	3	6.6	—		
C			10/10 MHz		4.4	—		
			1/1 MHz		1.45	—		
C	Run supply current FEI mode, all modules clocks disabled; run from flash	RI_{DD}	20/20 MHz	5	5.3	—	mA	–40 to 105 °C
C			10/10 MHz		3.7	—		
			1/1 MHz		1.5	—		
C			20/20 MHz	3	5.3	—		
C			10/10 MHz		3.7	—		
			1/1 MHz		1.4	—		
P	Run supply current FBE mode, all modules clocks enabled; run from RAM	RI_{DD}	20/20 MHz	5	9	14.8	mA	–40 to 105 °C
C			10/10 MHz		5.2	—		
			1/1 MHz		1.45	—		
P			20/20 MHz	3	8.8	11.8		
C			10/10 MHz		5.1	—		
			1/1 MHz		1.4	—		
P	Run supply current FBE mode, all modules clocks disabled; run from RAM	RI_{DD}	20/20 MHz	5	8	12.3	mA	–40 to 105 °C
C			10/10 MHz		4.4	—		
			1/1 MHz		1.35	—		
P			20/20 MHz	3	7.8	9.2		
C			10/10 MHz		4.2	—		
			1/1 MHz		1.3	—		
P	Wait mode current FEI mode, all modules clocks enabled	WI_{DD}	20/20 MHz	5	5.5	—	mA	–40 to 105 °C
C			20/10 MHz		3.5	—		
			1/1 MHz		1.4	—		
C			20/20 MHz	3	5.4	—		
			10/10 MHz		3.4	—		
			1/1 MHz		1.4	—		
P	Stop mode supply current no clocks active (except 1 kHz LPO clock)[3]	SI_{DD}	—	5	2	85	µA	–40 to 105 °C
P			—	3	1.9	80		–40 to 105 °C

Table continues on the next page...

1. Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.
2. This is the shortest pulse that is guaranteed to be recognized as a $\overline{\text{RESET}}$ pin request.
3. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized.
4. Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range -40 °C to 105 °C.

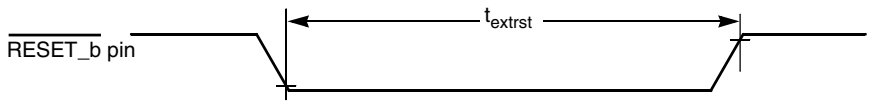

Figure 9. Reset timing

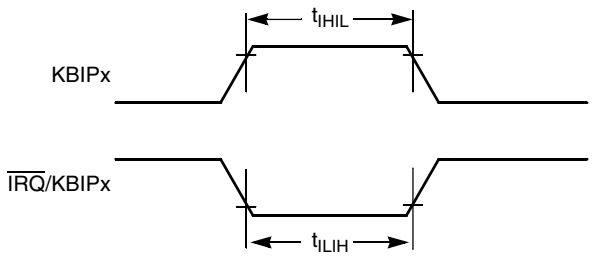

Figure 10. KBIPx timing

5.2.2 FTM module timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 8. FTM input timing

C	Function	Symbol	Min	Max	Unit
D	External clock frequency	f_{TCLK}	0	$f_{Bus}/4$	Hz
D	External clock period	t_{TCLK}	4	—	t_{cyc}
D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

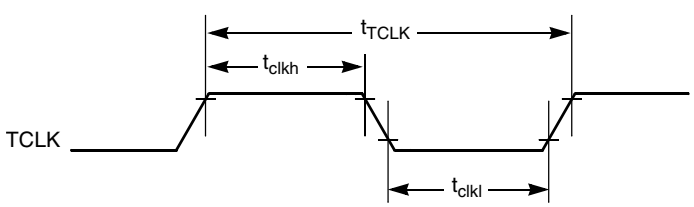

Figure 11. Timer external clock

where K is a constant pertaining to the particular part. K can be determined by measuring P_D (at equilibrium) for an known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving the above equations iteratively for any value of T_A.

6 Peripheral operating requirements and behaviors

6.1 Core modules

6.1.1 SWD electricals

Table 11. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	5.5	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	20	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	3	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	35	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

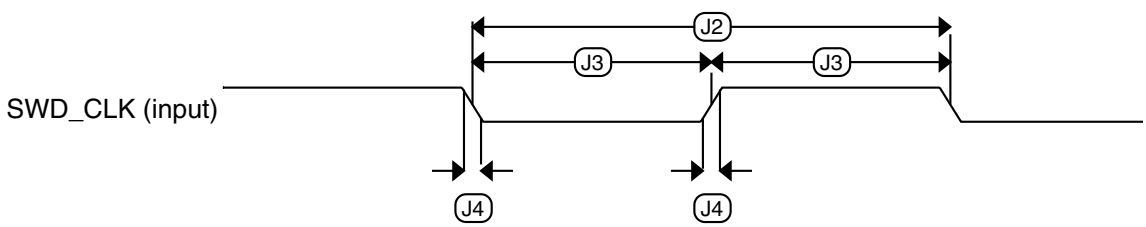

Figure 13. Serial wire clock input timing

Table 12. OSC and ICS specifications (temperature range = -40 to 105 °C ambient) (continued)

Num	C	Characteristic		Symbol	Min	Typical[1]	Max	Unit
	D	Series resistor - High Frequency, High-Gain Mode	4 MHz		—	0	—	kΩ
	D		8 MHz		—	0	—	kΩ
	D		16 MHz		—	0	—	kΩ
6	C	Crystal start-up time low range = 32.768 kHz crystal; High range = 20 MHz crystal[4,5]	Low range, low power	t_{CSTL}	—	1000	—	ms
	C		Low range, high gain		—	800	—	ms
	C		High range, low power	t_{CSTH}	—	3	—	ms
	C		High range, high gain		—	1.5	—	ms
7	T	Internal reference start-up time		t_{IRST}	—	20	50	µs
8	P	Internal reference clock (IRC) frequency trim range		f_{int_t}	31.25	—	39.0625	kHz
9	P	Internal reference clock frequency, factory trimmed,	T = 25 °C, V_{DD} = 5 V	f_{int_ft}	—	31.25	—	kHz
10	P	DCO output frequency range	FLL reference = fint_t, flo, or fhi/RDIV	f_{dco}	16	—	20	MHz
11	P	Factory trimmed internal oscillator accuracy	T = 25 °C, V_{DD} = 5 V	Δf_{int_ft}	-0.5	—	0.5	%
12	C	Deviation of IRC over temperature when trimmed at T = 25 °C, V_{DD} = 5 V	Over temperature range from -40 °C to 105°C	Δf_{int_t}	-1	—	0.5	%
			Over temperature range from 0 °C to 105°C	Δf_{int_t}	-0.5	—	0.5	
13	C	Frequency accuracy of DCO output using factory trim value	Over temperature range from -40 °C to 105°C	Δf_{dco_ft}	-1.5	—	1	%
			Over temperature range from 0 °C to 105°C	Δf_{dco_ft}	-1	—	1	
14	C	FLL acquisition time[4,6]		$t_{Acquire}$	—	—	2	ms
15	C	Long term jitter of DCO output clock (averaged over 2 ms interval)[7]		C_{Jitter}	—	0.02	0.2	$\%f_{dco}$

1. Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.
2. See crystal or resonator manufacturer's recommendation.
3. Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE = HGO = 0.
4. This parameter is characterized and not tested on each device.
5. Proper PC board layout procedures must be followed to achieve specifications.
6. This specification applies to any time the FLL reference source or reference divider is changed, trim value changed, or changing from FLL disabled (FBELP, FBILP) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{Bus}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

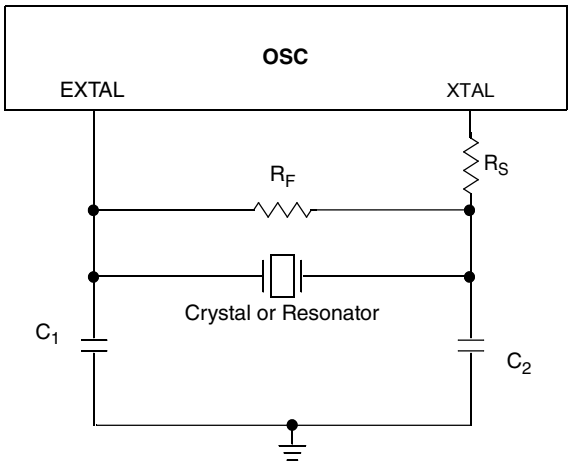

Figure 15. Typical crystal or resonator circuit

6.3 NVM specifications

This section provides details about program/erase times and program/erase endurance for the flash and EEPROM memories.

Table 13. Flash and EEPROM characteristics

C	Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
D	Supply voltage for program/erase –40 °C to 105 °C	$V_{prog/erase}$	2.7	—	5.5	V
D	Supply voltage for read operation	V_{Read}	2.7	—	5.5	V
D	NVM Bus frequency	f_{NVMBUS}	1	—	25	MHz
D	NVM Operating frequency	f_{NVMOP}	0.8	1	1.05	MHz
D	Erase Verify All Blocks	t_{VFYALL}	—	—	17338	t_{cyc}
D	Erase Verify Flash Block	t_{RD1BLK}	—	—	16913	t_{cyc}
D	Erase Verify EEPROM Block	t_{RD1BLK}	—	—	810	t_{cyc}
D	Erase Verify Flash Section	t_{RD1SEC}	—	—	484	t_{cyc}
D	Erase Verify EEPROM Section	$t_{DRD1SEC}$	—	—	555	t_{cyc}
D	Read Once	t_{RDONCE}	—	—	450	t_{cyc}
D	Program Flash (2 word)	t_{PGM2}	0.12	0.12	0.29	ms
D	Program Flash (4 word)	t_{PGM4}	0.20	0.21	0.46	ms
D	Program Once	$t_{PGMONCE}$	0.20	0.21	0.21	ms
D	Program EEPROM (1 Byte)	t_{DPGM1}	0.10	0.10	0.27	ms
D	Program EEPROM (2 Byte)	t_{DPGM2}	0.17	0.18	0.43	ms
D	Program EEPROM (3 Byte)	t_{DPGM3}	0.25	0.26	0.60	ms
D	Program EEPROM (4 Byte)	t_{DPGM4}	0.32	0.33	0.77	ms
D	Erase All Blocks	t_{ERSALL}	96.01	100.78	101.49	ms
D	Erase Flash Block	t_{ERSBLK}	95.98	100.75	101.44	ms

Table continues on the next page...

Table 13. Flash and EEPROM characteristics (continued)

C	Characteristic	Symbol	Min[1]	Typical[2]	Max[3]	Unit[4]
D	Erase Flash Sector	t_{ERSPG}	19.10	20.05	20.08	ms
D	Erase EEPROM Sector	t_{DERSPG}	4.81	5.05	20.57	ms
D	Unsecure Flash	t_{UNSECU}	96.01	100.78	101.48	ms
D	Verify Backdoor Access Key	t_{VFYKEY}	—	—	464	t_{cyc}
D	Set User Margin Level	t_{MLOADU}	—	—	407	t_{cyc}
C	FLASH Program/erase endurance T_L to T_H = -40 °C to 105 °C	n_{FLPE}	10 k	100 k	—	Cycles
C	EEPROM Program/erase endurance TL to TH = -40 °C to 105 °C	n_{FLPE}	50 k	500 k	—	Cycles
C	Data retention at an average junction temperature of T_{Javg} = 85°C after up to 10,000 program/erase cycles	t_{D_ret}	15	100	—	years

1. Minimum times are based on maximum f_{NVMOP} and maximum f_{NVMBUS}
2. Typical times are based on typical f_{NVMOP} and maximum f_{NVMBUS}
3. Maximum times are based on typical f_{NVMOP} and typical f_{NVMBUS} plus aging
4. $t_{cyc} = 1 / f_{NVMBUS}$

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Flash Memory Module section in the reference manual.

6.4 Analog

6.4.1 ADC characteristics

Table 14. 5 V 12-bit ADC operating conditions

Characteristic	Conditions	Symbol	Min	Typ[1]	Max	Unit	Comment
Reference potential	• Low • High	V_{REFL} V_{REFH}	V_{SSA} V_{DDA}	— —	V_{SSA} V_{DDA}	V	—
Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
	Delta to V_{DD} (V_{DD}-V_{DDA})	ΔV_{DDA}	-100	0	+100	mV	—
Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSA})	ΔV_{SSA}	-100	0	+100	mV	—
Input voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
Input capacitance		C_{ADIN}	—	4.5	5.5	pF	—

Table continues on the next page...

Table 15. 12-bit ADC characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Characteristic	Conditions	C	Symbol	Min	Typ[1]	Max	Unit
ADCO = 1							
Supply current ADLPC = 1 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	218	—	µA
Supply current ADLPC = 0 ADLSMP = 1 ADCO = 1		T	I_{DDA}	—	327	—	µA
Supply current ADLPC = 0 ADLSMP = 0 ADCO = 1		T	I_{DDA}	—	582	990	µA
Supply current	Stop, reset, module off	T	I_{DDA}	—	0.011	1	µA
ADC asynchronous clock source	High speed (ADLPC = 0)	P	f_{ADACK}	2	3.3	5	MHz
	Low power (ADLPC = 1)			1.25	2	3.3	
Conversion time (including sample time)	Short sample (ADLSMP = 0)	T	t_{ADC}	—	20	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	40	—	
Sample time	Short sample (ADLSMP = 0)	T	t_{ADS}	—	3.5	—	ADCK cycles
	Long sample (ADLSMP = 1)			—	23.5	—	
Total unadjusted Error[2]	12-bit mode[3]	T	E_{TUE}	—	±3.6	—	LSB[4]
	10-bit mode	P		—	±1.5	±2.0	
	8-bit mode	T		—	±0.7	±1.0	
Differential Non-Liniarity	12-bit mode	T	DNL	—	±1.0	—	LSB[4]
	10-bit mode[5]	P		—	±0.25	±0.5	
	8-bit mode[5]	T		—	±0.15	±0.25	
Integral Non-Linearity	12-bit mode[3]	T	INL	—	±1.0	—	LSB[4]
	10-bit mode	T		—	±0.3	±0.5	
	8-bit mode	T		—	±0.15	±0.25	
Zero-scale error[6]	12-bit mode	C	E_{ZS}	—	±2.0	—	LSB[4]
	10-bit mode	P		—	±0.25	±1.0	
	8-bit mode	T		—	±0.65	±1.0	
Full-scale error[7]	12-bit mode	T	E_{FS}	—	±2.5	—	LSB[4]
	10-bit mode	T		—	±0.5	±1.0	

Table continues on the next page...

Table 15. 12-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Characteristic	Conditions	C	Symbol	Min	Typ[1]	Max	Unit
	8-bit mode	T		—	±0.5	±1.0	
Quantization error	≤12 bit modes	D	E_Q	—	—	±0.5	LSB[4]
Input leakage error[8]	all modes	D	E_{IL}	I_{In} * R_{AS}			mV
Temp sensor slope	-40 °C–25 °C	D	m	—	3.266	—	mV/°C
	25 °C–125 °C			—	3.638	—	
Temp sensor voltage	25 °C	D	V_{TEMP25}	—	1.396	—	V

1. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Includes quantization
3. This parameter is valid for the temperature range of 25 °C to 50 °C.
4. 1 LSB = (V_{REFH} - V_{REFL})/2^N
5. Monotonicity and no-missing-codes guaranteed in 10-bit and 8-bit modes
6. V_{ADIN} = V_{SSA}
7. V_{ADIN} = V_{DDA}
8. I_{In} = leakage current (refer to DC characteristics)

6.4.2 Analog comparator (ACMP) electricals

Table 16. Comparator electrical specifications

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage	V_{DDA}	2.7	—	5.5	V
T	Supply current (Operation mode)	I_{DDA}	—	10	20	µA
D	Analog input voltage	V_{AIN}	V_{SS} - 0.3	—	V_{DDA}	V
P	Analog input offset voltage	V_{AIO}	—	—	40	mV
C	Analog comparator hysteresis (HYST=0)	V_H	—	15	20	mV
C	Analog comparator hysteresis (HYST=1)	V_H	—	20	30	mV
T	Supply current (Off mode)	I_{DDAOFF}	—	60	—	nA
C	Propagation Delay	t_D	—	0.4	1	µs

6.5 Communication interfaces

6.5.1 SPI switching specifications

The serial peripheral interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's reference manual for information about the modified transfer formats used for

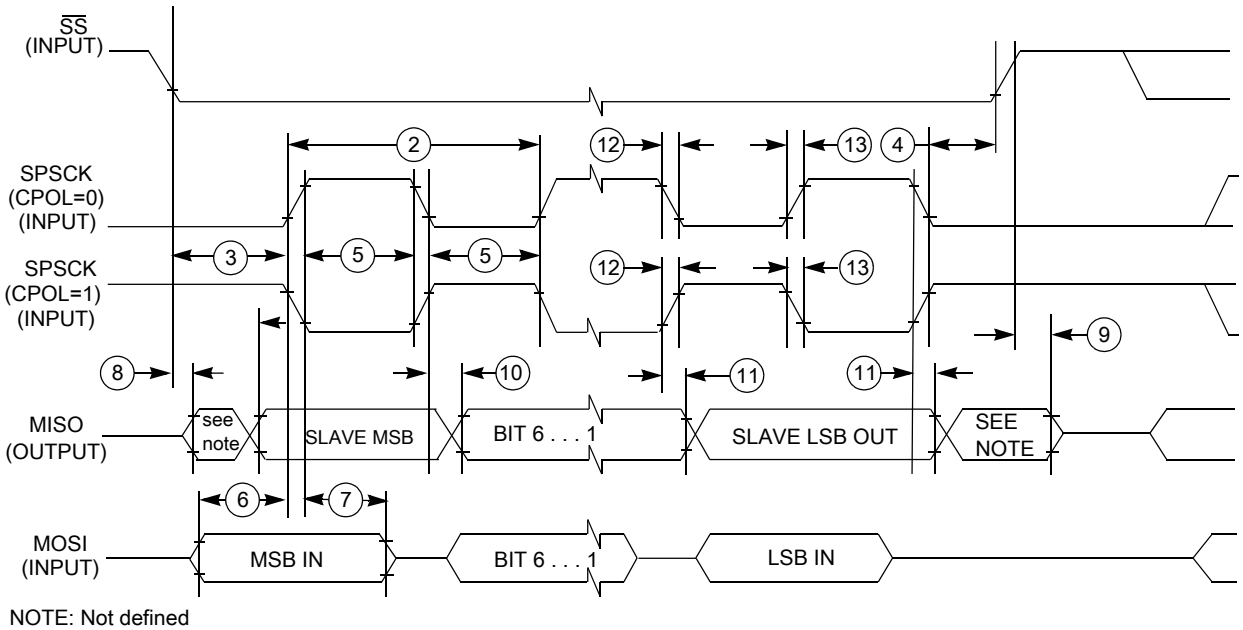

Figure 19. SPI slave mode timing (CPHA = 0)

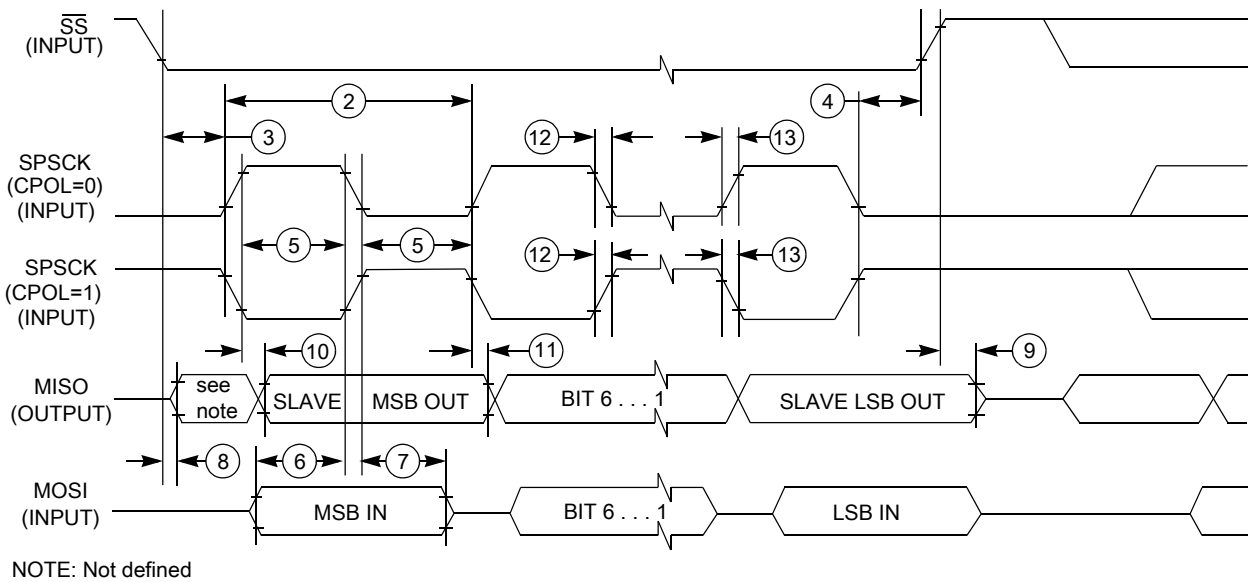

Figure 20. SPI slave mode timing (CPHA=1)

7 Dimensions

7.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to **nxp.com** and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
32-pin LQFP	98ASH70029A
44-pin LQFP	98ASS23225W
64-pin QFP	98ASB42844B
64-pin LQFP	98ASS23234W

8 Pinout

8.1 Signal multiplexing and pin assignments

The following table shows the signals available on each pin and the locations of these pins on the devices supported by this document. The Port Control Module is responsible for selecting which ALT functionality is available on each pin.

Table 19. Pin availability by package pin-count

Pin Number			Lowest Priority <-- --> Highest				
64-QFP/ LQFP	44-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
1	1	1	PTD1[1]	KBI1_P1	FTM2_CH3	SPI1_MOSI	—
2	2	2	PTD0[1]	KBI1_P0	FTM2_CH2	SPI1_SCK	—
3	—	—	PTH7	—	—	—	—
4	—	—	PTH6	—	—	—	—
5	3	—	PTE7	—	FTM2_CLK	—	FTM1_CH1
6	4	—	PTH2	—	BUSOUT	—	FTM1_CH0
7	5	3	—	—	—	—	VDD
8	6	4	—	—	—	VDDA	VREFH[2]
9	7	5	—	—	—	—	VREFL
10	8	6	—	—	—	VSSA	VSS[3]
11	9	7	PTB7	—	I2C0_SCL	—	EXTAL
12	10	8	PTB6	—	I2C0_SDA	—	XTAL
13	11	—	—	—	—	—	VSS
14	—	—	PTH1[1]	—	FTM2_CH1	—	—
15	—	—	PTH0[1]	—	FTM2_CH0	—	—
16	—	—	PTE6	—	—	—	—
17	—	—	PTE5	—	—	—	—
18	12	9	PTB5[1]	FTM2_CH5	SPI0_PCS0	ACMP1_OUT	—

Table continues on the next page...

Table 19. Pin availability by package pin-count (continued)

Pin Number			Lowest Priority <-- --> Highest				
64-QFP/ LQFP	44-LQFP	32-LQFP	Port Pin	Alt 1	Alt 2	Alt 3	Alt 4
19	13	10	PTB4[1]	FTM2_CH4	SPI0_MISO	$\overline{\text{NMI}}$	ACMP1_IN2
20	14	11	PTC3	FTM2_CH3	—	—	ADC0_SE11
21	15	12	PTC2	FTM2_CH2	—	—	ADC0_SE10
22	16	—	PTD7	KBI1_P7	UART2_TX	—	—
23	17	—	PTD6	KBI1_P6	UART2_RX	—	—
24	18	—	PTD5	KBI1_P5	—	—	—
25	19	13	PTC1	—	FTM2_CH1	—	ADC0_SE9
26	20	14	PTC0	—	FTM2_CH0	—	ADC0_SE8
27	—	—	PTF7	—	—	—	ADC0_SE15
28	—	—	PTF6	—	—	—	ADC0_SE14
29	—	—	PTF5	—	—	—	ADC0_SE13
30	—	—	PTF4	—	—	—	ADC0_SE12
31	21	15	PTB3	KBI0_P7	SPI0_MOSI	FTM0_CH1	ADC0_SE7
32	22	16	PTB2	KBI0_P6	SPI0_SCK	FTM0_CH0	ADC0_SE6
33	23	17	PTB1	KBI0_P5	UART0_TX	—	ADC0_SE5
34	24	18	PTB0	KBI0_P4	UART0_RX	—	ADC0_SE4
35	—	—	PTF3	—	—	—	—
36	—	—	PTF2	—	—	—	—
37	25	19	PTA7	—	FTM2_FLT2	ACMP1_IN1	ADC0_SE3
38	26	20	PTA6	—	FTM2_FLT1	ACMP1_IN0	ADC0_SE2
39	—	—	PTE4	—	—	—	—
40	27	—	—	—	—	—	VSS
41	28	—	—	—	—	—	VDD
42	—	—	PTF1	—	—	—	—
43	—	—	PTF0	—	—	—	—
44	29	—	PTD4	KBI1_P4	—	—	—
45	30	21	PTD3	KBI1_P3	SPI1_PCS0	—	—
46	31	22	PTD2	KBI1_P2	SPI1_MISO	—	—
47	32	23	PTA3[4]	KBI0_P3	UART0_TX	I2C0_SCL	—
48	33	24	PTA2[4]	KBI0_P2	UART0_RX	I2C0_SDA	—
49	34	25	PTA1	KBI0_P1	FTM0_CH1	ACMP0_IN1	ADC0_SE1
50	35	26	PTA0	KBI0_P0	FTM0_CH0	ACMP0_IN0	ADC0_SE0
51	36	27	PTC7	—	UART1_TX	—	—
52	37	28	PTC6	—	UART1_RX	—	—
53	—	—	PTE3	—	SPI0_PCS0	—	—
54	38	—	PTE2	—	SPI0_MISO	—	—
55	—	—	PTG3	—	—	—	—
56	—	—	PTG2	—	—	—	—

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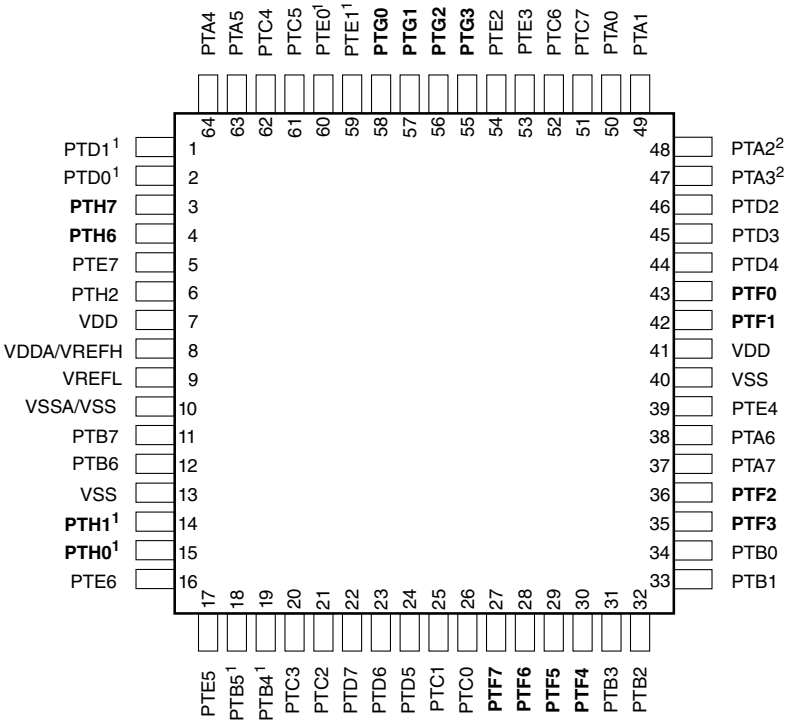
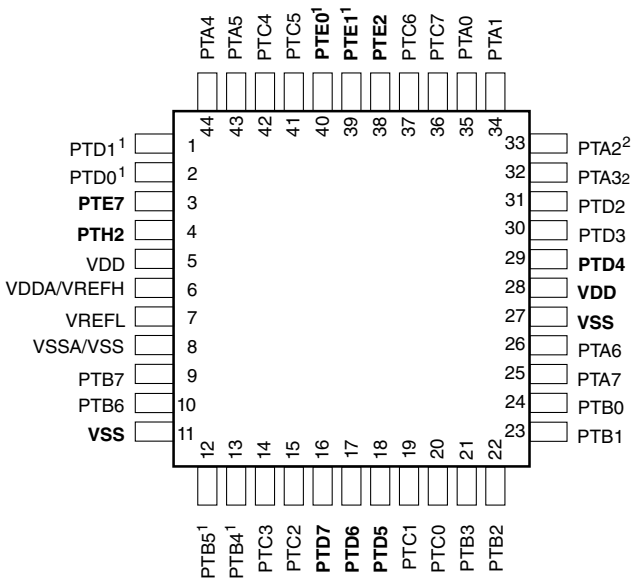


Pins in **bold** are not available on less pin-count packages.
1. High source/sink current pins
2. True open drain pins

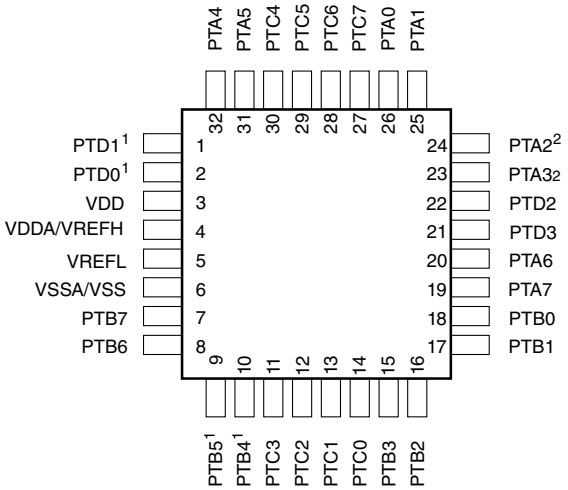
Figure 21. 64-pin QFP/LQFP packages



Pins in **bold** are not available on less pin-count packages.

1. High source/sink current pins
2. True open drain pins

Figure 22. 44-pin LQFP package



1. High source/sink current pins
2. True open drain pins

Figure 23. 32-pin LQFP package

9 Revision history

The following table provides a revision history for this document.

Table 20. Revision history

Rev. No.	Date	Substantial Changes
3	07/2013	Initial public release.
4	10/2014	• Updated all the V_{DDAD} to V_{DDA}, V_{SSAD} to V_{SSA} • Updated the features of OSC, ICS, UART, KBI and ADC in the front page • Updated I_{LAT} and V_{CDM} in the ESD handling ratings • Added V_{IN} and removed V_{DIO}, V_{AIO} in the Voltage and current operating ratings • Updated DC characteristics • Added the item of ACMP adder to Stop and a note to the Max. in Supply current characteristics • Added EMC radiated emissions operating behaviors • Added f_{Sys} and a note to t_{IHIL} in the Control timing • Added a new section of Thermal operating requirements • Updated J1, J10 and J11 in the SWD electricals • Updated External oscillator (OSC) and ICS characteristics • Added reference potential and a note to the E_{TUE} and E_{ZS} in ADC characteristics • Updated SPI switching specifications
5	07/2016	• Updated the Typical value of E_{TUE} in 12-bit mode and added a note to the 12-bit mode of E_{TUE} and INL in the ADC characteristics.

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