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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	4.7 ns
Voltage Supply - Internal	2.5V, 3.3V
Number of Logic Elements/Blocks	240
Number of Macrocells	192
Number of Gates	-
Number of I/O	80
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm240t100i5n

MAX II devices are available in space-saving FineLine BGA, Micro FineLine BGA, and thin quad flat pack (TQFP) packages (refer to Table 1–3 and Table 1–4). MAX II devices support vertical migration within the same package (for example, you can migrate between the EPM570, EPM1270, and EPM2210 devices in the 256-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins and JTAG pins are the same and power pins are subsets or supersets for a given package across device densities. The largest density in any package has the highest number of power pins; you must lay out for the largest planned density in a package to provide the necessary power pins for migration. For I/O pin migration across densities, cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins can be migrated. The Quartus® II software can automatically cross-reference and place all pins for you when given a device migration list.

Table 1–3. MAX II Packages and User I/O Pins

Device	68-Pin Micro FineLine BGA (1)	100-Pin Micro FineLine BGA (1)	100-Pin FineLine BGA	100-Pin TQFP	144-Pin TQFP	144-Pin Micro FineLine BGA (1)	256-Pin Micro FineLine BGA (1)	256-Pin FineLine BGA	324-Pin FineLine BGA
EPM240 EPM240G	—	80	80	80	—	—	—	—	—
EPM570 EPM570G	—	76	76	76	116	—	160	160	—
EPM1270 EPM1270G	—	—	—	—	116	—	212	212	—
EPM2210 EPM2210G	—	—	—	—	—	—	—	204	272
EPM240Z	54	80	—	—	—	—	—	—	—
EPM570Z	—	76	—	—	—	116	160	—	—

Note to Table 1–3:

(1) Packages available in lead-free versions only.

Table 1–4. MAX II TQFP, FineLine BGA, and Micro FineLine BGA Package Sizes

Package	68-Pin Micro FineLine BGA	100-Pin Micro FineLine BGA	100-Pin FineLine BGA	100-Pin TQFP	144-Pin TQFP	144-Pin Micro FineLine BGA	256-Pin Micro FineLine BGA	256-Pin FineLine BGA	324-Pin FineLine BGA
Pitch (mm)	0.5	0.5	1	0.5	0.5	0.5	0.5	1	1
Area (mm ²)	25	36	121	256	484	49	121	289	361
Length × width (mm × mm)	5 × 5	6 × 6	11 × 11	16 × 16	22 × 22	7 × 7	11 × 11	17 × 17	19 × 19

LUT Chain and Register Chain

In addition to the three general routing outputs, the LEs within an LAB have LUT chain and register chain outputs. LUT chain connections allow LUTs within the same LAB to cascade together for wide input functions. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows an LAB to use LUTs for a single combinational function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. Refer to “MultiTrack Interconnect” on page 2-12 for more information about LUT chain and register chain connections.

addnsub Signal

The LE's dynamic adder/subtractor feature saves logic resources by using one set of LEs to implement both an adder and a subtractor. This feature is controlled by the LAB-wide control signal `addnsub`. The `addnsub` signal sets the LAB to perform either $A + B$ or $A - B$. The LUT computes addition; subtraction is computed by adding the two's complement of the intended subtractor. The LAB-wide signal converts to two's complement by inverting the B bits within the LAB and setting carry-in to 1, which adds one to the least significant bit (LSB). The LSB of an adder/subtractor must be placed in the first LE of the LAB, where the LAB-wide `addnsub` signal automatically sets the carry-in to 1. The Quartus II Compiler automatically places and uses the adder/subtractor feature when using adder/subtractor parameterized functions.

LE Operating Modes

The MAX II LE can operate in one of the following modes:

- “Normal Mode”
- “Dynamic Arithmetic Mode”

Each mode uses LE resources differently. In each mode, eight available inputs to the LE, the four data inputs from the LAB local interconnect, `carry-in0` and `carry-in1` from the previous LE, the LAB carry-in from the previous carry-chain LAB, and the register chain connection are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset/load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes. The `addnsub` control signal is allowed in arithmetic mode.

The Quartus II software, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions.

Internal Oscillator

As shown in Figure 2–15, the dedicated circuitry within the UFM block contains an oscillator. The dedicated circuitry uses this internally for its read and program operations. This oscillator's divide by 4 output can drive out of the UFM block as a logic interface clock source or for general-purpose logic clocking. The typical OSC output signal frequency ranges from 3.3 to 5.5 MHz, and its exact frequency of operation is not programmable.

Program, Erase, and Busy Signals

The UFM block's dedicated circuitry automatically generates the necessary internal program and erase algorithm once the PROGRAM or ERASE input signals have been asserted. The PROGRAM or ERASE signal must be asserted until the busy signal deasserts, indicating the UFM internal program or erase operation has completed. The UFM block also supports JTAG as the interface for programming and/or reading.



For more information about programming and erasing the UFM block, refer to the *Using User Flash Memory in MAX II Devices* chapter in the *MAX II Device Handbook*.

Auto-Increment Addressing

The UFM block supports standard read or stream read operations. The stream read is supported with an auto-increment address feature. Deasserting the ARSHIFT signal while clocking the ARCLK signal increments the address register value to read consecutive locations from the UFM array.

Serial Interface

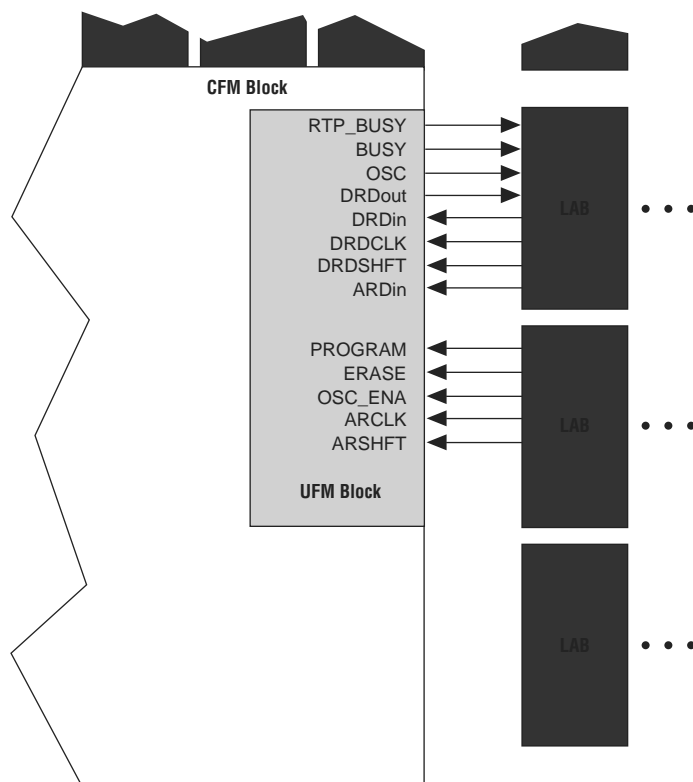
The UFM block supports a serial interface with serial address and data signals. The internal shift registers within the UFM block for address and data are 9 bits and 16 bits wide, respectively. The Quartus II software automatically generates interface logic in LEs for a parallel address and data interface to the UFM block. Other standard protocol interfaces such as SPI are also automatically generated in LE logic by the Quartus II software.



For more information about the UFM interface signals and the Quartus II LE-based alternate interfaces, refer to the *Using User Flash Memory in MAX II Devices* chapter in the *MAX II Device Handbook*.

UFM Block to Logic Array Interface

The UFM block is a small partition of the flash memory that contains the CFM block, as shown in Figure 2–1 and Figure 2–2. The UFM block for the EPM240 device is located on the left side of the device adjacent to the left most LAB column. The UFM block for the EPM570, EPM1270, and EPM2210 devices is located at the bottom left of the device. The UFM input and output signals interface to all types of interconnects (R4 interconnect, C4 interconnect, and DirectLink interconnect to/from adjacent LAB rows). The UFM signals can also be driven from global clocks, GCLK[3..0]. The interface region for the EPM240 device is shown in Figure 2–16. The interface regions for EPM570, EPM1270, and EPM2210 devices are shown in Figure 2–17.

Figure 2-17. EPM570, EPM1270, and EPM2210 UFM Block LAB Row Interface

MultiVolt Core

The MAX II architecture supports the MultiVolt core feature, which allows MAX II devices to support multiple V_{CC} levels on the V_{CCINT} supply. An internal linear voltage regulator provides the necessary 1.8-V internal voltage supply to the device. The voltage regulator supports 3.3-V or 2.5-V supplies on its inputs to supply the 1.8-V internal voltage to the device, as shown in Figure 2-18. The voltage regulator is not guaranteed for voltages that are between the maximum recommended 2.5-V operating voltage and the minimum recommended 3.3-V operating voltage.

The MAX IIG and MAX IIZ devices use external 1.8-V supply. The 1.8-V V_{CC} external supply powers the device core directly.

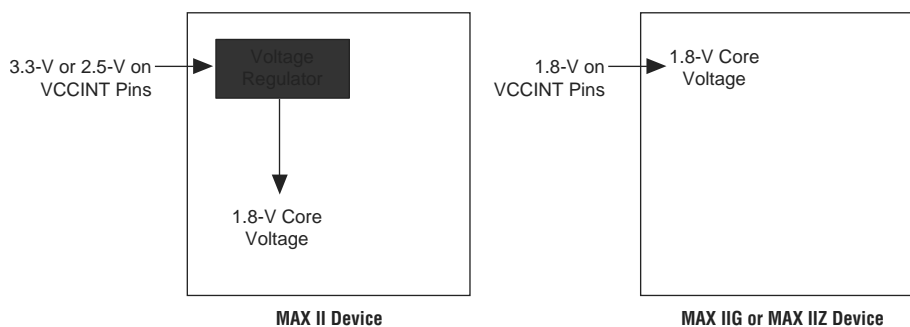
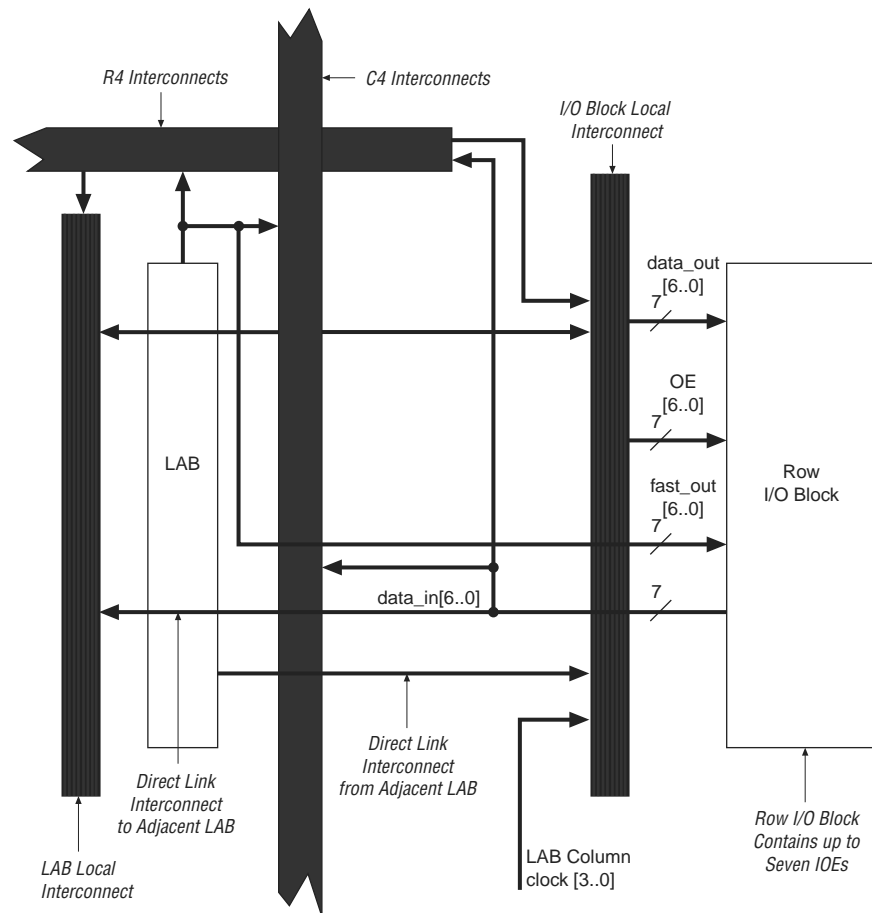
Figure 2-18. MultiVolt Core Feature in MAX II Devices

Figure 2-20 shows how a row I/O block connects to the logic array.

Figure 2-20. Row I/O Block Connection to the Interconnect (*Note 1*)

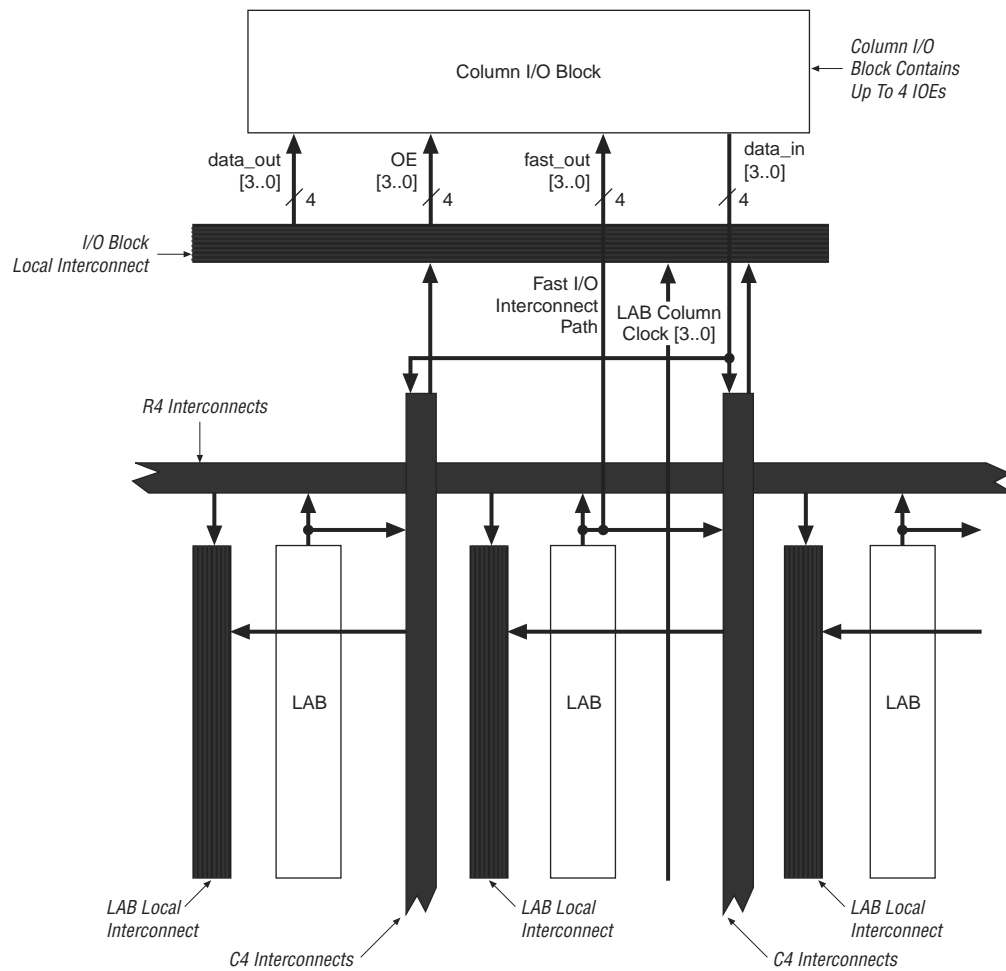


Note to Figure 2-20:

- (1) Each of the seven IOEs in the row I/O block can have one **data_out** or **fast_out** output, one **OE** output, and one **data_in** input.

Figure 2-21 shows how a column I/O block connects to the logic array.

Figure 2-21. Column I/O Block Connection to the Interconnect (*Note 1*)



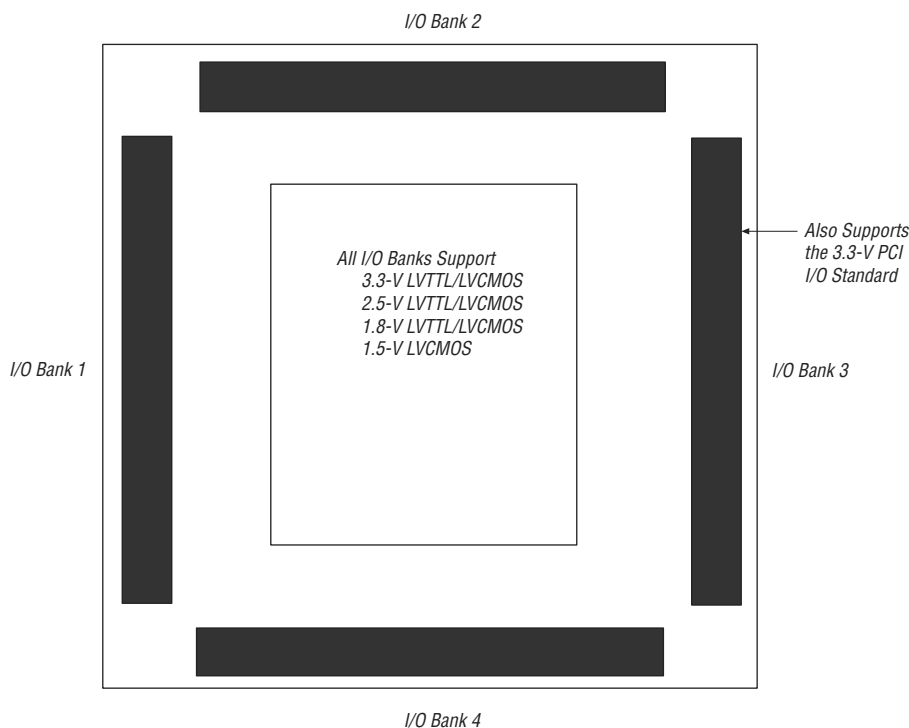
Note to Figure 2-21:

(1) Each of the four IOEs in the column I/O block can have one `data_out` or `fast_out` output, one `OE` output, and one `data_in` input.

I/O Standards and Banks

MAX II device IOEs support the following I/O standards:

- 3.3-V LVTTTL/LVCMOS
- 2.5-V LVTTTL/LVCMOS
- 1.8-V LVTTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI

Figure 2-23. MAX II I/O Banks for EPM1270 and EPM2210 (Note 1), (2)**Notes to Figure 2-23:**

- (1) Figure 2-23 is a top view of the silicon die.
- (2) Figure 2-23 is a graphical representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Each I/O bank has dedicated V_{CCIO} pins that determine the voltage standard support in that bank. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each individual bank can support a different standard. Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3 V, Bank 3 can support LVTTTL, LVCMOS, and 3.3-V PCI. V_{CCIO} powers both the input and output buffers in MAX II devices.

The JTAG pins for MAX II devices are dedicated pins that cannot be used as regular I/O pins. The pins TMS, TDI, TDO, and TCK support all the I/O standards shown in Table 2-4 on page 2-27 except for PCI. These pins reside in Bank 1 for all MAX II devices and their I/O standard support is controlled by the V_{CCIO} setting for Bank 1.

PCI Compliance

The MAX II EPM1270 and EPM2210 devices are compliant with PCI applications as well as all 3.3-V electrical specifications in the *PCI Local Bus Specification Revision 2.2*. These devices are also large enough to support PCI intellectual property (IP) cores. Table 2-5 shows the MAX II device speed grades that meet the PCI timing specifications.

Table 2-6. Programmable Drive Strength (*Note 1*)

I/O Standard	IOH/IOL Current Strength Setting (mA)
3.3-V LVTTTL	16
	8
3.3-V LVCMOS	8
	4
2.5-V LVTTTL/LVCMOS	14
	7
1.8-V LVTTTL/LVCMOS	6
	3
1.5-V LVCMOS	4
	2

Note to Table 2-6:

- (1) The I_{OH} current strength numbers shown are for a condition of a $V_{OUT} = V_{OH}$ minimum, where the V_{OH} minimum is specified by the I/O standard. The I_{OL} current strength numbers shown are for a condition of a $V_{OUT} = V_{OL}$ maximum, where the V_{OL} maximum is specified by the I/O standard. For 2.5-V LVTTTL/LVCMOS, the I_{OH} condition is $V_{OUT} = 1.7$ V and the I_{OL} condition is $V_{OUT} = 0.7$ V.

Slew-Rate Control

The output buffer for each MAX II device I/O pin has a programmable output slew-rate control that can be configured for low noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal output delay to rising and falling edges. The lower the voltage standard (for example, 1.8-V LVTTTL) the larger the output delay when slow slew is enabled. Each I/O pin has an individual slew-rate control, allowing the designer to specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges.

Open-Drain Output

MAX II devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that can be asserted by any of several devices. This output can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX II devices can be used as an additional ground pin. This programmable ground feature does not require the use of the associated LEs in the device. In the Quartus II software, unused pins can be set as programmable GND on a global default basis or they can be individually assigned. Unused pins also have the option of being set as tri-stated input pins.

3. JTAG and In-System Programmability

MII51003-1.6

Introduction

This chapter discusses how to use the IEEE Standard 1149.1 Boundary-Scan Test (BST) circuitry in MAX II devices and includes the following sections:

- “IEEE Std. 1149.1 (JTAG) Boundary-Scan Support” on page 3–1
- “In System Programmability” on page 3–4

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All MAX® II devices provide Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry that complies with the IEEE Std. 1149.1-2001 specification. JTAG boundary-scan testing can only be performed at any time after V_{CCINT} and all V_{CCIO} banks have been fully powered and a t_{CONFIG} amount of time has passed. MAX II devices can also use the JTAG port for in-system programming together with either the Quartus® II software or hardware using Programming Object Files (.pof), Jam™ Standard Test and Programming Language (STAPL) Files (.jam), or Jam Byte-Code Files (.jbc).

The JTAG pins support 1.5-V, 1.8-V, 2.5-V, or 3.3-V I/O standards. The supported voltage level and standard are determined by the V_{CCIO} of the bank where it resides. The dedicated JTAG pins reside in Bank 1 of all MAX II devices.

MAX II devices support the JTAG instructions shown in Table 3–1.

Table 3–1. MAX II JTAG Instructions (Part 1 of 2)

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
EXTEST (1)	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO. This register defaults to all 1's if not specified in the Quartus II software.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ (1)	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the boundary scan test data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.

4. Hot Socketing and Power-On Reset in MAX II Devices

MII51004-2.1

Introduction

MAX® II devices offer hot socketing, also known as hot plug-in or hot swap, and power sequencing support. Designers can insert or remove a MAX II board in a system during operation without undesirable effects to the system bus. The hot socketing feature removes some of the difficulties designers face when using components on printed circuit boards (PCBs) that contain a mixture of 3.3-, 2.5-, 1.8-, and 1.5-V devices.

The MAX II device hot socketing feature provides:

- Board or device insertion and removal
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter contains the following sections:

- “MAX II Hot-Socketing Specifications” on page 4-1
- “Power-On Reset Circuitry” on page 4-5

MAX II Hot-Socketing Specifications

MAX II devices offer all three of the features required for the hot-socketing capability listed above without any external components or special design requirements. The following are hot-socketing specifications:


- The device can be driven before and during power-up or power-down without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.
- Signal pins do not drive the V_{CCIO} or V_{CCINT} power supplies. External input signals to device I/O pins do not power the device V_{CCIO} or V_{CCINT} power supplies via internal paths. This is true if the V_{CCINT} and the V_{CCIO} supplies are held at GND.



Altera uses GND as reference for the hot-socketing and I/O buffers circuitry designs. You must connect the GND between boards before connecting the V_{CCINT} and the V_{CCIO} power supplies to ensure device reliability and compliance to the hot-socketing specifications.

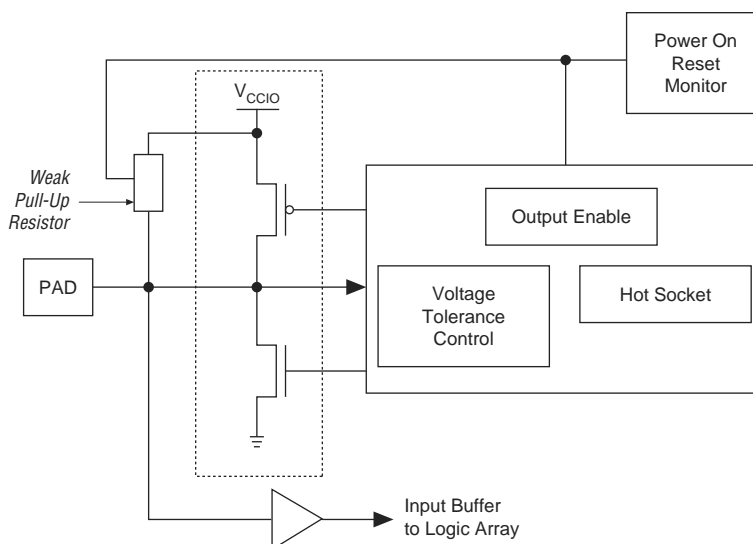
Devices Can Be Driven before Power-Up

Signals can be driven into the MAX II device I/O pins and $GCLK[3..0]$ pins before or during power-up or power-down without damaging the device. MAX II devices support any power-up or power-down sequence (V_{CCIO1} , V_{CCIO2} , V_{CCIO3} , V_{CCIO4} , V_{CCINT}), simplifying the system-level design.

 Make sure that the V_{CCINT} is within the recommended operating range even though SRAM download has completed.

Each I/O and clock pin has the circuitry shown in Figure 4-1.

Figure 4-1. Hot Socketing Circuit Block Diagram for MAX II Devices



The POR circuit monitors V_{CCINT} and V_{CCIO} voltage levels and keeps I/O pins tri-stated until the device has completed its flash memory configuration of the SRAM logic. The weak pull-up resistor (R) from the I/O pin to V_{CCIO} is enabled during download to keep the I/O pins from floating. The 3.3-V tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO} and/or V_{CCINT} are powered, and it prevents the I/O pins from driving out when the device is not fully powered or operational. The hot socket circuit prevents I/O pins from internally powering V_{CCIO} and V_{CCINT} when driven by external signals before the device is powered.


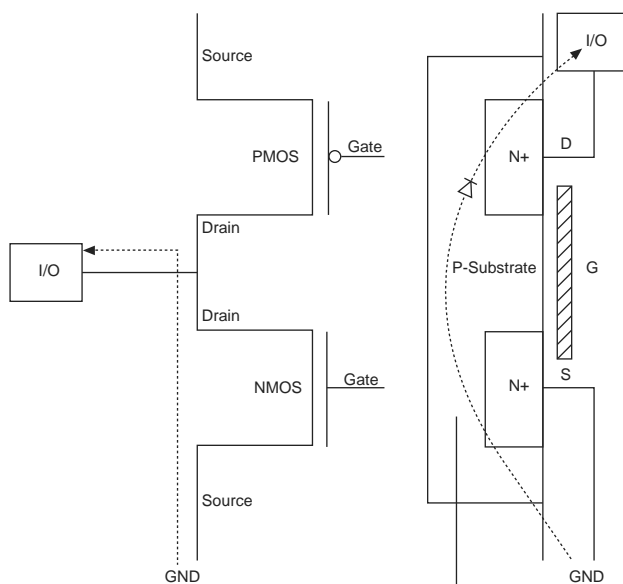
 For information about 5.0-V tolerance, refer to the *Using MAX II Devices in Multi-Voltage Systems* chapter in the *MAX II Device Handbook*.

Figure 4-2 shows a transistor-level cross section of the MAX II device I/O buffers. This design ensures that the output buffers do not drive when V_{CCIO} is powered before V_{CCINT} or if the I/O pad voltage is higher than V_{CCIO} . This also applies for sudden voltage spikes during hot insertion. The V_{PAD} leakage current charges the 3.3-V tolerant circuit capacitance.

When the I/O pin receives a negative ESD zap at the pin that is less than -0.7 V (0.7 V is the voltage drop across a diode), the intrinsic P-Substrate/N+ drain diode is forward biased. Therefore, the discharge ESD current path is from GND to the I/O pin, as shown in Figure 4-4.

Figure 4-4. ESD Protection During Negative Voltage Zap



Power-On Reset Circuitry

MAX II devices have POR circuits to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up. The POR circuit monitors these voltages, triggering download from the non-volatile configuration flash memory (CFM) block to the SRAM logic, maintaining tri-state of the I/O pins (with weak pull-up resistors enabled) before and during this process. When the MAX II device enters user mode, the POR circuit releases the I/O pins to user functionality. The POR circuit of the MAX II (except MAX IIZ) device continues to monitor the V_{CCINT} voltage level to detect a brown-out condition. The POR circuit of the MAX IIZ device does not monitor the V_{CCINT} voltage level after the device enters into user mode. More details are provided in the following sub-sections.

Referenced Documents

This chapter references the following documents:

- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *Using MAX II Devices in Multi-Voltage Systems* chapter in the *MAX II Device Handbook*

Document Revision History

Table 4–1 shows the revision history for this chapter.

Table 4–1. Document Revision History

Date and Revision	Changes Made	Summary of Changes
October 2008, version 2.1	<ul style="list-style-type: none"> ■ Updated “MAX II Hot-Socketing Specifications” and “Power-On Reset Circuitry” sections. ■ Updated New Document Format. 	—
December 2007, version 2.0	<ul style="list-style-type: none"> ■ Updated “Hot Socketing Feature Implementation in MAX II Devices” section. ■ Updated “Power-On Reset Circuitry” section. ■ Updated Figure 4–5. ■ Added “Referenced Documents” section. 	Updated document with MAX IIZ information.
December 2006, version 1.5	<ul style="list-style-type: none"> ■ Added document revision history. 	—
February 2006, version 1.4	<ul style="list-style-type: none"> ■ Updated “MAX II Hot-Socketing Specifications” section. ■ Updated “AC and DC Specifications” section. ■ Updated “Power-On Reset Circuitry” section. 	—
June 2005, version 1.3	<ul style="list-style-type: none"> ■ Updated AC and DC specifications on page 4-2. 	—
December 2004, version 1.2	<ul style="list-style-type: none"> ■ Added content to Power-Up Characteristics section. ■ Updated Figure 4-5. 	—
June 2004, version 1.1	<ul style="list-style-type: none"> ■ Corrected Figure 4-2. 	—

Table 5-4. MAX II Device DC Electrical Characteristics (Note 1) (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{PULLUP}	I/O pin pull-up resistor current when I/O is unprogrammed	—	—	—	300	μA
C_{IO}	Input capacitance for user I/O pin	—	—	—	8	pF
C_{GCLK}	Input capacitance for dual-purpose GCLK/user I/O pin	—	—	—	8	pF

Notes to Table 5-4:

- (1) Typical values are for $T_A = 25^\circ C$, $V_{CCINT} = 3.3$ or 2.5 V, and $V_{CCIO} = 1.5$ V, 1.8 V, 2.5 V, or 3.3 V.
- (2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3 , 2.5 , 1.8 , and 1.5 V).
- (3) $V_I =$ ground, no load, no toggling inputs.
- (4) Commercial temperature ranges from $0^\circ C$ to $85^\circ C$ with maximum current at $85^\circ C$.
- (5) Industrial temperature ranges from $-40^\circ C$ to $100^\circ C$ with maximum current at $100^\circ C$.
- (6) This value applies to commercial and industrial range devices. For extended temperature range devices, the $V_{SCHMITT}$ typical value is 300 mV for $V_{CCIO} = 3.3$ V and 120 mV for $V_{CCIO} = 2.5$ V.
- (7) The TCK input is susceptible to high pulse glitches when the input signal fall time is greater than 200 ns for all I/O standards.
- (8) This is a peak current value with a maximum duration of t_{CONFIG} time.
- (9) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO} .

Table 5-17. t_{ZX} IOE Microparameter Adders for Fast Slew Rate (Part 2 of 2)

Standard		MAX II / MAX IIG						MAX IIZ						Unit
		−3 Speed Grade		−4 Speed Grade		−5 Speed Grade		−6 Speed Grade		−7 Speed Grade		−8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
1.5-V LVCMOS	4 mA	—	1,118	—	1,454	—	1,789	—	580	—	588	—	588	ps
	2 mA	—	2,410	—	3,133	—	3,856	—	915	—	923	—	923	ps
3.3-V PCI	20 mA	—	19	—	25	—	31	—	72	—	71	—	74	ps

Table 5-18. t_{ZX} IOE Microparameter Adders for Slow Slew Rate

Standard		MAX II / MAX IIG						MAX IIZ						Unit
		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	16 mA	—	6,350	—	6,050	—	5,749	—	5,951	—	5,952	—	6,063	ps
	8 mA	—	9,383	—	9,083	—	8,782	—	6,534	—	6,533	—	6,662	ps
3.3-V LVCMOS	8 mA	—	6,350	—	6,050	—	5,749	—	5,951	—	5,952	—	6,063	ps
	4 mA	—	9,383	—	9,083	—	8,782	—	6,534	—	6,533	—	6,662	ps
2.5-V LVTTTL / LVCMOS	14 mA	—	10,412	—	10,112	—	9,811	—	9,110	—	9,105	—	9,237	ps
	7 mA	—	13,613	—	13,313	—	13,012	—	9,830	—	9,835	—	9,977	ps
3.3-V PCI	20 mA	—	-75	—	-97	—	-120	—	6,534	—	6,533	—	6,662	ps

Table 5-19. t_{XZ} IOE Microparameter Adders for Fast Slew Rate

Standard		MAX II / MAX IIG						MAX IIZ						Unit
		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	16 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	8 mA	—	-56	—	-72	—	-89	—	-69	—	-69	—	-69	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	4 mA	—	-56	—	-72	—	-89	—	-69	—	-69	—	-69	ps
2.5-V LVTTTL / LVCMOS	14 mA	—	-3	—	-4	—	-5	—	-7	—	-11	—	-11	ps
	7 mA	—	-47	—	-61	—	-75	—	-66	—	-70	—	-70	ps
1.8-V LVTTTL / LVCMOS	6 mA	—	119	—	155	—	191	—	45	—	34	—	37	ps
	3 mA	—	207	—	269	—	331	—	34	—	22	—	25	ps
1.5-V LVCMOS	4 mA	—	606	—	788	—	970	—	166	—	154	—	155	ps
	2 mA	—	673	—	875	—	1,077	—	190	—	177	—	179	ps
3.3-V PCI	20 mA	—	71	—	93	—	114	—	-69	—	-69	—	-69	ps

Table 5-23. EPM240 Global Clock External I/O Timing Parameters (Part 2 of 2)

Symbol	Parameter	Condition	MAX II / MAX IIG						MAX IIZ						Unit
			−3 Speed Grade		−4 Speed Grade		−5 Speed Grade		−6 Speed Grade		−7 Speed Grade		−8 Speed Grade		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f _{CNT}	Maximum global clock frequency for 16-bit counter	—	—	304.0 (1)	—	247.5	—	201.1	—	184.1	—	123.5	—	118.3	MHz

Note to Table 5-23:

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5-24 shows the external I/O timing parameters for EPM570 devices.

Table 5-24. EPM570 Global Clock External I/O Timing Parameters (Part 1 of 2)

Symbol	Parameter	Condition	MAX II / MAX IIG						MAX IIZ						Unit
			-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{PD1}	Worst case pin-to-pin delay through 1 look-up table (LUT)	10 pF	—	5.4	—	7.0	—	8.7	—	9.5	—	15.1	—	17.7	ns
t _{PD2}	Best case pin-to-pin delay through 1 LUT	10 pF	—	3.7	—	4.8	—	5.9	—	5.7	—	7.7	—	8.5	ns
t _{SU}	Global clock setup time	—	1.2	—	1.5	—	1.9	—	2.2	—	3.9	—	4.4	—	ns
t _H	Global clock hold time	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t _{CO}	Global clock to output delay	10 pF	2.0	4.5	2.0	5.8	2.0	7.1	2.0	6.7	2.0	8.2	2.0	8.7	ns
t _{CH}	Global clock high time	—	166	—	216	—	266	—	253	—	335	—	339	—	ps
t _{CL}	Global clock low time	—	166	—	216	—	266	—	253	—	335	—	339	—	ps
t _{CNT}	Minimum global clock period for 16-bit counter	—	3.3	—	4.0	—	5.0	—	5.4	—	8.1	—	8.4	—	ns

Table 5–26 shows the external I/O timing parameters for EPM2210 devices.

Table 5–26. EPM2210 Global Clock External I/O Timing Parameters

Symbol	Parameter	Condition	MAX II / MAX IIG						Unit
			–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Worst case pin-to-pin delay through 1 look-up table (LUT)	10 pF	—	7.0	—	9.1	—	11.2	ns
t _{PD2}	Best case pin-to-pin delay through 1 LUT	10 pF	—	3.7	—	4.8	—	5.9	ns
t _{SU}	Global clock setup time	—	1.2	—	1.5	—	1.9	—	ns
t _H	Global clock hold time	—	0	—	0	—	0	—	ns
t _{CO}	Global clock to output delay	10 pF	2.0	4.6	2.0	6.0	2.0	7.4	ns
t _{CH}	Global clock high time	—	166	—	216	—	266	—	ps
t _{CL}	Global clock low time	—	166	—	216	—	266	—	ps
t _{CNT}	Minimum global clock period for 16-bit counter	—	3.3	—	4.0	—	5.0	—	ns
f _{CNT}	Maximum global clock frequency for 16-bit counter	—	—	304.0 (1)	—	247.5	—	201.1	MHz

Note to Table 5–26:

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

External Timing I/O Delay Adders

The I/O delay timing parameters for I/O standard input and output adders, and input delays are specified by speed grade independent of device density.

Table 5–27 through Table 5–31 show the adder delays associated with I/O pins for all packages. The delay numbers for –3, –4, and –5 speed grades shown in Table 5–27 through Table 5–33 are based on an EPM1270 device target, while –6, –7, and –8 speed grade values are based on an EPM570Z device target. If an I/O standard other than 3.3-V LVTTTL is selected, add the input delay adder to the external t_{SU} timing parameters shown in Table 5–23 through Table 5–26. If an I/O standard other than 3.3-V LVTTTL with 16 mA drive strength and fast slew rate is selected, add the output delay adder to the external t_{CO} and t_{PD} shown in Table 5–23 through Table 5–26.

Table 5–27. External Timing Input Delay Adders (Part 1 of 2)

I/O Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LV TTL	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	334	—	434	—	535	—	387	—	434	—	442	ps

Table 5-34. MAX II JTAG Timing Parameters (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{JPSU}	JTAG port setup time (2)	8	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output (2)	—	15	ns
t_{JPZX}	JTAG port high impedance to valid output (2)	—	15	ns
t_{JPXZ}	JTAG port valid output to high impedance (2)	—	15	ns
t_{JSU}	Capture register setup time	8	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Notes to Table 5-34:

- (1) Minimum clock period specified for 10 pF load on the TDO pin. Larger loads on TDO will degrade the maximum TCK frequency.
- (2) This specification is shown for 3.3-V LVTTTL/LVCMOS and 2.5-V LVTTTL/LVCMOS operation of the JTAG pins. For 1.8-V LVTTTL/LVCMOS and 1.5-V LVCMOS, the t_{JPSU} minimum is 6 ns and t_{JPCO} , t_{JPZX} , and t_{JPXZ} are maximum values at 35 ns.

Referenced Documents

This chapter references the following documents:

- *I/O Structure* section in the *MAX II Architecture* chapter in the *MAX II Device Handbook*
- *Hot Socketing and Power-On Reset in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Operating Requirements for Altera Devices Data Sheet*
- *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*
- *Understanding and Evaluating Power in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Understanding Timing in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Using MAX II Devices in Multi-Voltage Systems* chapter in the *MAX II Device Handbook*

Document Revision History

Table 5–35 shows the revision history for this chapter.

Table 5–35. Document Revision History (Part 1 of 2)

Date and Revision	Changes Made	Summary of Changes
August 2009, version 2.5	<ul style="list-style-type: none"> ■ Added Table 5–28, Table 5–29, and Table 5–30. ■ Updated Table 5–2, Table 5–4, Table 5–14, Table 5–15, Table 5–16, Table 5–17, Table 5–18, Table 5–19, Table 5–20, Table 5–21, Table 5–22, Table 5–23, Table 5–24, Table 5–27, Table 5–31, Table 5–32, and Table 5–33. 	Added information for speed grade –8
November 2008, version 2.4	<ul style="list-style-type: none"> ■ Updated Table 5–2. ■ Updated “Internal Timing Parameters” section. 	—
October 2008, version 2.3	<ul style="list-style-type: none"> ■ Updated New Document Format. ■ Updated Figure 5–1. 	—
July 2008, version 2.2	<ul style="list-style-type: none"> ■ Updated Table 5–14, Table 5–23, and Table 5–24. 	—
March 2008, version 2.1	<ul style="list-style-type: none"> ■ Added (Note 5) to Table 5–4. 	—
December 2007, version 2.0	<ul style="list-style-type: none"> ■ Updated (Note 3) and (4) to Table 5–1. ■ Updated Table 5–2 and added (Note 5). ■ Updated ICCSTANDBY and ICCPOWERUP information and added IPULLUP information in Table 5–4. ■ Added (Note 1) to Table 5–10. ■ Updated Figure 5–2. ■ Added (Note 1) to Table 5–13. ■ Updated Table 5–13 through Table 5–24, and Table 5–27 through Table 5–30. ■ Added tCOMB information to Table 5–15. ■ Updated Figure 5–6. ■ Added “Referenced Documents” section. 	Updated document with MAX IIZ information.
December 2006, version 1.8	<ul style="list-style-type: none"> ■ Added note to Table 5–1. ■ Added document revision history. 	—
July 2006, version 1.7	<ul style="list-style-type: none"> ■ Minor content and table updates. 	—
February 2006, version 1.6	<ul style="list-style-type: none"> ■ Updated “External Timing I/O Delay Adders” section. ■ Updated Table 5–29. ■ Updated Table 5–30. 	—
November 2005, version 1.5	<ul style="list-style-type: none"> ■ Updated Tables 5–2, 5–4, and 5–12. 	—
August 2005, version 1.4	<ul style="list-style-type: none"> ■ Updated Figure 5–1. ■ Updated Tables 5–13, 5–16, and 5–26. ■ Removed Note 1 from Table 5–12. 	—

Table 5-35. Document Revision History (Part 2 of 2)

Date and Revision	Changes Made	Summary of Changes
June 2005, version 1.3	<ul style="list-style-type: none"> ■ Updated the R_{PULLUP} parameter in Table 5-4. ■ Added Note 2 to Tables 5-8 and 5-9. ■ Updated Table 5-13. ■ Added “Output Drive Characteristics” section. ■ Added I²C mode and Notes 5 and 6 to Table 5-14. ■ Updated timing values to Tables 5-14 through 5-33. 	—
December 2004, version 1.2	<ul style="list-style-type: none"> ■ Updated timing Tables 5-2, 5-4, 5-12, and Tables 15-14 through 5-34. ■ Table 5-31 is new. 	—
June 2004, version 1.1	<ul style="list-style-type: none"> ■ Updated timing Tables 5-15 through 5-32. 	—