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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.4 ns
Voltage Supply - Internal	2.5V, 3.3V
Number of Logic Elements/Blocks	570
Number of Macrocells	440
Number of Gates	-
Number of I/O	76
Operating Temperature	-40°C ~ 125°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-LBGA
Supplier Device Package	100-FBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm570f100a5n

1. Introduction

MII51001-1.9

Introduction

The MAX® II family of instant-on, non-volatile CPLDs is based on a 0.18-µm, 6-layer-metal-flash process, with densities from 240 to 2,210 logic elements (LEs) (128 to 2,210 equivalent macrocells) and non-volatile storage of 8 Kbits. MAX II devices offer high I/O counts, fast performance, and reliable fitting versus other CPLD architectures. Featuring MultiVolt core, a user flash memory (UFM) block, and enhanced in-system programmability (ISP), MAX II devices are designed to reduce cost and power while providing programmable solutions for applications such as bus bridging, I/O expansion, power-on reset (POR) and sequencing control, and device configuration control.

Features

The MAX II CPLD has the following features:

- Low-cost, low-power CPLD
- Instant-on, non-volatile architecture
- Standby current as low as 25 µA
- Provides fast propagation delay and clock-to-output times
- Provides four global clocks with two clocks available per logic array block (LAB)
- UFM block up to 8 Kbits for non-volatile storage
- MultiVolt core enabling external supply voltages to the device of either 3.3 V/2.5 V or 1.8 V
- MultiVolt I/O interface supporting 3.3-V, 2.5-V, 1.8-V, and 1.5-V logic levels
- Bus-friendly architecture including programmable slew rate, drive strength, bus-hold, and programmable pull-up resistors
- Schmitt triggers enabling noise tolerant inputs (programmable per pin)
- I/Os are fully compliant with the Peripheral Component Interconnect Special Interest Group (PCI SIG) PCI Local Bus Specification, Revision 2.2 for 3.3-V operation at 66 MHz
- Supports hot-socketing
- Built-in Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry compliant with IEEE Std. 1149.1-1990
- ISP circuitry compliant with IEEE Std. 1532

Table 1–6. Document Revision History

Date and Revision	Changes Made	Summary of Changes
June 2005, version 1.3	■ Updated timing numbers in Table 1-1.	—
December 2004, version 1.2	■ Updated timing numbers in Table 1-1.	—
June 2004, version 1.1	■ Updated timing numbers in Table 1-1.	—

2. MAX II Architecture

MII51002-2.2

Introduction

This chapter describes the architecture of the MAX II device and contains the following sections:

Functional Description

MAX® II devices contain a two-dimensional row- and column-based architecture to implement custom logic. Row and column interconnects provide signal interconnects between the logic array blocks (LABs).

The logic array consists of LABs, with 10 logic elements (LEs) in each LAB. An LE is a small unit of logic providing efficient implementation of user logic functions. LABs are grouped into rows and columns across the device. The MultiTrack interconnect provides fast granular timing delays between LABs. The fast routing between LEs provides minimum timing delay for added levels of logic versus globally routed interconnect structures.

The MAX II device I/O pins are fed by I/O elements (IOE) located at the ends of LAB rows and columns around the periphery of the device. Each IOE contains a bidirectional I/O buffer with several advanced features. I/O pins support Schmitt trigger inputs and various single-ended standards, such as 66-MHz, 32-bit PCI, and LVTTL.

MAX II devices provide a global clock network. The global clock network consists of four global clock lines that drive throughout the entire device, providing clocks for all resources within the device. The global clock lines can also be used for control signals such as clear, preset, or output enable.

LUT Chain and Register Chain

In addition to the three general routing outputs, the LEs within an LAB have LUT chain and register chain outputs. LUT chain connections allow LUTs within the same LAB to cascade together for wide input functions. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows an LAB to use LUTs for a single combinational function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. Refer to "MultiTrack Interconnect" on page 2–12 for more information about LUT chain and register chain connections.

addnsub Signal

The LE's dynamic adder/subtractor feature saves logic resources by using one set of LEs to implement both an adder and a subtractor. This feature is controlled by the LAB-wide control signal addnsub. The addnsub signal sets the LAB to perform either A + B or A – B. The LUT computes addition; subtraction is computed by adding the two's complement of the intended subtractor. The LAB-wide signal converts to two's complement by inverting the B bits within the LAB and setting carry-in to 1, which adds one to the least significant bit (LSB). The LSB of an adder/subtractor must be placed in the first LE of the LAB, where the LAB-wide addnsub signal automatically sets the carry-in to 1. The Quartus II Compiler automatically places and uses the adder/subtractor feature when using adder/subtractor parameterized functions.

LE Operating Modes

The MAX II LE can operate in one of the following modes:

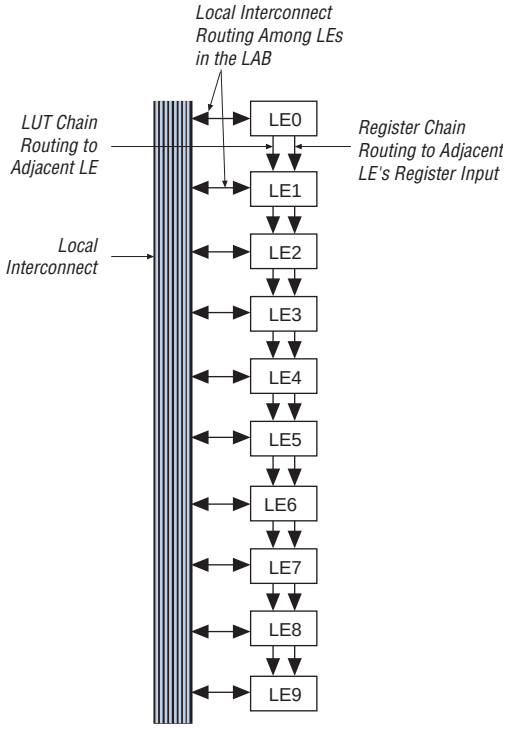
- "Normal Mode"
- "Dynamic Arithmetic Mode"

Each mode uses LE resources differently. In each mode, eight available inputs to the LE, the four data inputs from the LAB local interconnect, `carry-in0` and `carry-in1` from the previous LE, the LAB carry-in from the previous carry-chain LAB, and the register chain connection are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset/load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes. The addnsub control signal is allowed in arithmetic mode.

The Quartus II software, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions.

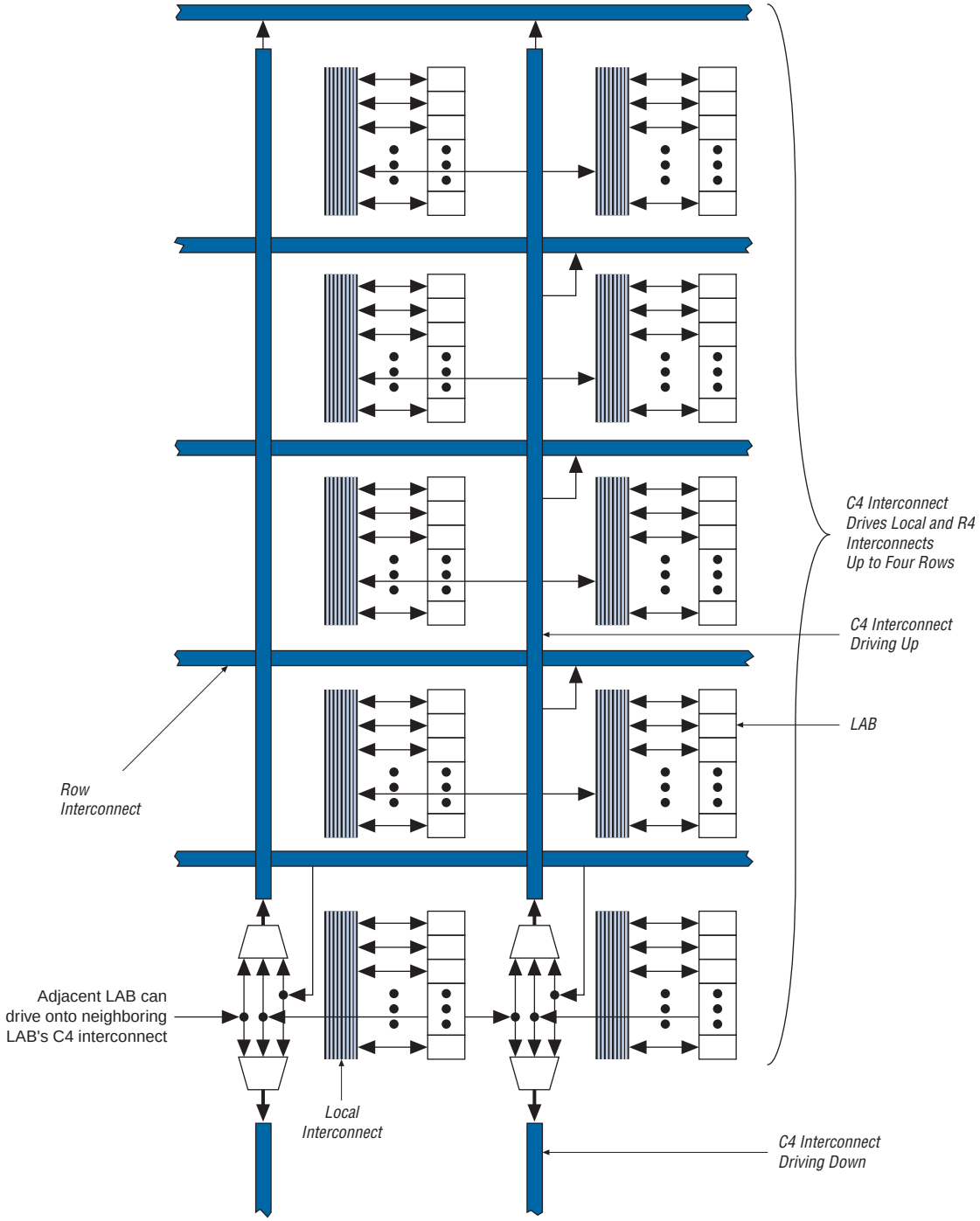
functions from LE 1 to LE 10 in the same LAB. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–11 shows the LUT chain and register chain interconnects.

Figure 2–11. LUT Chain and Register Chain Interconnects



The C4 interconnects span four LABs up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–12 shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by column and row IOEs. For LAB interconnection, a primary LAB or its vertical LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Figure 2–12. C4 Interconnect Connections *(Note 1)*



Note to Figure 2–12:

(1) Each C4 interconnect can drive either up or down four rows.

The UFM block communicates with the logic array similar to LAB-to-LAB interfaces. The UFM block connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. This block also has DirectLink interconnects for fast connections to and from a neighboring LAB. For more information about the UFM interface to the logic array, see "User Flash Memory Block" on page 2–18.

Table 2–2 shows the MAX II device routing scheme.

Table 2–2. MAX II Device Routing Scheme

Source	Destination										
	LUT Chain	**Register Chain**	**Local *(1)***	**DirectLink *(1)***	**R4 *(1)***	**C4 *(1)***	**LE**	**UFM Block**	**Column IOE**	**Row IOE**	**Fast I/O *(1)***
LUT Chain	—	—	—	—	—	—	✓	—	—	—	—
Register Chain	—	—	—	—	—	—	✓	—	—	—	—
Local Interconnect	—	—	—	—	—	—	✓	✓	✓	✓	—
DirectLink Interconnect	—	—	✓	—	—	—	—	—	—	—	—
R4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
C4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
LE	✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓
UFM Block	—	—	✓	✓	✓	✓	—	—	—	—	—
Column IOE	—	—	—	—	—	✓	—	—	—	—	—
Row IOE	—	—	—	✓	✓	✓	—	—	—	—	—

Note to Table 2–2:

(1) These categories are interconnects.

Global Signals

Each MAX II device has four dual-purpose dedicated clock pins (`GCLK[3..0]`, two pins on the left side and two pins on the right side) that drive the global clock network for clocking, as shown in Figure 2–13. These four pins can also be used as general-purpose I/O if they are not used to drive the global clock network.

The four global clock lines in the global clock network drive throughout the entire device. The global clock network can provide clocks for all resources within the device including LEs, LAB local interconnect, IOEs, and the UFM block. The global clock lines can also be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, or protocol control signals such as `TRDY` and `IRDY` for PCI. Internal logic can drive the global clock network for internally-generated global clocks and control signals. Figure 2–13 shows the various sources that drive the global clock network.

Document Revision History

Table 2–8 shows the revision history for this chapter.

Table 2–8. Document Revision History

Date and Revision	Changes Made	Summary of Changes
October 2008, version 2.2	■ Updated Table 2–4 and Table 2–6. ■ Updated "I/O Standards and Banks" section. ■ Updated New Document Format.	—
March 2008, version 2.1	■ Updated "Schmitt Trigger" section.	—
December 2007, version 2.0	■ Updated "Clear and Preset Logic Control" section. ■ Updated "MultiVolt Core" section. ■ Updated "MultiVolt I/O Interface" section. ■ Updated Table 2–7. ■ Added "Referenced Documents" section.	Updated document with MAX IIZ information.
December 2006, version 1.7	■ Minor update in "Internal Oscillator" section. Added document revision history.	—
August 2006, version 1.6	■ Updated functional description and I/O structure sections.	—
July 2006, vervion 1.5	■ Minor content and table updates.	—
February 2006, version 1.4	■ Updated "LAB Control Signals" section. ■ Updated "Clear and Preset Logic Control" section. ■ Updated "Internal Oscillator" section. ■ Updated Table 2–5.	—
August 2005, version 1.3	■ Removed Note 2 from Table 2-7.	—
December 2004, version 1.2	■ Added a paragraph to page 2-15.	—
June 2004, version 1.1	■ Added CFM acronym. Corrected Figure 2-19.	—

Table 3–3. 32-Bit MAX II Device IDCODE (Part 2 of 2)

Device	Binary IDCODE (32 Bits) *(1)*				HEX IDCODE
	Version (4 Bits)	Part Number	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*	
EPM240Z	0000	0010 0000 1010 0101	000 0110 1110	1	0x020A50DD
EPM570Z	0000	0010 0000 1010 0110	000 0110 1110	1	0x020A60DD

Notes to Table 3–2:

(1) The most significant bit (MSB) is on the left.

(2) The IDCODE's least significant bit (LSB) is always 1.

For JTAG AC characteristics, refer to the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*.

For more information about JTAG BST, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for MAX II Devices* chapter in the *MAX II Device Handbook*.

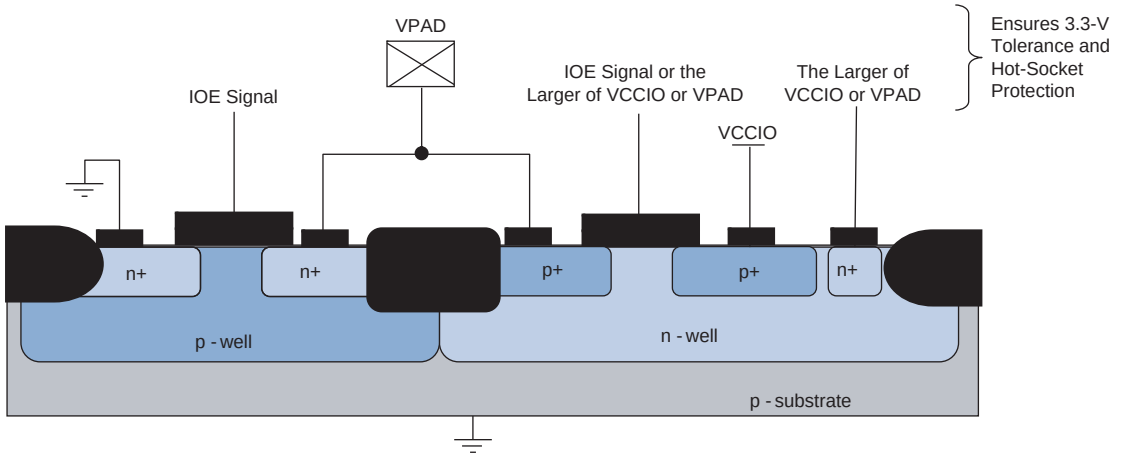
JTAG Block

The MAX II JTAG block feature allows you to access the JTAG TAP and state signals when either the USER0 or USER1 instruction is issued to the JTAG TAP. The USER0 and USER1 instructions bring the JTAG boundary-scan chain (TDI) through the user logic instead of the MAX II device's boundary-scan cells. Each USER instruction allows for one unique user-defined JTAG chain into the logic array.

Parallel Flash Loader

The JTAG block ability to interface JTAG to non-JTAG devices is ideal for general-purpose flash memory devices (such as Intel- or Fujitsu-based devices) that require programming during in-circuit test. The flash memory devices can be used for FPGA configuration or be part of system memory. In many cases, the MAX II device is already connected to these devices as the configuration control logic between the FPGA and the flash device. Unlike ISP-capable CPLD devices, bulk flash devices do not have JTAG TAP pins or connections. For small flash devices, it is common to use the serial JTAG scan chain of a connected device to program the non-JTAG flash device. This is slow and inefficient in most cases and impractical for large parallel flash devices. Using the MAX II device's JTAG block as a parallel flash loader, with the Quartus II software, to program and verify flash contents provides a fast and cost-effective means of in-circuit programming during test. Figure 3–1 shows MAX II being used as a parallel flash loader.

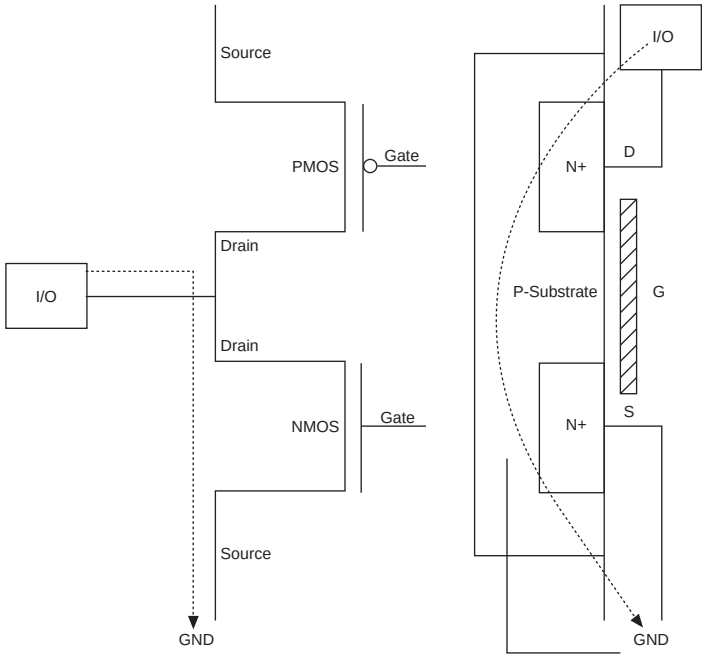
Figure 4–2. Transistor-Level Diagram of MAX II Device I/O Buffers



The CMOS output drivers in the I/O pins intrinsically provide electrostatic discharge (ESD) protection. There are two cases to consider for ESD voltage strikes: positive voltage zap and negative voltage zap.

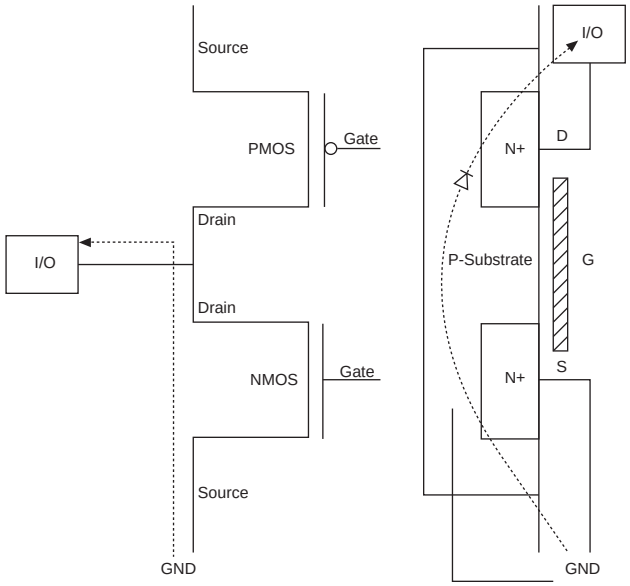
A positive ESD voltage zap occurs when a positive voltage is present on an I/O pin due to an ESD charge event. This can cause the N+ (Drain)/ P-Substrate junction of the N-channel drain to break down and the N+ (Drain)/P-Substrate/N+ (Source) intrinsic bipolar transistor turn on to discharge ESD current from I/O pin to GND. The dashed line (see Figure 4–3) shows the ESD current discharge path during a positive ESD zap.

Figure 4–3. ESD Protection During Positive Voltage Zap



When the I/O pin receives a negative ESD zap at the pin that is less than –0.7 V (0.7 V is the voltage drop across a diode), the intrinsic P-Substrate/N+ drain diode is forward biased. Therefore, the discharge ESD current path is from GND to the I/O pin, as shown in Figure 4–4.

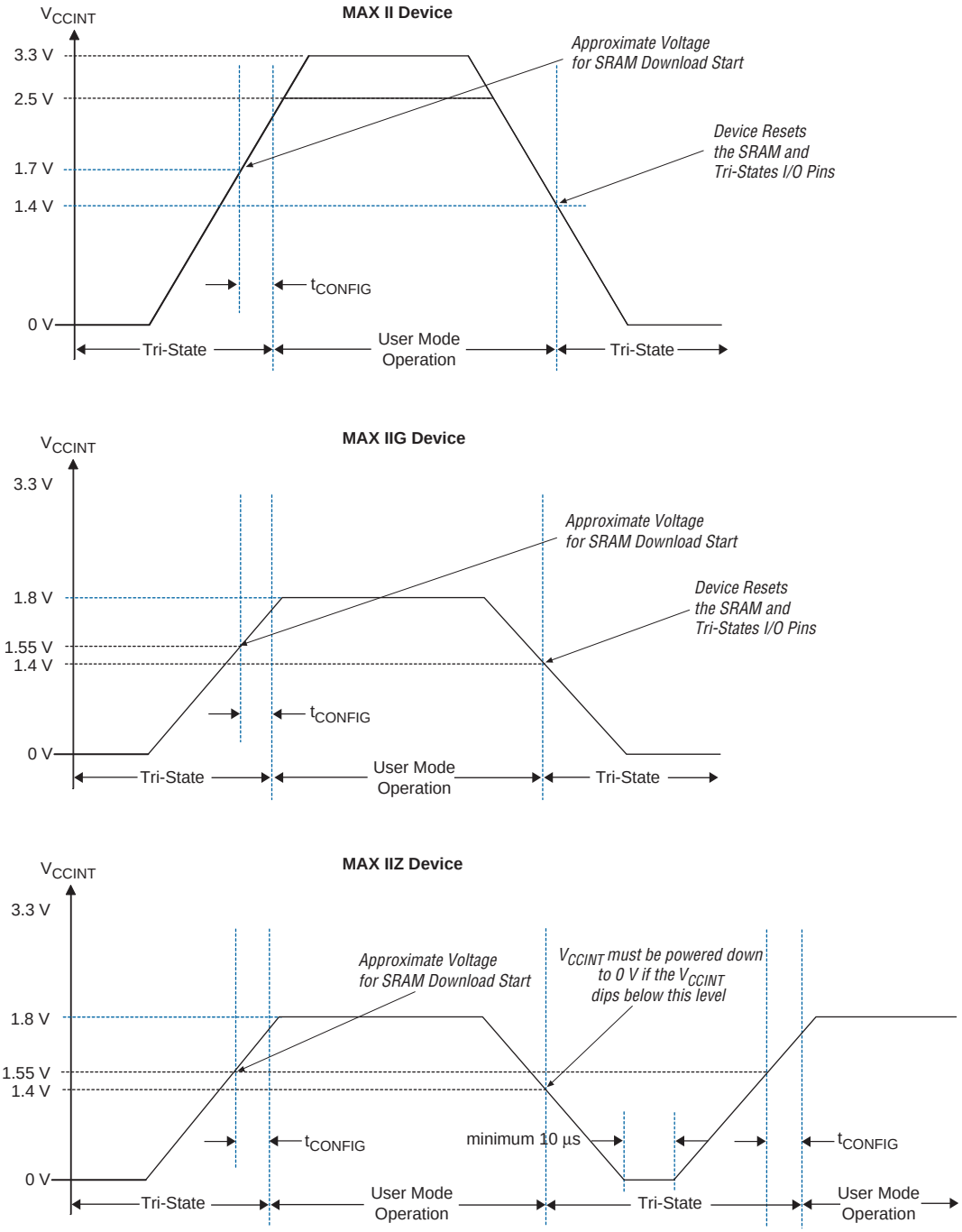
Figure 4–4. ESD Protection During Negative Voltage Zap



Power-On Reset Circuitry

MAX II devices have POR circuits to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up. The POR circuit monitors these voltages, triggering download from the non-volatile configuration flash memory (CFM) block to the SRAM logic, maintaining tri-state of the I/O pins (with weak pull-up resistors enabled) before and during this process. When the MAX II device enters user mode, the POR circuit releases the I/O pins to user functionality. The POR circuit of the MAX II (except MAX IIZ) device continues to monitor the V_{CCINT} voltage level to detect a brown-out condition. The POR circuit of the MAX IIZ device does not monitor the V_{CCINT} voltage level after the device enters into user mode. More details are provided in the following sub-sections.

Figure 4–5. Power-Up Characteristics for MAX II, MAX IIG, and MAX IIZ Devices *(Note 1), (2)*



Notes to Figure 4–5:

(1) Time scale is relative.

(2) Figure 4–5 assumes all V_{CCIO} banks power up simultaneously with the V_{CCINT} profile shown. If not, t_{CONFIG} stretches out until all V_{CCIO} banks are powered.

After SRAM configuration, all registers in the device are cleared and released into user function before I/O tri-states are released. To release clears after tri-states are released, use the DEV_CLRn pin option. To hold the tri-states beyond the power-up configuration time, use the DEV_OE pin option.

Power-Up Timing

Table 5–12 shows the power-up timing characteristics for MAX II devices.

Table 5–12. MAX II Power-Up Timing

Symbol	Parameter	Device	Min	Typ	Max	Unit
t_{CONFIG} *(1)*	The amount of time from when minimum V_{CCINT} is reached until the device enters user mode *(2)*	EPM240	—	—	200	µs
		EPM570	—	—	300	µs
		EPM1270	—	—	300	µs
		EPM2210	—	—	450	µs

Notes to Table 5–12:

(1) Table 5–12 values apply to commercial and industrial range devices. For extended temperature range devices, the t_{CONFIG} maximum values are as follows:

Device	Maximum
EPM240	300 µs
EPM570	400 µs
EPM1270	400 µs
EPM2210	500 µs

(2) For more information about POR trigger voltage, refer to the *Hot Socketing and Power-On Reset in MAX II Devices* chapter in the *MAX II Device Handbook*.

Power Consumption

Designers can use the Altera® PowerPlay Early Power Estimator and PowerPlay Power Analyzer to estimate the device power.

For more information about these power analysis tools, refer to the *Understanding and Evaluating Power in MAX II Devices* chapter in the *MAX II Device Handbook* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Timing Model and Specifications

MAX II devices timing can be analyzed with the Altera Quartus® II software, a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 5–2.

MAX II devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Table 5–13. MAX II Device Timing Model Status (Part 2 of 2)

Device	Preliminary	Final
EPM1270	—	✓
EPM2210	—	✓

Note to Table 5–13:

(1) The MAX IIZ device timing models are only available in the Quartus II software version 8.0 and later.

Performance

Table 5–14 shows the MAX II device performance for some common designs. All performance values were obtained with the Quartus II software compilation of megafunctions. Performance values for –3, –4, and –5 speed grades are based on an EPM1270 device target, while –6, –7, and –8 speed grades are based on an EPM570Z device target.

Table 5–14. MAX II Device Performance

Resource Used	Design Size and Function	Resources Used			Performance						Unit
					MAX II / MAX IIG			MAX IIZ			
		Mode	LEs	UFM Blocks	–3 Speed Grade	–4 Speed Grade	–5 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	
LE	16-bit counter *(1)*	—	16	0	304.0	247.5	201.1	184.1	123.5	118.3	MHz
	64-bit counter *(1)*	—	64	0	201.5	154.8	125.8	83.2	83.2	80.5	MHz
	16-to-1 multiplexer	—	11	0	6.0	8.0	9.3	17.4	17.3	20.4	ns
	32-to-1 multiplexer	—	24	0	7.1	9.0	11.4	12.5	22.8	25.3	ns
	16-bit XOR function	—	5	0	5.1	6.6	8.2	9.0	15.0	16.1	ns
	16-bit decoder with single address line	—	5	0	5.2	6.6	8.2	9.2	15.0	16.1	ns
UFM	512 × 16	None	3	1	10.0	10.0	10.0	10.0	10.0	10.0	MHz
	512 × 16	SPI *(2)*	37	1	8.0	8.0	8.0	9.7	9.7	9.7	MHz
	512 × 8	Parallel *(3)*	73	1	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	MHz
	512 × 16	I^2C *(3)*	142	1	100 *(5)*	100 *(5)*	100 *(5)*	100 *(5)*	100 *(5)*	100 *(5)*	kHz

Notes to Table 5–14:

(1) This design is a binary loadable up counter.
(2) This design is configured for read-only operation in Extended mode. Read and write ability increases the number of LEs used.
(3) This design is configured for read-only operation. Read and write ability increases the number of LEs used.
(4) This design is asynchronous.
(5) The I^2C megafunction is verified in hardware up to 100-kHz serial clock line (SCL) rate.

Figure 5–4. UFM Program Waveforms

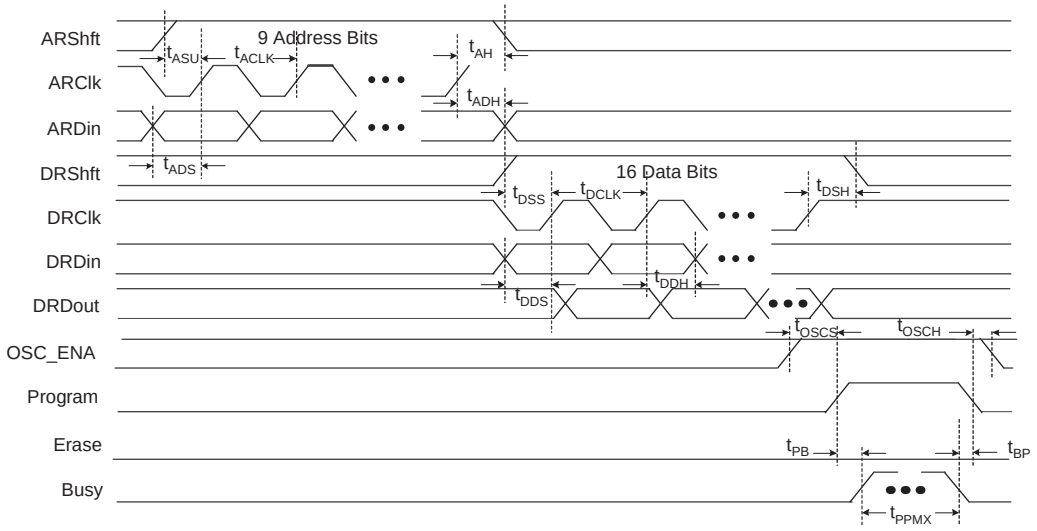


Figure 5–5. UFM Erase Waveform

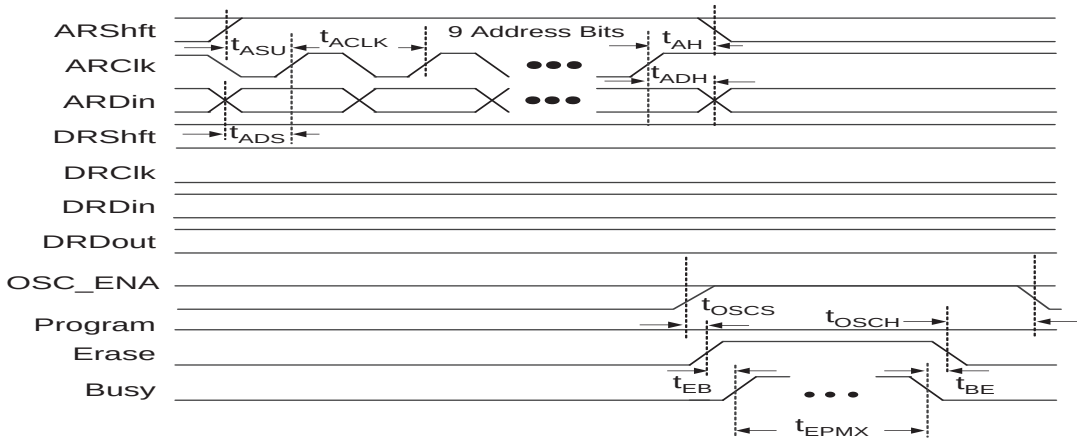


Table 5–22. Routing Delay Internal Timing Microparameters

Routing	MAX II / MAX IIG						MAX IIZ						Unit
	–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{C4}	—	429	—	556	—	687	—	*(1)*	—	*(1)*	—	*(1)*	ps
t_{R4}	—	326	—	423	—	521	—	*(1)*	—	*(1)*	—	*(1)*	ps
t_{LOCAL}	—	330	—	429	—	529	—	*(1)*	—	*(1)*	—	*(1)*	ps

Note to Table 5–22:

(1) The numbers will only be available in a later revision.

External Timing Parameters

External timing parameters are specified by device density and speed grade. All external I/O timing parameters shown are for the 3.3-V LVTTL I/O standard with the maximum drive strength and fast slew rate. For external I/O timing using standards other than LVTTL or for different drive strengths, use the I/O standard input and output delay adders in Table 5–27 through Table 5–31.

For more information about each external timing parameters symbol, refer to the *Understanding Timing in MAX II Devices* chapter in the *MAX II Device Handbook*.

Table 5–23 shows the external I/O timing parameters for EPM240 devices.

Table 5–23. EPM240 Global Clock External I/O Timing Parameters (Part 1 of 2)

			MAX II / MAX IIG						MAX IIZ						
			–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{PD1}	Worst case pin-to-pin delay through 1 look-up table (LUT)	10 pF	—	4.7	—	6.1	—	7.5	—	7.9	—	12.0	—	14.0	ns
t_{PD2}	Best case pin-to-pin delay through 1 LUT	10 pF	—	3.7	—	4.8	—	5.9	—	5.8	—	7.8	—	8.5	ns
t_{SU}	Global clock setup time	—	1.7	—	2.2	—	2.7	—	2.4	—	4.1	—	4.6	—	ns
t_{H}	Global clock hold time	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	4.3	2.0	5.6	2.0	6.9	2.0	6.6	2.0	8.1	2.0	8.6	ns
t_{CH}	Global clock high time	—	166	—	216	—	266	—	253	—	335	—	339	—	ps
t_{CL}	Global clock low time	—	166	—	216	—	266	—	253	—	335	—	339	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	3.3	—	4.0	—	5.0	—	5.4	—	8.1	—	8.4	—	ns

Table 5–29. External Timing Output Delay and t_{OD} Adders for Fast Slew Rate

I/O Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	8 mA	—	65	—	84	—	104	—	–6	—	–2	—	–3	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	4 mA	—	65	—	84	—	104	—	–6	—	–2	—	–3	ps
2.5-V LVTTL / LVCMOS	14 mA	—	122	—	158	—	195	—	–63	—	–71	—	–88	ps
	7 mA	—	193	—	251	—	309	—	10	—	–1	—	1	ps
1.8-V LVTTL / LVCMOS	6 mA	—	568	—	738	—	909	—	128	—	118	—	118	ps
	3 mA	—	654	—	850	—	1,046	—	352	—	327	—	332	ps
1.5-V LVCMOS	4 mA	—	1,059	—	1,376	—	1,694	—	421	—	400	—	400	ps
	2 mA	—	1,167	—	1,517	—	1,867	—	757	—	743	—	743	ps
3.3-V PCI	20 mA	—	3	—	4	—	5	—	–6	—	–2	—	–3	ps

Table 5–30. External Timing Output Delay and t_{OD} Adders for Slow Slew Rate

I/O Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	7,064	—	6,745	—	6,426	—	5,966	—	5,992	—	6,118	ps
	8 mA	—	7,946	—	7,627	—	7,308	—	6,541	—	6,570	—	6,720	ps
3.3-V LVCMOS	8 mA	—	7,064	—	6,745	—	6,426	—	5,966	—	5,992	—	6,118	ps
	4 mA	—	7,946	—	7,627	—	7,308	—	6,541	—	6,570	—	6,720	ps
2.5-V LVTTL / LVCMOS	14 mA	—	10,434	—	10,115	—	9,796	—	9,141	—	9,154	—	9,297	ps
	7 mA	—	11,548	—	11,229	—	10,910	—	9,861	—	9,874	—	10,037	ps
1.8-V LVTTL / LVCMOS	6 mA	—	22,927	—	22,608	—	22,289	—	21,811	—	21,854	—	21,857	ps
	3 mA	—	24,731	—	24,412	—	24,093	—	23,081	—	23,034	—	23,107	ps
1.5-V LVCMOS	4 mA	—	38,723	—	38,404	—	38,085	—	39,121	—	39,124	—	39,124	ps
	2 mA	—	41,330	—	41,011	—	40,692	—	40,631	—	40,634	—	40,634	ps
3.3-V PCI	20 mA	—	261	—	339	—	418	—	6,644	—	6,627	—	6,914	ps

Table 5–35. Document Revision History (Part 2 of 2)

Date and Revision	Changes Made	Summary of Changes
June 2005, version 1.3	■ Updated the R_{PULLUP} parameter in Table 5-4. ■ Added Note 2 to Tables 5-8 and 5-9. ■ Updated Table 5-13. ■ Added "Output Drive Characteristics" section. ■ Added I^2C mode and Notes 5 and 6 to Table 5-14. ■ Updated timing values to Tables 5-14 through 5-33.	—
December 2004, version 1.2	■ Updated timing Tables 5-2, 5-4, 5-12, and Tables 15-14 through 5-34. ■ Table 5-31 is new.	—
June 2004, version 1.1	■ Updated timing Tables 5-15 through 5-32.	—

Referenced Documents

This chapter references the following document:

- *Package Information* chapter in the *MAX II Device Handbook*

Document Revision History

Table 6–1 shows the revision history for this chapter.

Table 6–1. Document Revision History

Date and Revision	Changes Made	Summary of Changes
August 2009, version 1.6	■ Updated Figure 6–1.	Added information for speed grade –8
October 2008, version 1.5	■ Updated New Document Format.	—
December 2007, version 1.4	■ Added "Referenced Documents" section. ■ Updated Figure 6–1.	Updated document with MAX IIZ information.
December 2006, version 1.3	■ Added document revision history.	—
October 2006, version 1.2	■ Updated Figure 6-1.	—
June 2005, version 1.1	■ Removed Dual Marking section.	—