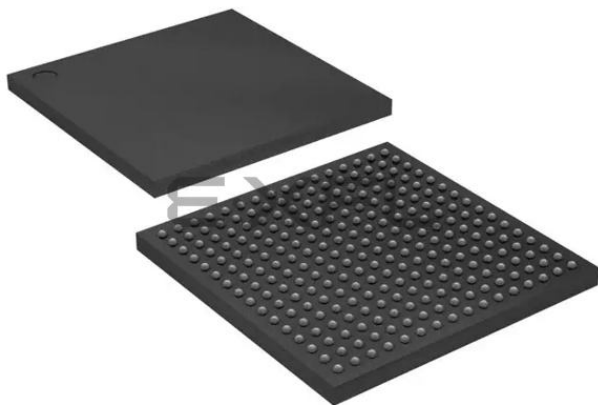




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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.4 ns
Voltage Supply - Internal	2.5V, 3.3V
Number of Logic Elements/Blocks	570
Number of Macrocells	440
Number of Gates	-
Number of I/O	160
Operating Temperature	0°C ~ 85°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm570f256c3

The Quartus II software automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions. The Quartus II software creates carry chains longer than 10 LEs by linking adjacent LABs within the same row together automatically. A carry chain can extend horizontally up to one full LAB row, but does not extend between LAB rows.

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. MAX II devices support simultaneous preset/asynchronous load and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, MAX II devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals and uses its own dedicated routing resources (that is, it does not use any of the four global resources). Driving this signal low before or during power-up prevents user mode from releasing clears within the design. This allows you to control when clear is released on a device that has just been powered-up. If not set for its chip-wide reset function, the DEV_CLRn pin is a regular I/O pin.

By default, all registers in MAX II devices are set to power-up low. However, this power-up state can be set to high on individual registers during design entry using the Quartus II software.

MultiTrack Interconnect

In the MAX II architecture, connections between LEs, the UFM, and device I/O pins are provided by the MultiTrack interconnect structure. The MultiTrack interconnect consists of continuous, performance-optimized routing lines used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

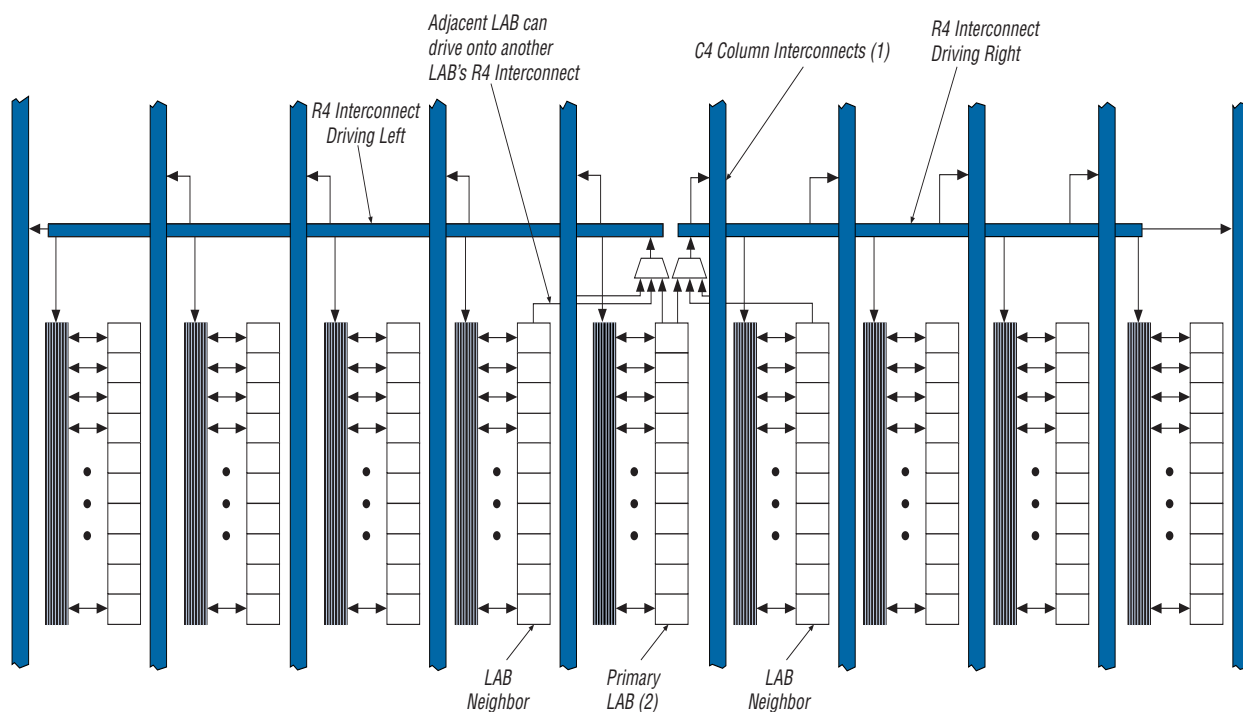
The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and short delays between logic levels instead of large delays associated with global or long routing lines. Dedicated row interconnects route signals to and from LABs within the same row. These row resources include:

- DirectLink interconnects between LABs
- R4 interconnects traversing four LABs to the right or left

The DirectLink interconnect allows an LAB to drive into the local interconnect of its left and right neighbors. The DirectLink interconnect provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The R4 interconnects span four LABs and are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2-10 shows R4 interconnect connections from an LAB. R4 interconnects can drive and be driven by row IOEs. For LAB interfacing, a primary LAB or horizontal LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 interconnects for connections from one row to another.

Figure 2-10. R4 Interconnect Connections



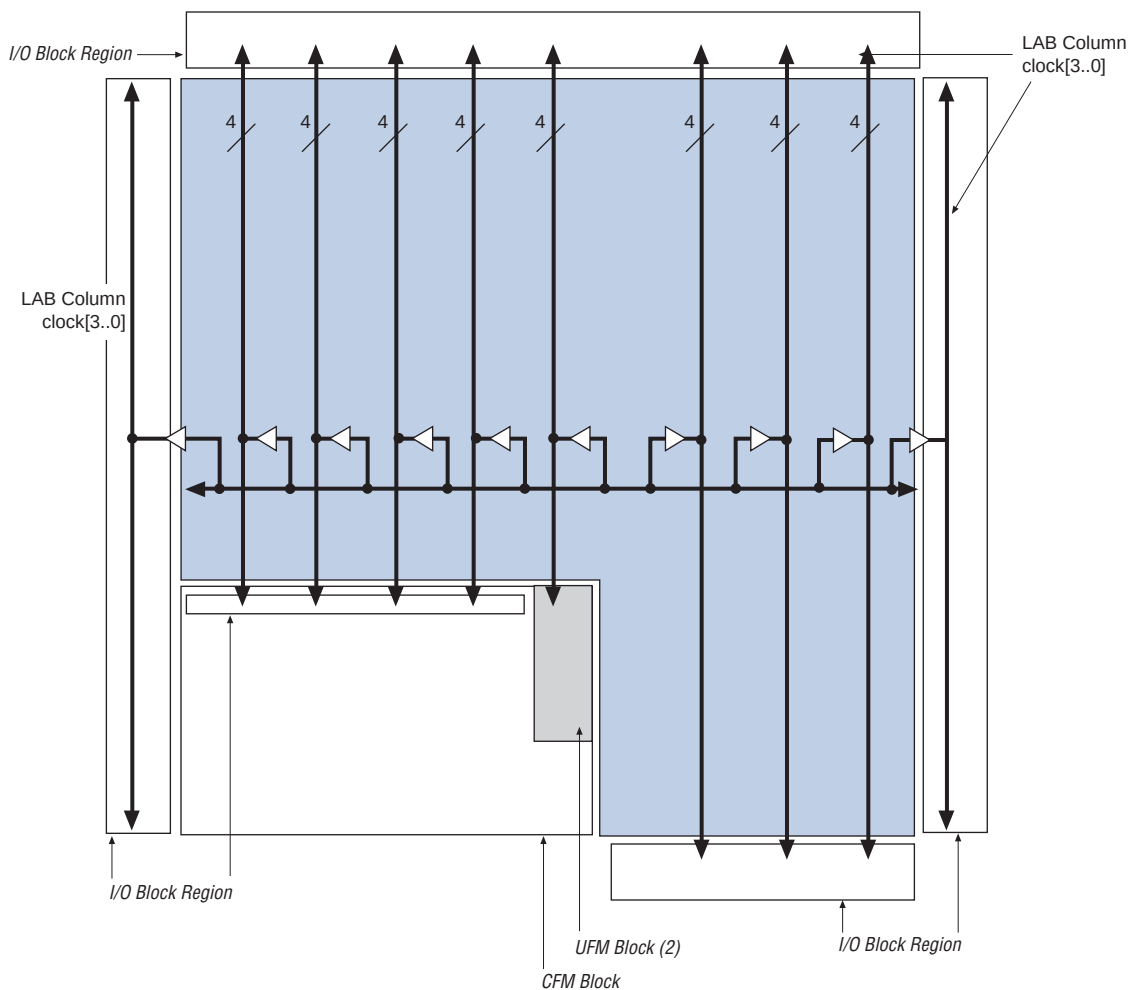
Notes to Figure 2-10:

- (1) C4 interconnects can drive R4 interconnects.
- (2) This pattern is repeated for every LAB in the LAB row.

The column interconnect operates similarly to the row interconnect. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs and row and column IOEs. These column resources include:

- LUT chain interconnects within an LAB
- Register chain interconnects within an LAB
- C4 interconnects traversing a distance of four LABs in an up and down direction

MAX II devices include an enhanced interconnect structure within LABs for routing LE output to LE input connections faster using LUT chain connections and register chain connections. The LUT chain connection allows the combinational output of an LE to directly drive the fast input of the LE right below it, bypassing the local interconnect. These resources can be used as a high-speed connection for wide fan-in

Figure 2-14. Global Clock Network (Note 1)**Notes to Figure 2-14:**

- (1) LAB column clocks in I/O block regions provide high fan-out output enable signals.
- (2) LAB column clocks drive to the UFM block.

User Flash Memory Block

MAX II devices feature a single UFM block, which can be used like a serial EEPROM for storing non-volatile information up to 8,192 bits. The UFM block connects to the logic array through the MultiTrack interconnect, allowing any LE to interface to the UFM block. Figure 2-15 shows the UFM block and interface signals. The logic array is used to create customer interface or protocol logic to interface the UFM block data outside of the device. The UFM block offers the following features:

- Non-volatile storage up to 16-bit wide and 8,192 total bits
- Two sectors for partitioned sector erase
- Built-in internal oscillator that optionally drives logic array
- Program, erase, and busy signals

Table 2-4 describes the I/O standards supported by MAX II devices.

Table 2-4. MAX II I/O Standards

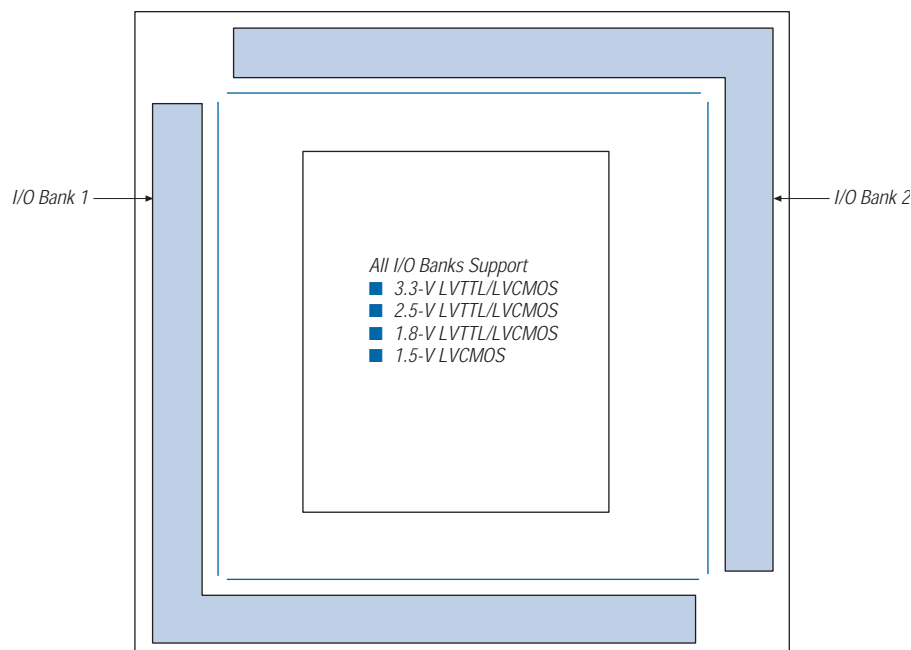
I/O Standard	Type	Output Supply Voltage (VCCIO) (V)
3.3-V LVTTL/LVCMOS	Single-ended	3.3
2.5-V LVTTL/LVCMOS	Single-ended	2.5
1.8-V LVTTL/LVCMOS	Single-ended	1.8
1.5-V LVCMOS	Single-ended	1.5
3.3-V PCI (1)	Single-ended	3.3

Note to Table 2-4:

(1) The 3.3-V PCI compliant I/O is supported in Bank 3 of the EPM1270 and EPM2210 devices.

The EPM240 and EPM570 devices support two I/O banks, as shown in Figure 2-22. Each of these banks support all the LVTTL and LVCMOS standards shown in Table 2-4. PCI compliant I/O is not supported in these devices and banks.

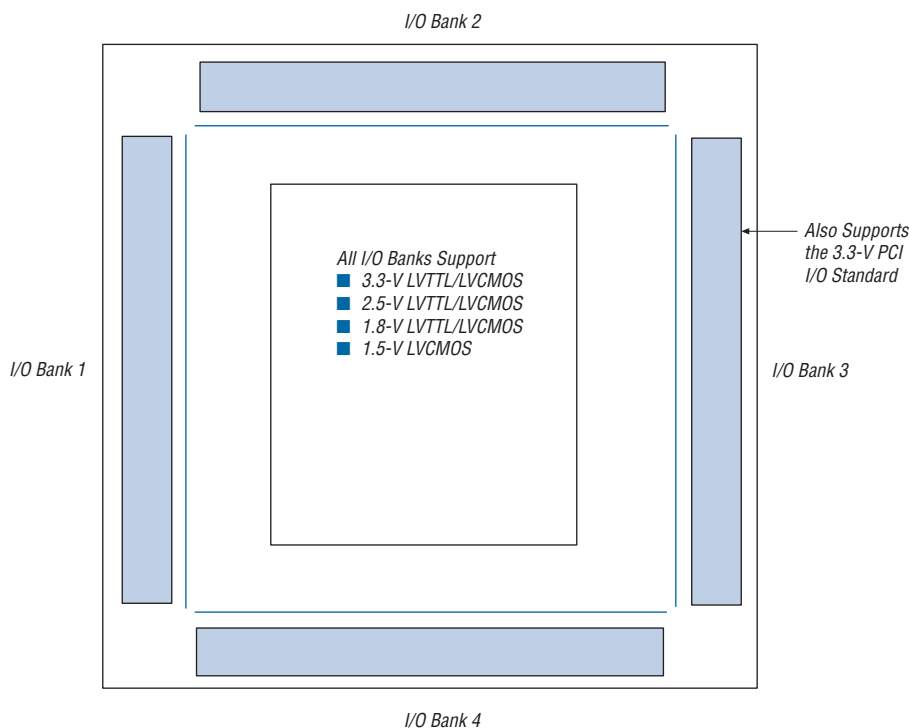
Figure 2-22. MAX II I/O Banks for EPM240 and EPM570 (Note 1), (2)



Notes to Figure 2-22:

- (1) Figure 2-22 is a top view of the silicon die.
- (2) Figure 2-22 is a graphical representation only. Refer to the pin list and the Quartus II software for exact pin locations.

The EPM1270 and EPM2210 devices support four I/O banks, as shown in Figure 2-23. Each of these banks support all of the LVTTL and LVCMOS standards shown in Table 2-4. PCI compliant I/O is supported in Bank 3. Bank 3 supports the PCI clamping diode on inputs and PCI drive compliance on outputs. You must use Bank 3 for designs requiring PCI compliant I/O pins. The Quartus II software automatically places I/O pins in this bank if assigned with the PCI I/O standard.

Figure 2-23. MAX II I/O Banks for EPM1270 and EPM2210 (Note 1), (2)**Notes to Figure 2-23:**

- (1) Figure 2-23 is a top view of the silicon die.
- (2) Figure 2-23 is a graphical representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Each I/O bank has dedicated V_{CCIO} pins that determine the voltage standard support in that bank. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each individual bank can support a different standard. Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3 V, Bank 3 can support LVTTTL, LVCMOS, and 3.3-V PCI. V_{CCIO} powers both the input and output buffers in MAX II devices.

The JTAG pins for MAX II devices are dedicated pins that cannot be used as regular I/O pins. The pins TMS, TDI, TDO, and TCK support all the I/O standards shown in Table 2-4 on page 2-27 except for PCI. These pins reside in Bank 1 for all MAX II devices and their I/O standard support is controlled by the V_{CCIO} setting for Bank 1.

PCI Compliance

The MAX II EPM1270 and EPM2210 devices are compliant with PCI applications as well as all 3.3-V electrical specifications in the *PCI Local Bus Specification Revision 2.2*. These devices are also large enough to support PCI intellectual property (IP) cores. Table 2-5 shows the MAX II device speed grades that meet the PCI timing specifications.

Table 2-6. Programmable Drive Strength *(Note 1)*

I/O Standard	IOH/IOL Current Strength Setting (mA)
3.3-V LVTTTL	16
	8
3.3-V LVCMOS	8
	4
2.5-V LVTTTL/LVCMOS	14
	7
1.8-V LVTTTL/LVCMOS	6
	3
1.5-V LVCMOS	4
	2

Note to Table 2-6:

- (1) The I_{OH} current strength numbers shown are for a condition of a $V_{OUT} = V_{OH}$ minimum, where the V_{OH} minimum is specified by the I/O standard. The I_{OL} current strength numbers shown are for a condition of a $V_{OUT} = V_{OL}$ maximum, where the V_{OL} maximum is specified by the I/O standard. For 2.5-V LVTTTL/LVCMOS, the I_{OH} condition is $V_{OUT} = 1.7$ V and the I_{OL} condition is $V_{OUT} = 0.7$ V.

Slew-Rate Control

The output buffer for each MAX II device I/O pin has a programmable output slew-rate control that can be configured for low noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal output delay to rising and falling edges. The lower the voltage standard (for example, 1.8-V LVTTTL) the larger the output delay when slow slew is enabled. Each I/O pin has an individual slew-rate control, allowing the designer to specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges.

Open-Drain Output

MAX II devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that can be asserted by any of several devices. This output can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX II devices can be used as an additional ground pin. This programmable ground feature does not require the use of the associated LEs in the device. In the Quartus II software, unused pins can be set as programmable GND on a global default basis or they can be individually assigned. Unused pins also have the option of being set as tri-stated input pins.

Bus Hold

Each MAX II device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. The designer can select this feature individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the device cannot use the programmable pull-up option.

The bus-hold circuitry uses a resistor to pull the signal level to the last driven state. The *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* gives the specific sustaining current for each V_{CCIO} voltage level driven through this resistor and overdrive current used to identify the next-driven input level.

The bus-hold circuitry is only active after the device has fully initialized. The bus-hold circuit captures the value on the pin present at the moment user mode is entered.

Programmable Pull-Up Resistor

Each MAX II device I/O pin provides an optional programmable pull-up resistor during user mode. If the designer enables this feature for an I/O pin, the pull-up resistor holds the output to the V_{CCIO} level of the output pin's bank.



The programmable pull-up resistor feature should not be used at the same time as the bus-hold feature on a given I/O pin.

Programmable Input Delay

The MAX II IOE includes a programmable input delay that is activated to ensure zero hold times. A path where a pin directly drives a register, with minimal routing between the two, may require the delay to ensure zero hold time. However, a path where a pin drives a register through long routing or through combinational logic may not require the delay to achieve a zero hold time. The Quartus II software uses this delay to ensure zero hold times when needed.

MultiVolt I/O Interface

The MAX II architecture supports the MultiVolt I/O interface feature, which allows MAX II devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation (V_{CCINT}), and up to four sets for input buffers and I/O output driver buffers (V_{CCIO}), depending on the number of I/O banks available in the devices where each set of VCC pins powers one I/O bank. The EPM240 and EPM570 devices have two I/O banks respectively while the EPM1270 and EPM2210 devices have four I/O banks respectively.

Table 3–1. MAX II JTAG Instructions (Part 2 of 2)

JTAG Instruction	Instruction Code	Description
CLAMP (1)	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the boundary scan test data to pass synchronously through selected devices to adjacent devices during normal device operation, while holding I/O pins to a state defined by the data in the boundary-scan register.
USER0	00 0000 1100	This instruction allows you to define the scan chain between TDI and TDO in the MAX II logic array. This instruction is also used for custom logic and JTAG interfaces.
USER1	00 0000 1110	This instruction allows you to define the scan chain between TDI and TDO in the MAX II logic array. This instruction is also used for custom logic and JTAG interfaces.
IEEE 1532 instructions	(2)	IEEE 1532 ISC instructions used when programming a MAX II device via the JTAG port.

Notes to Table 3–1:

- (1) HIGHZ, CLAMP, and EXTEST instructions do not disable weak pull-up resistors or bus hold features.
- (2) These instructions are shown in the 1532 BSDL files, which will be posted on the Altera® website at www.altera.com when they are available.



Unsupported JTAG instructions should not be issued to the MAX II device as this may put the device into an unknown state, requiring a power cycle to recover device operation.

The MAX II device instruction register length is 10 bits and the USERCODE register length is 32 bits. Table 3–2 and Table 3–3 show the boundary-scan register length and device IDCODE information for MAX II devices.

Table 3–2. MAX II Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM240	240
EPM570	480
EPM1270	636
EPM2210	816

Table 3–3. 32-Bit MAX II Device IDCODE (Part 1 of 2)

Device	Binary IDCODE (32 Bits) (1)				HEX IDCODE
	Version (4 Bits)	Part Number	Manufacturer Identity (11 Bits)	LSB (1 Bit) (2)	
EPM240 EPM240G	0000	0010 0000 1010 0001	000 0110 1110	1	0x020A10DD
EPM570 EPM570G	0000	0010 0000 1010 0010	000 0110 1110	1	0x020A20DD
EPM1270 EPM1270G	0000	0010 0000 1010 0011	000 0110 1110	1	0x020A30DD
EPM2210 EPM2210G	0000	0010 0000 1010 0100	000 0110 1110	1	0x020A40DD

IEEE 1532 Support

The JTAG circuitry and ISP instruction set in MAX II devices is compliant to the IEEE 1532-2002 programming specification. This provides industry-standard hardware and software for in-system programming among multiple vendor programmable logic devices (PLDs) in a JTAG chain.

The MAX II 1532 BSDL files will be released on the Altera website when available.

Jam Standard Test and Programming Language (STAPL)

The Jam STAPL JEDEC standard, JESD71, can be used to program MAX II devices with in-circuit testers, PCs, or embedded processors. The Jam byte code is also supported for MAX II devices. These software programming protocols provide a compact embedded solution for programming MAX II devices.



For more information, refer to the *Using Jam STAPL for ISP via an Embedded Processor* chapter in the *MAX II Device Handbook*.

Programming Sequence

During in-system programming, 1532 instructions, addresses, and data are shifted into the MAX II device through the TDI input pin. Data is shifted out through the TDO output pin and compared against the expected data. Programming a pattern into the device requires the following six ISP steps. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6. These steps are automatically executed by third-party programmers, the Quartus II software, or the Jam STAPL and Jam Byte-Code Players.

1. *Enter ISP*—The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode.
2. *Check ID*—Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Sector Erase*—Erasing the device in-system involves shifting in the instruction to erase the device and applying an erase pulse(s). The erase pulse is automatically generated internally by waiting in the run/test/idle state for the specified erase pulse time of 500 ms for the CFM block and 500 ms for each sector of the UFM block.
4. *Program*—Programming the device in-system involves shifting in the address, data, and program instruction and generating the program pulse to program the flash cells. The program pulse is automatically generated internally by waiting in the run/test/idle state for the specified program pulse time of 75 μ s. This process is repeated for each address in the CFM and UFM blocks.
5. *Verify*—Verifying a MAX II device in-system involves shifting in addresses, applying the verify instruction to generate the read pulse, and shifting out the data for comparison. This process is repeated for each CFM and UFM address.
6. *Exit ISP*—An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode.

Real-Time ISP

For systems that require more than DC logic level control of I/O pins, the real-time ISP feature allows you to update the CFM block with a new design image while the current design continues to operate in the SRAM logic array and I/O pins. A new programming file is updated into the MAX II device without halting the original design's operation, saving down-time costs for remote or field upgrades. The updated CFM block configures the new design into the SRAM upon the next power cycle. It is also possible to execute an immediate configuration of the SRAM without a power cycle by using a specific sequence of ISP commands. The configuration of SRAM without a power cycle takes a specific amount of time (t_{CONFIG}). During this time, the I/O pins are tri-stated and weakly pulled-up to V_{CCIO} .

Design Security

All MAX II devices contain a programmable security bit that controls access to the data programmed into the CFM block. When this bit is programmed, design programming information, stored in the CFM block, cannot be copied or retrieved. This feature provides a high level of design security because programmed data within flash memory cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is erased. The SRAM is also invisible and cannot be accessed regardless of the security bit setting. The UFM block data is not protected by the security bit and is accessible through JTAG or logic array connections.

Programming with External Hardware

MAX II devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera® ByteblasterMV™, MasterBlaster™, ByteBlaster™ II, and USB-Blaster cables.

BP Microsystems, System General, and other programming hardware manufacturers provide programming support for Altera devices. Check their websites for device support information.

Referenced Documents

This chapter references the following documents:

- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *IEEE 1149.1 (JTAG) Boundary-Scan Testing for MAX II Devices* chapter in the *MAX II Device Handbook*
- *Real-Time ISP and ISP Clamp for MAX II Devices* chapter in the *MAX II Device Handbook*
- *Using Jam STAPL for ISP via an Embedded Processor* chapter in the *MAX II Device Handbook*

Document Revision History

Table 3-5 shows the revision history for this chapter.

Table 3-5. Document Revision History

Date and Revision	Changes Made	Summary of Changes
October 2008, version 1.6	■ Updated New Document Format.	—
December 2007, version 1.5	■ Added warning note after Table 3-1. ■ Updated Table 3-3 and Table 3-4. ■ Added “Referenced Documents” section.	—
December 2006, version 1.4	■ Added document revision history.	—
June 2005, version 1.3	■ Added text and Table 3-4.	—
June 2005, version 1.3	■ Updated text on pages 3-5 to 3-8.	—
June 2004, version 1.1	■ Corrected Figure 3-1. Added CFM acronym.	—

Introduction

MAX® II devices offer hot socketing, also known as hot plug-in or hot swap, and power sequencing support. Designers can insert or remove a MAX II board in a system during operation without undesirable effects to the system bus. The hot socketing feature removes some of the difficulties designers face when using components on printed circuit boards (PCBs) that contain a mixture of 3.3-, 2.5-, 1.8-, and 1.5-V devices.

The MAX II device hot socketing feature provides:

- Board or device insertion and removal
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter contains the following sections:

- [“MAX II Hot-Socketing Specifications” on page 4-1](#)
- [“Power-On Reset Circuitry” on page 4-5](#)

MAX II Hot-Socketing Specifications

MAX II devices offer all three of the features required for the hot-socketing capability listed above without any external components or special design requirements. The following are hot-socketing specifications:

- The device can be driven before and during power-up or power-down without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.
- Signal pins do not drive the V_{CCIO} or V_{CCINT} power supplies. External input signals to device I/O pins do not power the device V_{CCIO} or V_{CCINT} power supplies via internal paths. This is true if the V_{CCINT} and the V_{CCIO} supplies are held at GND.



Altera uses GND as reference for the hot-socketing and I/O buffers circuitry designs. You must connect the GND between boards before connecting the V_{CCINT} and the V_{CCIO} power supplies to ensure device reliability and compliance to the hot-socketing specifications.

Devices Can Be Driven before Power-Up

Signals can be driven into the MAX II device I/O pins and GCLK[3..0] pins before or during power-up or power-down without damaging the device. MAX II devices support any power-up or power-down sequence (V_{CCIO1} , V_{CCIO2} , V_{CCIO3} , V_{CCIO4} , V_{CCINT}), simplifying the system-level design.

Table 5-13. MAX II Device Timing Model Status (Part 2 of 2)

Device	Preliminary	Final
EPM1270	—	✓
EPM2210	—	✓

Note to Table 5-13:

- (1) The MAX IIZ device timing models are only available in the Quartus II software version 8.0 and later.

Performance

Table 5-14 shows the MAX II device performance for some common designs. All performance values were obtained with the Quartus II software compilation of megafunctions. Performance values for -3, -4, and -5 speed grades are based on an EPM1270 device target, while -6, -7, and -8 speed grades are based on an EPM570Z device target.

Table 5-14. MAX II Device Performance

Resource Used	Design Size and Function	Resources Used			Performance						Unit
					MAX II / MAX IIG			MAX IIZ			
		Mode	LEs	UFM Blocks	–3 Speed Grade	–4 Speed Grade	–5 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	
LE	16-bit counter (1)	—	16	0	304.0	247.5	201.1	184.1	123.5	118.3	MHz
	64-bit counter (1)	—	64	0	201.5	154.8	125.8	83.2	83.2	80.5	MHz
	16-to-1 multiplexer	—	11	0	6.0	8.0	9.3	17.4	17.3	20.4	ns
	32-to-1 multiplexer	—	24	0	7.1	9.0	11.4	12.5	22.8	25.3	ns
	16-bit XOR function	—	5	0	5.1	6.6	8.2	9.0	15.0	16.1	ns
	16-bit decoder with single address line	—	5	0	5.2	6.6	8.2	9.2	15.0	16.1	ns
UFM	512 × 16	None	3	1	10.0	10.0	10.0	10.0	10.0	10.0	MHz
	512 × 16	SPI (2)	37	1	8.0	8.0	8.0	9.7	9.7	9.7	MHz
	512 × 8	Parallel (3)	73	1	(4)	(4)	(4)	(4)	(4)	(4)	MHz
	512 × 16	I²C (3)	142	1	100 (5)	100 (5)	100 (5)	100 (5)	100 (5)	100 (5)	kHz

Notes to Table 5-14:

- (1) This design is a binary loadable up counter.
- (2) This design is configured for read-only operation in Extended mode. Read and write ability increases the number of LEs used.
- (3) This design is configured for read-only operation. Read and write ability increases the number of LEs used.
- (4) This design is asynchronous.
- (5) The I²C megafunction is verified in hardware up to 100-kHz serial clock line (SCL) rate.

Table 5-16. IOE Internal Timing Microparameters

Symbol	Parameter	MAX II / MAX IIG						MAX IIZ						Unit
		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{FASTIO}	Data output delay from adjacent LE to I/O block	—	159	—	207	—	254	—	170	—	348	—	428	ps
t _{IIN}	I/O input pad and buffer delay	—	708	—	920	—	1,132	—	907	—	970	—	986	ps
t _{GLOB} (1)	I/O input pad and buffer delay used as global signal pin	—	1,519	—	1,974	—	2,430	—	2,261	—	2,670	—	3,322	ps
t _{IOE}	Internally generated output enable delay	—	354	—	374	—	460	—	530	—	966	—	1,410	ps
t _{DL}	Input routing delay	—	224	—	291	—	358	—	318	—	410	—	509	ps
t _{OD} (2)	Output delay buffer and pad delay	—	1,064	—	1,383	—	1,702	—	1,319	—	1,526	—	1,543	ps
t _{XZ} (3)	Output buffer disable delay	—	756	—	982	—	1,209	—	1,045	—	1,264	—	1,276	ps
t _{ZX} (4)	Output buffer enable delay	—	1,003	—	1,303	—	1,604	—	1,160	—	1,325	—	1,353	ps

Notes to Table 5-16:

- (1) Delay numbers for t_{GLOB} differ for each device density and speed grade. The delay numbers for t_{GLOB} , shown in Table 5-16, are based on an EPM240 device target.
- (2) Refer to Table 5-32 and 5-24 for delay adders associated with different I/O standards, drive strengths, and slew rates.
- (3) Refer to Table 5-19 and 5-14 for t_{XZ} delay adders associated with different I/O standards, drive strengths, and slew rates.
- (4) Refer to Table 5-17 and 5-13 for t_{ZX} delay adders associated with different I/O standards, drive strengths, and slew rates.

Table 5-17 through Table 5-20 show the adder delays for t_{ZX} and t_{XZ} microparameters when using an I/O standard other than 3.3-V LVTTTL with 16 mA drive strength.

Table 5-17. t_{ZX} IOE Microparameter Adders for Fast Slew Rate (Part 1 of 2)

Standard		MAX II / MAX IIG						MAX IIZ						Unit
		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	16 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	8 mA	—	28	—	37	—	45	—	72	—	71	—	74	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	4 mA	—	28	—	37	—	45	—	72	—	71	—	74	ps
2.5-V LVTTTL / LVCMOS	14 mA	—	14	—	19	—	23	—	75	—	87	—	90	ps
	7 mA	—	314	—	409	—	503	—	162	—	174	—	177	ps
1.8-V LVTTTL / LVCMOS	6 mA	—	450	—	585	—	720	—	279	—	289	—	291	ps
	3 mA	—	1,443	—	1,876	—	2,309	—	499	—	508	—	512	ps

Table 5-21. UFM Block Internal Timing Microparameters (Part 2 of 3)

Symbol	Parameter	MAX II / MAX IIG						MAX IIZ						Unit
		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{DDS}	Data register data in setup to data register clock	20	—	20	—	20	—	20	—	20	—	20	—	ns
t _{DDH}	Data register data in hold from data register clock	20	—	20	—	20	—	20	—	20	—	20	—	ns
t _{DP}	Program signal to data clock hold time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t _{PB}	Maximum delay between program rising edge to UFM busy signal rising edge	—	960	—	960	—	960	—	960	—	960	—	960	ns
t _{BP}	Minimum delay allowed from UFM busy signal going low to program signal going low	20	—	20	—	20	—	20	—	20	—	20	—	ns
t _{PPMX}	Maximum length of busy pulse during a program	—	100	—	100	—	100	—	100	—	100	—	100	μs
t _{AE}	Minimum erase signal to address clock hold time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t _{EB}	Maximum delay between the erase rising edge to the UFM busy signal rising edge	—	960	—	960	—	960	—	960	—	960	—	960	ns
t _{BE}	Minimum delay allowed from the UFM busy signal going low to erase signal going low	20	—	20	—	20	—	20	—	20	—	20	—	ns
t _{EPMX}	Maximum length of busy pulse during an erase	—	500	—	500	—	500	—	500	—	500	—	500	ms
t _{DCO}	Delay from data register clock to data register output	—	5	—	5	—	5	—	5	—	5	—	5	ns

Table 5-21. UFM Block Internal Timing Microparameters (Part 3 of 3)

Symbol	Parameter	MAX II / MAX IIG						MAX IIZ						Unit
		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{OE}	Delay from data register clock to data register output	180	—	180	—	180	—	180	—	180	—	180	—	ns
t _{RA}	Maximum read access time	—	65	—	65	—	65	—	65	—	65	—	65	ns
t _{OSCS}	Maximum delay between the OSC_ENA rising edge to the erase/program signal rising edge	250	—	250	—	250	—	250	—	250	—	250	—	ns
t _{OSCH}	Minimum delay allowed from the erase/program signal going low to OSC_ENA signal going low	250	—	250	—	250	—	250	—	250	—	250	—	ns

Figure 5-3 through Figure 5-5 show the read, program, and erase waveforms for UFM block timing parameters shown in Table 5-21.

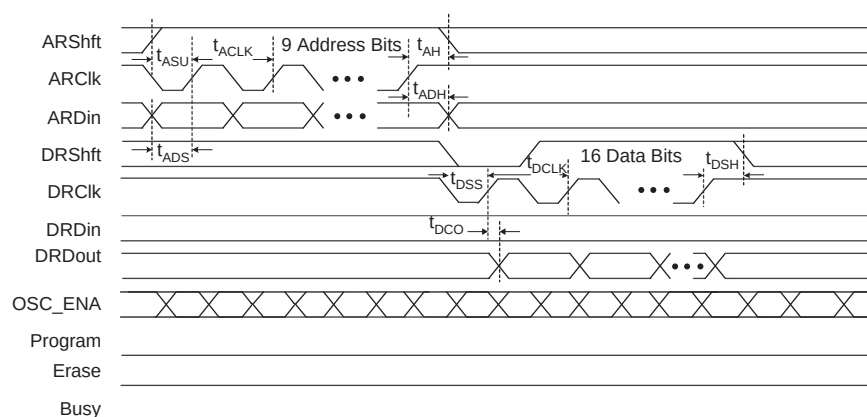
Figure 5-3. UFM Read Waveforms

Table 5-24. EPM570 Global Clock External I/O Timing Parameters (Part 2 of 2)

Symbol	Parameter	Condition	MAX II / MAX IIG						MAX IIZ						Unit
			−3 Speed Grade		−4 Speed Grade		−5 Speed Grade		−6 Speed Grade		−7 Speed Grade		−8 Speed Grade		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f _{CNT}	Maximum global clock frequency for 16-bit counter	—	—	304.0 <i>(1)</i>	—	247.5	—	201.1	—	184.1	—	123.5	—	118.3	MHz

Note to Table 5-24:

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5-25 shows the external I/O timing parameters for EPM1270 devices.

Table 5-25. EPM1270 Global Clock External I/O Timing Parameters

Symbol	Parameter	Condition	MAX II / MAX IIG						Unit
			–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Worst case pin-to-pin delay through 1 look-up table (LUT)	10 pF	—	6.2	—	8.1	—	10.0	ns
t _{PD2}	Best case pin-to-pin delay through 1 LUT	10 pF	—	3.7	—	4.8	—	5.9	ns
t _{SU}	Global clock setup time	—	1.2	—	1.5	—	1.9	—	ns
t _H	Global clock hold time	—	0	—	0	—	0	—	ns
t _{CO}	Global clock to output delay	10 pF	2.0	4.6	2.0	5.9	2.0	7.3	ns
t _{CH}	Global clock high time	—	166	—	216	—	266	—	ps
t _{CL}	Global clock low time	—	166	—	216	—	266	—	ps
t _{CNT}	Minimum global clock period for 16-bit counter	—	3.3	—	4.0	—	5.0	—	ns
f _{CNT}	Maximum global clock frequency for 16-bit counter	—	—	304.0 (1)	—	247.5	—	201.1	MHz

Note to Table 5-25:

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5-27. External Timing Input Delay Adders (Part 2 of 2)

I/O Standard		MAX II / MAX IIG						MAX IIZ						Unit
		−3 Speed Grade		−4 Speed Grade		−5 Speed Grade		−6 Speed Grade		−7 Speed Grade		−8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVCMOS	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	334	—	434	—	535	—	387	—	434	—	442	ps
2.5-V LVTTTL / LVCMOS	Without Schmitt Trigger	—	23	—	30	—	37	—	42	—	43	—	43	ps
	With Schmitt Trigger	—	339	—	441	—	543	—	429	—	476	—	483	ps
1.8-V LVTTTL / LVCMOS	Without Schmitt Trigger	—	291	—	378	—	466	—	378	—	373	—	373	ps
1.5-V LVCMOS	Without Schmitt Trigger	—	681	—	885	—	1,090	—	681	—	622	—	658	ps
3.3-V PCI	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	—	0	ps

Table 5-28. External Timing Input Delay t_{GLOB} Adders for GCLK Pins

I/O Standard		MAX II / MAX IIG						MAX IIZ						Unit
		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	308	—	400	—	493	—	387	—	434	—	442	ps
3.3-V LVCMOS	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	308	—	400	—	493	—	387	—	434	—	442	ps
2.5-V LVTTTL / LVCMOS	Without Schmitt Trigger	—	21	—	27	—	33	—	42	—	43	—	43	ps
	With Schmitt Trigger	—	423	—	550	—	677	—	429	—	476	—	483	ps
1.8-V LVTTTL / LVCMOS	Without Schmitt Trigger	—	353	—	459	—	565	—	378	—	373	—	373	ps
1.5-V LVCMOS	Without Schmitt Trigger	—	855	—	1,111	—	1,368	—	681	—	622	—	658	ps
3.3-V PCI	Without Schmitt Trigger	—	6	—	7	—	9	—	0	—	0	—	0	ps

Table 5-35. Document Revision History (Part 2 of 2)

Date and Revision	Changes Made	Summary of Changes
June 2005, version 1.3	■ Updated the R_{PULLUP} parameter in Table 5-4. ■ Added Note 2 to Tables 5-8 and 5-9. ■ Updated Table 5-13. ■ Added “Output Drive Characteristics” section. ■ Added I²C mode and Notes 5 and 6 to Table 5-14. ■ Updated timing values to Tables 5-14 through 5-33.	—
December 2004, version 1.2	■ Updated timing Tables 5-2, 5-4, 5-12, and Tables 15-14 through 5-34. ■ Table 5-31 is new.	—
June 2004, version 1.1	■ Updated timing Tables 5-15 through 5-32.	—