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Understanding <u>Embedded - CPLDs (Complex</u> <u>Programmable Logic Devices)</u>

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixedfunction ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.4 ns
Voltage Supply - Internal	2.5V, 3.3V
Number of Logic Elements/Blocks	570
Number of Macrocells	440
Number of Gates	-
Number of I/O	160
Operating Temperature	0°C ~ 85°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm570f256c4n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

MAX II devices are available in space-saving FineLine BGA, Micro FineLine BGA, and thin quad flat pack (TQFP) packages (refer to Table 1–3 and Table 1–4). MAX II devices support vertical migration within the same package (for example, you can migrate between the EPM570, EPM1270, and EPM2210 devices in the 256-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins and JTAG pins are the same and power pins are subsets or supersets for a given package across device densities. The largest density in any package has the highest number of power pins; you must lay out for the largest planned density in a package to provide the necessary power pins for migration. For I/O pin migration across densities, cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins can be migrated. The Quartus® II software can automatically cross-reference and place all pins for you when given a device migration list.

 Table 1–3.
 MAX II Packages and User I/O Pins

Device	68-Pin Micro FineLine BGA <i>(1)</i>	100-Pin Micro FineLine BGA <i>(1)</i>	100-Pin FineLine BGA	100-Pin TQFP	144-Pin TQFP	144-Pin Micro FineLine BGA <i>(1)</i>	256-Pin Micro FineLine BGA <i>(1)</i>	256-Pin FineLine BGA	324-Pin FineLine BGA
EPM240	—	80	80	80	—	_	_	—	_
EPM240G									
EPM570	—	76	76	76	116	_	160	160	
EPM570G									
EPM1270	—	_	—	—	116	_	212	212	_
EPM1270G									
EPM2210	—	—	—	—	—	—	—	204	272
EPM2210G									
EPM240Z	54	80	_	_	—	_	_	—	
EPM570Z	—	76	—	_	—	116	160	_	_

Note to Table 1-3:

(1) Packages available in lead-free versions only.

Table 1-4. MAX II TQFP, FineLine BGA, and Micro FineLine BGA Package Sizes

Package	68-Pin Micro FineLine BGA	100-Pin Micro FineLine BGA	100-Pin FineLine BGA	100-Pin TQFP	144-Pin TQFP	144-Pin Micro FineLine BGA	256-Pin Micro FineLine BGA	256-Pin FineLine BGA	324-Pin FineLine BGA
Pitch (mm)	0.5	0.5	1	0.5	0.5	0.5	0.5	1	1
Area (mm2)	25	36	121	256	484	49	121	289	361
Length × width (mm × mm)	5 × 5	6 × 6	11 × 11	16 × 16	22 × 22	7×7	11 × 11	17 × 17	19 × 19

Table 1–6. Document Revision History

Date and Revision	Changes Made	Summary of Changes
June 2005, version 1.3	Updated timing numbers in Table 1-1.	_
December 2004, version 1.2	Updated timing numbers in Table 1-1.	_
June 2004, version 1.1	 Updated timing numbers in Table 1-1. 	

Table 2–1.	MAX II	Device	Resources
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			LAB		
Devices	UFM Blocks	LAB Columns	Long LAB Rows	Short LAB Rows (Width) <i>(1)</i>	Total LABs
EPM240	1	6	4	—	24
EPM570	1	12	4	3 (3)	57
EPM1270	1	16	7	3 (5)	127
EPM2210	1	20	10	3 (7)	221

Note to Table 2–1:

(1) The width is the number of LAB columns in length.

Figure 2–2 shows a floorplan of a MAX II device.





Note to Figure 2-2:

(1) The device shown is an EPM570 device. EPM1270 and EPM2210 devices have a similar floorplan with more LABs. For EPM240 devices, the CFM and UFM blocks are located on the left side of the device.



Figure 2–5. LAB-Wide Control Signals

Logic Elements

The smallest unit of logic in the MAX II architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry-select capability. A single LE also supports dynamic single-bit addition or subtraction mode selectable by an LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and DirectLink interconnects. See Figure 2–6.

Figure 2-6. MAX II LE



Each LE's programmable register can be configured for D, T, JK, or SR operation. Each register has data, true asynchronous load data, clock, clock enable, clear, and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any LE can drive the register's clock and clear control signals. Either general-purpose I/O pins or LEs can drive the clock enable, preset, asynchronous load, and asynchronous data. The asynchronous load data input comes from the data3 input of the LE. For combinational functions, the LUT output bypasses the register and drives directly to the LE outputs.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and DirectLink routing connections and one drives local interconnect resources. This allows the LUT to drive one output while the register drives another output. This register packing feature improves device utilization because the device can use the register and the LUT for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same LE so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

Normal Mode

The normal mode is suitable for general logic applications and combinational functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (see Figure 2–7). The Quartus II Compiler automatically selects the carry-in or the data3 signal as one of the inputs to the LUT. Each LE can use LUT chain connections to drive its combinational output directly to the next LE in the LAB. Asynchronous load data for the register comes from the data3 input of the LE. LEs in normal mode support packed registers.





Note to Figure 2-7:

(1) This signal is only allowed in normal mode if the LE is at the end of an adder/subtractor chain.

Dynamic Arithmetic Mode

The dynamic arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An LE in dynamic arithmetic mode uses four 2-input LUTs configurable as a dynamic adder/subtractor. The first two 2-input LUTs compute two summations based on a possible carry-in of 1 or 0; the other two LUTs generate carry outputs for the two chains of the carry-select circuitry. As shown in Figure 2–8, the LAB carry-in signal selects either the carry-in0 or carry-in1 chain. The selected chain's logic level in turn determines which parallel sum is generated as a combinational or registered output. For example, when implementing an adder, the sum output is the selection of two possible calculated sums:

```
data1 + data2 + carry in0
or
data1 + data2 + carry-in1
```

The other two LUTs use the data1 and data2 signals to generate two possible carry-out signals: one for a carry of 1 and the other for a carry of 0. The carry-in0 signal acts as the carry-select for the carry-out0 output and carry-in1 acts as the carry-select for the carry-out1 output. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The dynamic arithmetic mode also offers clock enable, counter enable, synchronous up/down control, synchronous clear, synchronous load, and dynamic adder/subtractor options. The LAB local interconnect data inputs generate the counter enable and synchronous up/down control signals. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs. The addnsub LAB-wide signal controls whether the LE acts as an adder or subtractor.

Figure 2–8. LE in Dynamic Arithmetic Mode



Note to Figure 2-8:

(1) The addnsub signal is tied to the carry input for the first LE of a carry chain only.

Carry-Select Chain

The carry-select chain provides a very fast carry-select function between LEs in dynamic arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 0 and carry-in of 1 in parallel. The carry-in0 and carry-in1 signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

The Quartus II software automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions. The Quartus II software creates carry chains longer than 10 LEs by linking adjacent LABs within the same row together automatically. A carry chain can extend horizontally up to one full LAB row, but does not extend between LAB rows.

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. MAX II devices support simultaneous preset/asynchronous load and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, MAX II devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals and uses its own dedicated routing resources (that is, it does not use any of the four global resources). Driving this signal low before or during power-up prevents user mode from releasing clears within the design. This allows you to control when clear is released on a device that has just been powered-up. If not set for its chip-wide reset function, the DEV_CLRn pin is a regular I/O pin.

By default, all registers in MAX II devices are set to power-up low. However, this power-up state can be set to high on individual registers during design entry using the Quartus II software.

MultiTrack Interconnect

In the MAX II architecture, connections between LEs, the UFM, and device I/O pins are provided by the MultiTrack interconnect structure. The MultiTrack interconnect consists of continuous, performance-optimized routing lines used for inter- and intradesign block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and short delays between logic levels instead of large delays associated with global or long routing lines. Dedicated row interconnects route signals to and from LABs within the same row. These row resources include:

- DirectLink interconnects between LABs
- R4 interconnects traversing four LABs to the right or left

The DirectLink interconnect allows an LAB to drive into the local interconnect of its left and right neighbors. The DirectLink interconnect provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.





MultiVolt Core

The MAX II architecture supports the MultiVolt core feature, which allows MAX II devices to support multiple V_{CC} levels on the V_{CCINT} supply. An internal linear voltage regulator provides the necessary 1.8-V internal voltage supply to the device. The voltage regulator supports 3.3-V or 2.5-V supplies on its inputs to supply the 1.8-V internal voltage to the device, as shown in Figure 2–18. The voltage regulator is not guaranteed for voltages that are between the maximum recommended 2.5-V operating voltage and the minimum recommended 3.3-V operating voltage.

The MAX IIG and MAX IIZ devices use external 1.8-V supply. The 1.8-V V_{cc} external supply powers the device core directly.





Table 2–4 describes the I/O standards supported by MAX II devices.

Table 2-4.	MAX II I/O	Standards
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I/O Standard	Туре	Output Supply Voltage (VCCIO) (V)
3.3-V LVTTL/LVCMOS	Single-ended	3.3
2.5-V LVTTL/LVCMOS	Single-ended	2.5
1.8-V LVTTL/LVCMOS	Single-ended	1.8
1.5-V LVCMOS	Single-ended	1.5
3.3-V PCI (1)	Single-ended	3.3

Note to Table 2-4:

(1) The 3.3-V PCI compliant I/O is supported in Bank 3 of the EPM1270 and EPM2210 devices.

The EPM240 and EPM570 devices support two I/O banks, as shown in Figure 2–22. Each of these banks support all the LVTTL and LVCMOS standards shown in Table 2–4. PCI compliant I/O is not supported in these devices and banks.





Notes to Figure 2–22:

(1) Figure 2-22 is a top view of the silicon die.

(2) Figure 2-22 is a graphical representation only. Refer to the pin list and the Quartus II software for exact pin locations.

The EPM1270 and EPM2210 devices support four I/O banks, as shown in Figure 2–23. Each of these banks support all of the LVTTL and LVCMOS standards shown in Table 2–4. PCI compliant I/O is supported in Bank 3. Bank 3 supports the PCI clamping diode on inputs and PCI drive compliance on outputs. You must use Bank 3 for designs requiring PCI compliant I/O pins. The Quartus II software automatically places I/O pins in this bank if assigned with the PCI I/O standard.





I/O Bank 4

Notes to Figure 2-23:

(1) Figure 2–23 is a top view of the silicon die.

(2) Figure 2–23 is a graphical representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Each I/O bank has dedicated V_{CCIO} pins that determine the voltage standard support in that bank. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each individual bank can support a different standard. Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3 V, Bank 3 can support LVTTL, LVCMOS, and 3.3-V PCI. V_{CCIO} powers both the input and output buffers in MAX II devices.

The JTAG pins for MAX II devices are dedicated pins that cannot be used as regular I/O pins. The pins TMS, TDI, TDO, and TCK support all the I/O standards shown in Table 2–4 on page 2–27 except for PCI. These pins reside in Bank 1 for all MAX II devices and their I/O standard support is controlled by the V_{CCIO} setting for Bank 1.

PCI Compliance

The MAX II EPM1270 and EPM2210 devices are compliant with PCI applications as well as all 3.3-V electrical specifications in the *PCI Local Bus Specification Revision* 2.2. These devices are also large enough to support PCI intellectual property (IP) cores. Table 2–5 shows the MAX II device speed grades that meet the PCI timing specifications.

Bus Hold

Each MAX II device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. The designer can select this feature individually for each I/O pin. The bus-hold output will drive no higher than $V_{\rm CCIO}$ to prevent overdriving signals. If the bus-hold feature is enabled, the device cannot use the programmable pull-up option.

The bus-hold circuitry uses a resistor to pull the signal level to the last driven state. The *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* gives the specific sustaining current for each V_{CCIO} voltage level driven through this resistor and overdrive current used to identify the next-driven input level.

The bus-hold circuitry is only active after the device has fully initialized. The bus-hold circuit captures the value on the pin present at the moment user mode is entered.

Programmable Pull-Up Resistor

Each MAX II device I/O pin provides an optional programmable pull-up resistor during user mode. If the designer enables this feature for an I/O pin, the pull-up resistor holds the output to the V_{CCIO} level of the output pin's bank.

P

The programmable pull-up resistor feature should not be used at the same time as the bus-hold feature on a given I/O pin.

Programmable Input Delay

The MAX II IOE includes a programmable input delay that is activated to ensure zero hold times. A path where a pin directly drives a register, with minimal routing between the two, may require the delay to ensure zero hold time. However, a path where a pin drives a register through long routing or through combinational logic may not require the delay to achieve a zero hold time. The Quartus II software uses this delay to ensure zero hold times when needed.

MultiVolt I/O Interface

The MAX II architecture supports the MultiVolt I/O interface feature, which allows MAX II devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation (V_{CCINT}), and up to four sets for input buffers and I/O output driver buffers (V_{CCIO}), depending on the number of I/O banks available in the devices where each set of VCC pins powers one I/O bank. The EPM240 and EPM570 devices have two I/O banks respectively while the EPM1270 and EPM2210 devices have four I/O banks respectively.

4. Hot Socketing and Power-On Reset in MAX II Devices

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Introduction

MAX[®] II devices offer hot socketing, also known as hot plug-in or hot swap, and power sequencing support. Designers can insert or remove a MAX II board in a system during operation without undesirable effects to the system bus. The hot socketing feature removes some of the difficulties designers face when using components on printed circuit boards (PCBs) that contain a mixture of 3.3-, 2.5-, 1.8-, and 1.5-V devices.

The MAX II device hot socketing feature provides:

- Board or device insertion and removal
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter contains the following sections:

- "MAX II Hot-Socketing Specifications" on page 4–1
- "Power-On Reset Circuitry" on page 4–5

MAX II Hot-Socketing Specifications

MAX II devices offer all three of the features required for the hot-socketing capability listed above without any external components or special design requirements. The following are hot-socketing specifications:

- The device can be driven before and during power-up or power-down without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.
- Signal pins do not drive the V_{CCIO} or V_{CCINT} power supplies. External input signals to device I/O pins do not power the device V_{CCIO} or V_{CCINT} power supplies via internal paths. This is true if the V_{CCINT} and the V_{CCIO} supplies are held at GND.

Devices Can Be Driven before Power-Up

Signals can be driven into the MAX II device I/O pins and GCLK[3..0] pins before or during power-up or power-down without damaging the device. MAX II devices support any power-up or power-down sequence (V_{CCIO1} , V_{CCIO2} , V_{CCIO3} , V_{CCIO4} , V_{CCINT}), simplifying the system-level design.

Power-Up Characteristics

When power is applied to a MAX II device, the POR circuit monitors V_{CCINT} and begins SRAM download at an approximate voltage of 1.7 V or 1.55 V for MAX IIG and MAX IIZ devices. From this voltage reference, SRAM download and entry into user mode takes 200 to 450 µs maximum, depending on device density. This period of time is specified as t_{CONFIG} in the power-up timing section of the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*.

Entry into user mode is gated by whether all V_{CCIO} banks are powered with sufficient operating voltage. If $V_{\text{CCIN}}T$ and V_{CCIO} are powered simultaneously, the device enters user mode within the t_{CONFIG} specifications. If V_{CCIO} is powered more than t_{CONFIG} after V_{CCINT} , the device does not enter user mode until 2 μ s after all V_{CCIO} banks are powered.

For MAX II and MAX IIG devices, when in user mode, the POR circuitry continues to monitor the V_{CCINT} (but not V_{CCIO}) voltage level to detect a brown-out condition. If there is a V_{CCINT} voltage sag at or below 1.4 V during user mode, the POR circuit resets the SRAM and tri-states the I/O pins. Once V_{CCINT} rises back to approximately 1.7 V (or 1.55 V for MAX IIG devices), the SRAM download restarts and the device begins to operate after t_{CONFIG} time has passed.

For MAX IIZ devices, the POR circuitry does not monitor the V_{CCINT} and V_{CCIO} voltage levels after the device enters user mode. If there is a V_{CCINT} voltage sag below 1.4 V during user mode, the functionality of the device will not be guaranteed and you must power down the V_{CCINT} to 0 V for a minimum of 10 µs before powering the V_{CCINT} and V_{CCIO} up again. Once V_{CCINT} rises from 0 V back to approximately 1.55 V, the SRAM download restarts and the device begins to operate after t_{CONFIG} time has passed.

Figure 4–5 shows the voltages for POR of MAX II, MAX IIG, and MAX IIZ devices during power-up into user mode and from user mode to power-down or brown-out.

 $\label{eq:linear} \begin{tabular}{ll} \hline \end{tabular} \end{tabular} All \ V_{\text{CCINT}} \ and \ V_{\text{CCINT}} \ pins \ of \ all \ banks \ must \ be \ powered \ on \ MAX \ II \ devices \ before \ entering \ user \ mode. \end{tabular}$

5–6	

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{OH}	High-level output voltage	$V_{ccio} = 3.0,$ IOH = -0.1 mA (1)	$V_{\text{ccio}} - 0.2$	—	V
V _{OL}	Low-level output voltage	$V_{ccio} = 3.0,$ IOL = 0.1 mA (1)	_	0.2	V

Table 5-6. 3.3-V LVCMOS Specifications (Part 2 of 2)

Table 5-7. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{CCIO}	I/O supply voltage	—	2.375	2.625	V
VIH	High-level input voltage	—	1.7	4.0	V
VIL	Low-level input voltage	_	-0.5	0.7	V
V _{OH}	High-level output voltage	IOH = -0.1 mA (1)	2.1		V
		IOH = -1 mA (1)	2.0	_	V
		IOH = -2 mA (1)	1.7	—	V
Vol	Low-level output voltage	IOL = 0.1 mA (1)		0.2	V
		IOL = 1 mA (1)		0.4	V
		IOL = 2 mA (1)		0.7	V

Table 5-8. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{ccio}	I/O supply voltage	—	1.71	1.89	V
V _{IH}	High-level input voltage		$0.65 \times V_{cc10}$	2.25 <i>(2)</i>	V
VIL	Low-level input voltage		-0.3	$0.35 \times V_{ccio}$	V
V _{OH}	High-level output voltage	IOH = -2 mA (1)	$V_{\text{ccio}} - 0.45$		V
VOL	Low-level output voltage	IOL = 2 mA (1)		0.45	V

Table 5-9. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{ccio}	I/O supply voltage	—	1.425	1.575	V
VIH	High-level input voltage		$0.65 \times V_{ccio}$	V _{ccio} + 0.3 <i>(2)</i>	V
VIL	Low-level input voltage		-0.3	$0.35 \times V_{ccio}$	V
V _{OH}	High-level output voltage	IOH = -2 mA (1)	$0.75 \times V_{ccio}$		V
VOL	Low-level output voltage	IOL = 2 mA <i>(1)</i>	—	$0.25 \times V_{ccio}$	V

Notes to Table 5–5 through Table 5–9:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the MAX II Architecture chapter (I/O Structure section) in the MAX II Device Handbook.

(2) This maximum V_{IH} reflects the JEDEC specification. The MAX II input buffer can tolerate a V_{IH} maximum of 4.0, as specified by the V_{I} parameter in Table 5–2.

Figure 5-2. MAX II Device Timing Model



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters.

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Refer to the *Understanding Timing in MAX II Devices* chapter in the *MAX II Device Handbook* for more information.

This section describes and specifies the performance, internal, external, and UFM timing specifications. All specifications are representative of the worst-case supply voltage and junction temperature conditions.

Preliminary and Final Timing

Timing models can have either preliminary or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. Table 5–13 shows the status of the MAX II device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under the worst-case voltage and junction temperature conditions.

Device	Preliminary	Final
EPM240	—	\checkmark
EPM240Z (1)	—	\checkmark
EPM570	_	\checkmark
EPM570Z (1)		\checkmark

Table 5-13. MAX II Device Timing Model Status (Part 1 of 2)

Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Table 5–15 through Table 5–22 describe the MAX II device internal timing microparameters for logic elements (LEs), input/output elements (IOEs), UFM blocks, and MultiTrack interconnects. The timing values for –3, –4, and –5 speed grades shown in Table 5–15 through Table 5–22 are based on an EPM1270 device target, while –6, –7, and –8 speed grade values are based on an EPM570Z device target.

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• For more explanations and descriptions about each internal timing microparameters symbol, refer to the *Understanding Timing in MAX II Devices* chapter in the *MAX II Device Handbook*.

Table 5–15. LE Internal Timing Microparameters

		MAX II / MAX IIG					MAX IIZ							
			–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		Speed rade	–8 Speed Grade		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t _{lut}	LE combinational LUT delay	_	571	-	742	_	914	-	1,215		2,247	_	2,247	ps
t _{сомв}	Combinational path delay	-	147	-	192	_	236	-	243	—	305	—	309	ps
t _{clr}	LE register clear delay	238	_	309	—	381	_	401	—	541	—	545		ps
t _{PRE}	LE register preset delay	238	_	309	—	381	_	401	—	541	—	545		ps
t _{su}	LE register setup time before clock	208	_	271	—	333	_	260	—	319	—	321		ps
t _H	LE register hold time after clock	0	-	0	_	0	_	0	_	0	_	0		ps
t _{co}	LE register clock- to-output delay	-	235	-	305	_	376	-	380	—	489	_	494	ps
t _{clkhl}	Minimum clock high or low time	166	-	216	—	266	_	253	—	335	-	339	_	ps
t _c	Register control delay	—	857	—	1,114	—	1,372	—	1,356		1,722	_	1,741	ps





Figure 5–5. UFM Erase Waveform



MAX II / MAX IIG							MAX IIZ						
	–3 S Gr	-3 Speed -4 Speed -5 Speed Grade Grade Grade		Speed rade	–6 Speed Grade		–7 Speed Grade		–8 Speed Grade				
Routing	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t _{c4}	—	429	—	556	—	687	—	(1)	—	(1)	—	(1)	ps
t _{R4}	_	326	—	423	_	521	—	(1)	_	(1)	_	(1)	ps
t _{local}	—	330	—	429	_	529	—	(1)	—	(1)		(1)	ps

Table 5-22.	Routing	Delay	Internal	Timing	Microparameters
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Note to Table 5-22:

(1) The numbers will only be available in a later revision.

			MAX II / MAX IIG							MA	X IIZ				
			-3 S Gi	–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		Speed ade	–7 Speed Grade		–8 Speed Grade		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
f _{cnt}	Maximum global clock frequency for 16-bit counter	—		304.0 <i>(1)</i>		247.5		201.1		184.1		123.5		118.3	MHz

Table 5–24. EPM570 Global Clock External I/O Timing Parameters (Part 2 of 2)

Note to Table 5-24:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5–25 shows the external I/O timing parameters for EPM1270 devices.

Table 5-25. EPM1270 Global Clock External I/O Timing Parameters

			MAX II / MAX IIG						
			–3 Sp	–3 Speed Grade –4 Speed Grade		–5 Speed Grade			
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Unit
t _{PD1}	Worst case pin-to-pin delay through 1 look-up table (LUT)	10 pF		6.2		8.1	_	10.0	ns
t _{PD2}	Best case pin-to-pin delay through 1 LUT	10 pF	_	3.7	_	4.8	—	5.9	ns
t _{su}	Global clock setup time	—	1.2	—	1.5		1.9	—	ns
t _H	Global clock hold time	—	0	—	0		0	—	ns
t _{co}	Global clock to output delay	10 pF	2.0	4.6	2.0	5.9	2.0	7.3	ns
t _{ch}	Global clock high time	—	166	—	216		266	—	ps
t _{cL}	Global clock low time	—	166	—	216	—	266	_	ps
t _{cnt}	Minimum global clock period for 16-bit counter	_	3.3	_	4.0		5.0	_	ns
f _{cnt}	Maximum global clock frequency for 16-bit counter	_		304.0 (1)	_	247.5	_	201.1	MHz

Note to Table 5-25:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Document Revision History

Table 5–35 shows the revision history for this chapter.

Table 5-35. Document Revision History (Part 1 of 2)

Date and Revision	Changes Made	Summary of Changes			
August 2009, version 2.5	 Added Table 5–28, Table 5–29, and Table 5–30. Updated Table 5–2, Table 5–4, Table 5–14, Table 5–15, Table 5–16, Table 5–17, Table 5–18, Table 5–19, Table 5–20, Table 5–21, Table 5–22, Table 5–23, Table 5–24, Table 5–27, Table 5–31, Table 5–32, and Table 5–33. 	Added information for speed grade –8			
November 2008, version 2.4	 Updated Table 5–2. Updated "Internal Timing Parameters" section. 	_			
October 2008, version 2.3	 Updated New Document Format. Updated Figure 5–1. 				
July 2008, version 2.2	■ Updated Table 5–14 , Table 5–23 , and Table 5–24.	_			
March 2008, version 2.1	Added (Note 5) to Table 5–4.	_			
December 2007, version 2.0	 Updated (Note 3) and (4) to Table 5–1. Updated Table 5–2 and added (Note 5). Updated ICCSTANDBY and ICCPOWERUP information and added IPULLUP information in Table 5–4. Added (Note 1) to Table 5–10. Updated Figure 5–2. Added (Note 1) to Table 5–13. Updated Table 5–13 through Table 5–24, and Table 5–27 through Table 5–30. Added tCOMB information to Table 5–15. Updated Figure 5–6. Added "Referenced Documents" section. 	Updated document with MAX IIZ information.			
December 2006, version 1.8	 Added note to Table 5–1. Added document revision history. 	_			
July 2006, version 1.7	 Minor content and table updates. 	—			
February 2006, version 1.6	 Updated "External Timing I/O Delay Adders" section. Updated Table 5–29. Updated Table 5–30. 	_			
November 2005, version 1.5	■ Updated Tables 5-2, 5-4, and 5-12.	_			
August 2005, version 1.4	 Updated Figure 5-1. Updated Tables 5-13, 5-16, and 5-26. Removed Note 1 from Table 5-12. 				