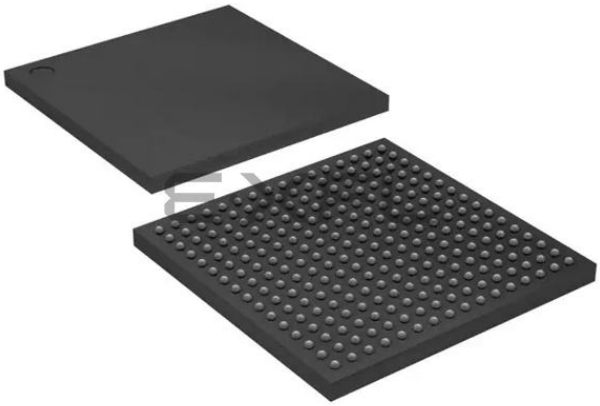

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.4 ns
Voltage Supply - Internal	2.5V, 3.3V
Number of Logic Elements/Blocks	570
Number of Macrocells	440
Number of Gates	-
Number of I/O	160
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm570f256i5

MAX II devices are available in space-saving FineLine BGA, Micro FineLine BGA, and thin quad flat pack (TQFP) packages (refer to Table 1–3 and Table 1–4). MAX II devices support vertical migration within the same package (for example, you can migrate between the EPM570, EPM1270, and EPM2210 devices in the 256-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins and JTAG pins are the same and power pins are subsets or supersets for a given package across device densities. The largest density in any package has the highest number of power pins; you must lay out for the largest planned density in a package to provide the necessary power pins for migration. For I/O pin migration across densities, cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins can be migrated. The Quartus® II software can automatically cross-reference and place all pins for you when given a device migration list.

Table 1–3. MAX II Packages and User I/O Pins

Device	68-Pin Micro FineLine BGA *(1)*	100-Pin Micro FineLine BGA *(1)*	100-Pin FineLine BGA	100-Pin TQFP	144-Pin TQFP	144-Pin Micro FineLine BGA *(1)*	256-Pin Micro FineLine BGA *(1)*	256-Pin FineLine BGA	324-Pin FineLine BGA
EPM240 EPM240G	—	80	80	80	—	—	—	—	—
EPM570 EPM570G	—	76	76	76	116	—	160	160	—
EPM1270 EPM1270G	—	—	—	—	116	—	212	212	—
EPM2210 EPM2210G	—	—	—	—	—	—	—	204	272
EPM240Z	54	80	—	—	—	—	—	—	—
EPM570Z	—	76	—	—	—	116	160	—	—

Note to Table 1–3:

(1) Packages available in lead-free versions only.

Table 1–4. MAX II TQFP, FineLine BGA, and Micro FineLine BGA Package Sizes

Package	68-Pin Micro FineLine BGA	100-Pin Micro FineLine BGA	100-Pin FineLine BGA	100-Pin TQFP	144-Pin TQFP	144-Pin Micro FineLine BGA	256-Pin Micro FineLine BGA	256-Pin FineLine BGA	324-Pin FineLine BGA
Pitch (mm)	0.5	0.5	1	0.5	0.5	0.5	0.5	1	1
Area (mm2)	25	36	121	256	484	49	121	289	361
Length × width (mm × mm)	5 × 5	6 × 6	11 × 11	16 × 16	22 × 22	7 × 7	11 × 11	17 × 17	19 × 19

The Quartus II software automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions. The Quartus II software creates carry chains longer than 10 LEs by linking adjacent LABs within the same row together automatically. A carry chain can extend horizontally up to one full LAB row, but does not extend between LAB rows.

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. MAX II devices support simultaneous preset/asynchronous load and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, MAX II devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals and uses its own dedicated routing resources (that is, it does not use any of the four global resources). Driving this signal low before or during power-up prevents user mode from releasing clears within the design. This allows you to control when clear is released on a device that has just been powered-up. If not set for its chip-wide reset function, the DEV_CLRn pin is a regular I/O pin.

By default, all registers in MAX II devices are set to power-up low. However, this power-up state can be set to high on individual registers during design entry using the Quartus II software.

MultiTrack Interconnect

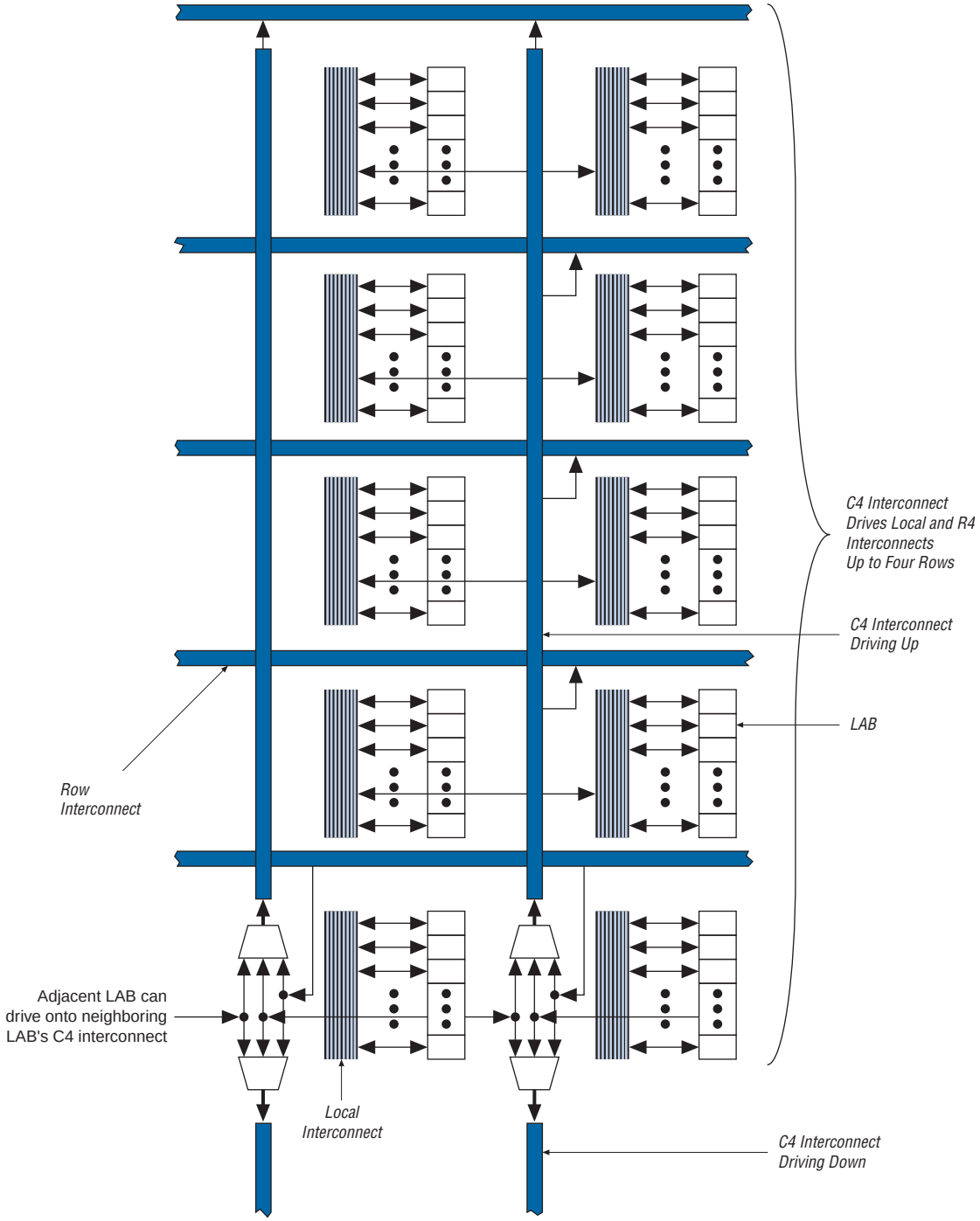
In the MAX II architecture, connections between LEs, the UFM, and device I/O pins are provided by the MultiTrack interconnect structure. The MultiTrack interconnect consists of continuous, performance-optimized routing lines used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and short delays between logic levels instead of large delays associated with global or long routing lines. Dedicated row interconnects route signals to and from LABs within the same row. These row resources include:

- DirectLink interconnects between LABs
- R4 interconnects traversing four LABs to the right or left

The DirectLink interconnect allows an LAB to drive into the local interconnect of its left and right neighbors. The DirectLink interconnect provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.

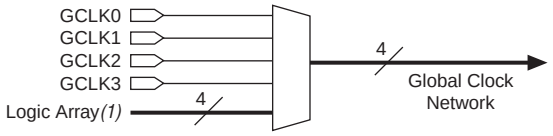
Figure 2–12. C4 Interconnect Connections *(Note 1)*



Note to Figure 2–12:

(1) Each C4 interconnect can drive either up or down four rows.

Figure 2–13. Global Clock Generation



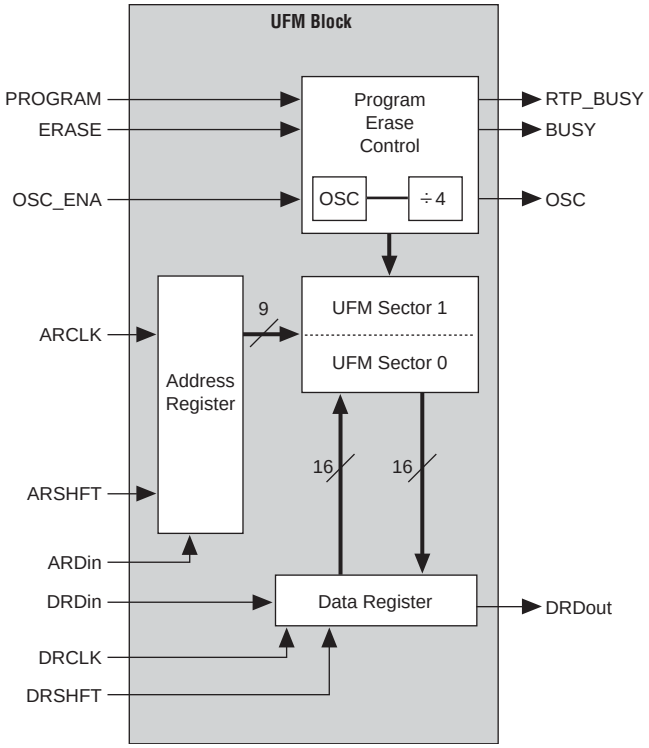
Note to Figure 2–13:

(1) Any I/O pin can use a MultiTrack interconnect to route as a logic array-generated global clock signal.

The global clock network drives to individual LAB column signals, LAB column clocks [3..0], that span an entire LAB column from the top to the bottom of the device. Unused global clocks or control signals in a LAB column are turned off at the LAB column clock buffers shown in Figure 2–14. The LAB column clocks [3..0] are multiplexed down to two LAB clock signals and one LAB clear signal. Other control signal types route from the global clock network into the LAB local interconnect. See "LAB Control Signals" on page 2–5 for more information.

- Auto-increment addressing
- Serial interface to logic array with programmable interface

Figure 2–15. UFM Block and Interface Signals



UFM Storage

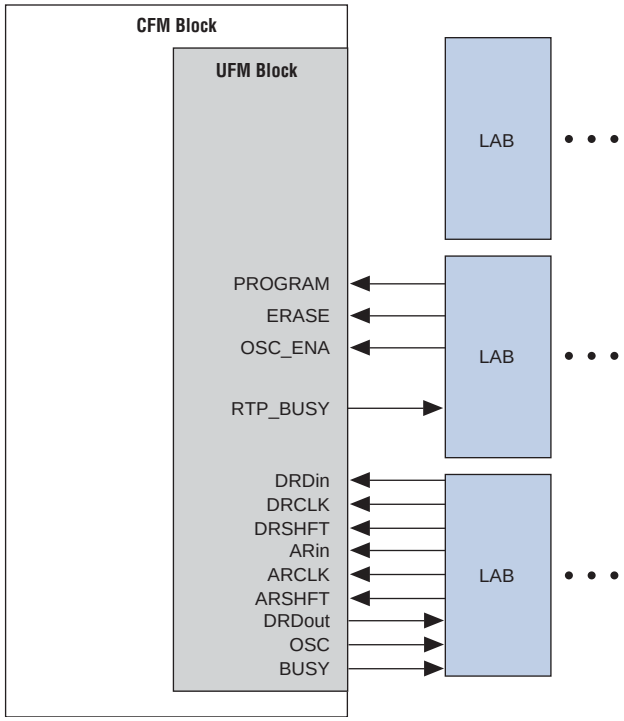
Each device stores up to 8,192 bits of data in the UFM block. Table 2–3 shows the data size, sector, and address sizes for the UFM block.

Table 2–3. UFM Array Size

Device	Total Bits	Sectors	Address Bits	Data Width
EPM240 EPM570 EPM1270 EPM2210	8,192	2 (4,096 bits/sector)	9	16

There are 512 locations with 9-bit addressing ranging from `000h` to `1FFh`. Sector 0 address space is `000h` to `0FFh` and Sector 1 address space is from `100h` to `1FFh`. The data width is up to 16 bits of data. The Quartus II software automatically creates logic to accommodate smaller read or program data widths. Erasure of the UFM involves individual sector erasing (that is, one erase of sector 0 and one erase of sector 1 is required to erase the entire UFM block). Since sector erase is required before a program or write, having two sectors enables a sector size of data to be left untouched while the other sector is erased and programmed with new data.

Figure 2–16. EPM240 UFM Block LAB Row Interface *(Note 1)*



Note to Figure 2–16:

(1) The UFM block inputs and outputs can drive to/from all types of interconnects, not only DirectLink interconnects from adjacent row LABs.

Table 2–4 describes the I/O standards supported by MAX II devices.

Table 2–4. MAX II I/O Standards

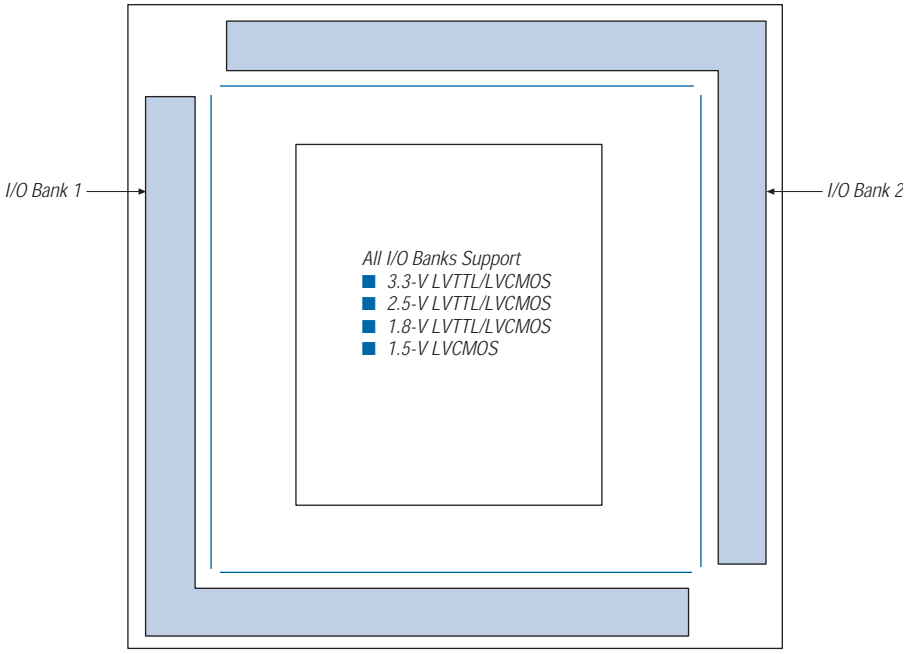
I/O Standard	Type	Output Supply Voltage (VCCIO) (V)
3.3-V LVTTL/LVCMOS	Single-ended	3.3
2.5-V LVTTL/LVCMOS	Single-ended	2.5
1.8-V LVTTL/LVCMOS	Single-ended	1.8
1.5-V LVCMOS	Single-ended	1.5
3.3-V PCI *(1)*	Single-ended	3.3

Note to Table 2–4:

(1) The 3.3-V PCI compliant I/O is supported in Bank 3 of the EPM1270 and EPM2210 devices.

The EPM240 and EPM570 devices support two I/O banks, as shown in Figure 2–22. Each of these banks support all the LVTTL and LVCMOS standards shown in Table 2–4. PCI compliant I/O is not supported in these devices and banks.

Figure 2–22. MAX II I/O Banks for EPM240 and EPM570 *(Note 1)*, *(2)*



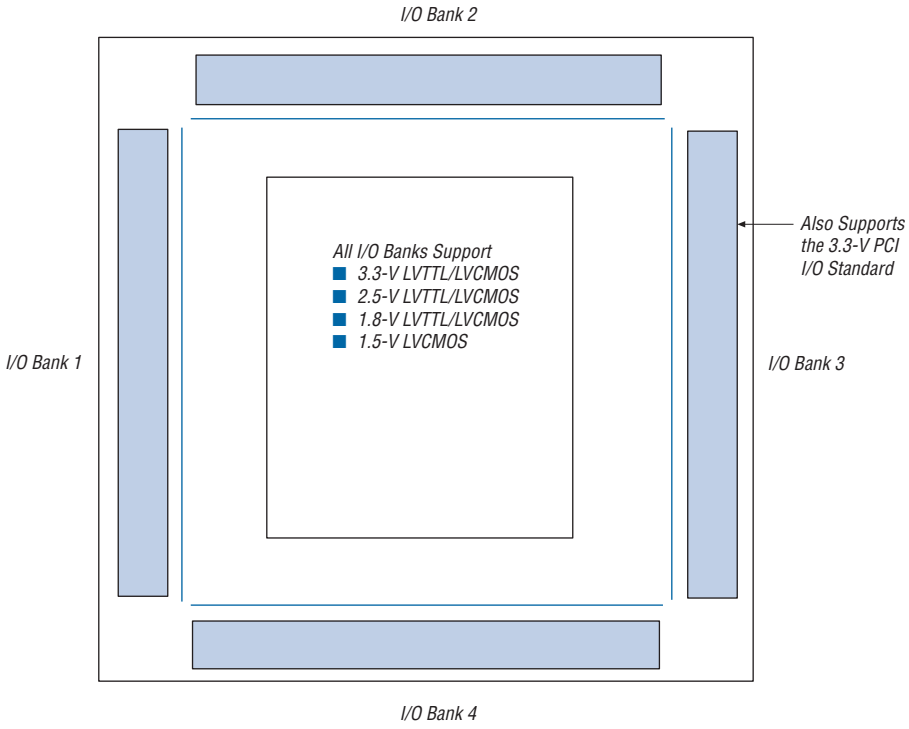
Notes to Figure 2–22:

(1) Figure 2–22 is a top view of the silicon die.

(2) Figure 2–22 is a graphical representation only. Refer to the pin list and the Quartus II software for exact pin locations.

The EPM1270 and EPM2210 devices support four I/O banks, as shown in Figure 2–23. Each of these banks support all of the LVTTL and LVCMOS standards shown in Table 2–4. PCI compliant I/O is supported in Bank 3. Bank 3 supports the PCI clamping diode on inputs and PCI drive compliance on outputs. You must use Bank 3 for designs requiring PCI compliant I/O pins. The Quartus II software automatically places I/O pins in this bank if assigned with the PCI I/O standard.

Figure 2–23. MAX II I/O Banks for EPM1270 and EPM2210 *(Note 1), (2)*



Notes to Figure 2–23:

(1) Figure 2–23 is a top view of the silicon die.

(2) Figure 2–23 is a graphical representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Each I/O bank has dedicated V_{CCIO} pins that determine the voltage standard support in that bank. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each individual bank can support a different standard. Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3 V, Bank 3 can support LVTTL, LVCMOS, and 3.3-V PCI. V_{CCIO} powers both the input and output buffers in MAX II devices.

The JTAG pins for MAX II devices are dedicated pins that cannot be used as regular I/O pins. The pins `TMS`, `TDI`, `TDO`, and `TCK` support all the I/O standards shown in Table 2–4 on page 2–27 except for PCI. These pins reside in Bank 1 for all MAX II devices and their I/O standard support is controlled by the V_{CCIO} setting for Bank 1.

PCI Compliance

The MAX II EPM1270 and EPM2210 devices are compliant with PCI applications as well as all 3.3-V electrical specifications in the *PCI Local Bus Specification Revision 2.2*. These devices are also large enough to support PCI intellectual property (IP) cores. Table 2–5 shows the MAX II device speed grades that meet the PCI timing specifications.

Table 2–5. MAX II Devices and Speed Grades that Support 3.3-V PCI Electrical Specifications and Meet PCI Timing

Device	33-MHz PCI	66-MHz PCI
EPM1270	All Speed Grades	–3 Speed Grade
EPM2210	All Speed Grades	–3 Speed Grade

Schmitt Trigger

The input buffer for each MAX II device I/O pin has an optional Schmitt trigger setting for the 3.3-V and 2.5-V standards. The Schmitt trigger allows input buffers to respond to slow input edge rates with a fast output edge rate. Most importantly, Schmitt triggers provide hysteresis on the input buffer, preventing slow-rising noisy input signals from ringing or oscillating on the input signal driven into the logic array. This provides system noise tolerance on MAX II inputs, but adds a small, nominal input delay.

The JTAG input pins (TMS, TCK, and TDI) have Schmitt trigger buffers that are always enabled.

The TCK input is susceptible to high pulse glitches when the input signal fall time is greater than 200 ns for all I/O standards.

Output Enable Signals

Each MAX II IOE output buffer supports output enable signals for tri-state control. The output enable signal can originate from the GCLK[3..0] global signals or from the MultiTrack interconnect. The MultiTrack interconnect routes output enable signals and allows for a unique output enable for each output or bidirectional pin.

MAX II devices also provide a chip-wide output enable pin (DEV_OE) to control the output enable for every output pin in the design. An option set before compilation in the Quartus II software controls this pin. This chip-wide output enable uses its own routing resources and does not use any of the four global resources. If this option is turned on, all outputs on the chip operate normally when DEV_OE is asserted. When the pin is deasserted, all outputs are tri-stated. If this option is turned off, the DEV_OE pin is disabled when the device operates in user mode and is available as a user I/O pin.

Programmable Drive Strength

The output buffer for each MAX II device I/O pin has two levels of programmable drive strength control for each of the LVTTL and LVCMOS I/O standards. Programmable drive strength provides system noise reduction control for high performance I/O designs. Although a separate slew-rate control feature exists, using the lower drive strength setting provides signal slew-rate control to reduce system noise and signal overshoot without the large delay adder associated with the slew-rate control feature. Table 2–6 shows the possible settings for the I/O standards with drive strength control. The Quartus II software uses the maximum current strength as the default setting. The PCI I/O standard is always set at 20 mA with no alternate setting.

IEEE 1532 Support

The JTAG circuitry and ISP instruction set in MAX II devices is compliant to the IEEE 1532-2002 programming specification. This provides industry-standard hardware and software for in-system programming among multiple vendor programmable logic devices (PLDs) in a JTAG chain.

The MAX II 1532 BSDL files will be released on the Altera website when available.

Jam Standard Test and Programming Language (STAPL)

The Jam STAPL JEDEC standard, JESD71, can be used to program MAX II devices with in-circuit testers, PCs, or embedded processors. The Jam byte code is also supported for MAX II devices. These software programming protocols provide a compact embedded solution for programming MAX II devices.

For more information, refer to the *Using Jam STAPL for ISP via an Embedded Processor* chapter in the *MAX II Device Handbook*.

Programming Sequence

During in-system programming, 1532 instructions, addresses, and data are shifted into the MAX II device through the `TDI` input pin. Data is shifted out through the `TDO` output pin and compared against the expected data. Programming a pattern into the device requires the following six ISP steps. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6. These steps are automatically executed by third-party programmers, the Quartus II software, or the Jam STAPL and Jam Byte-Code Players.

1. *Enter ISP*—The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode.
2. *Check ID*—Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Sector Erase*—Erasing the device in-system involves shifting in the instruction to erase the device and applying an erase pulse(s). The erase pulse is automatically generated internally by waiting in the run/test/idle state for the specified erase pulse time of 500 ms for the CFM block and 500 ms for each sector of the UFM block.
4. *Program*—Programming the device in-system involves shifting in the address, data, and program instruction and generating the program pulse to program the flash cells. The program pulse is automatically generated internally by waiting in the run/test/idle state for the specified program pulse time of 75 µs. This process is repeated for each address in the CFM and UFM blocks.
5. *Verify*—Verifying a MAX II device in-system involves shifting in addresses, applying the verify instruction to generate the read pulse, and shifting out the data for comparison. This process is repeated for each CFM and UFM address.
6. *Exit ISP*—An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode.

Table 3–4 shows the programming times for MAX II devices using in-circuit testers to execute the algorithm vectors in hardware. Software-based programming tools used with download cables are slightly slower because of data processing and transfer limitations.

Table 3–4. MAX II Device Family Programming Times

Description	EPM240 EPM240G EPM240Z	EPM570 EPM570G EPM570Z	EPM1270 EPM1270G	EPM2210 EPM2210G	Unit
Erase + Program (1 MHz)	1.72	2.16	2.90	3.92	sec
Erase + Program (10 MHz)	1.65	1.99	2.58	3.40	sec
Verify (1 MHz)	0.09	0.17	0.30	0.49	sec
Verify (10 MHz)	0.01	0.02	0.03	0.05	sec
Complete Program Cycle (1 MHz)	1.81	2.33	3.20	4.41	sec
Complete Program Cycle (10 MHz)	1.66	2.01	2.61	3.45	sec

UFM Programming

The Quartus II software, with the use of POF, Jam, or JBC files, supports programming of the user flash memory (UFM) block independent of the logic array design pattern stored in the CFM block. This allows updating or reading UFM contents through ISP without altering the current logic array design, or vice versa. By default, these programming files and methods will program the entire flash memory contents, which includes the CFM block and UFM contents. The stand-alone embedded Jam STAPL player and Jam Byte-Code Player provides action commands for programming or reading the entire flash memory (UFM and CFM together) or each independently.

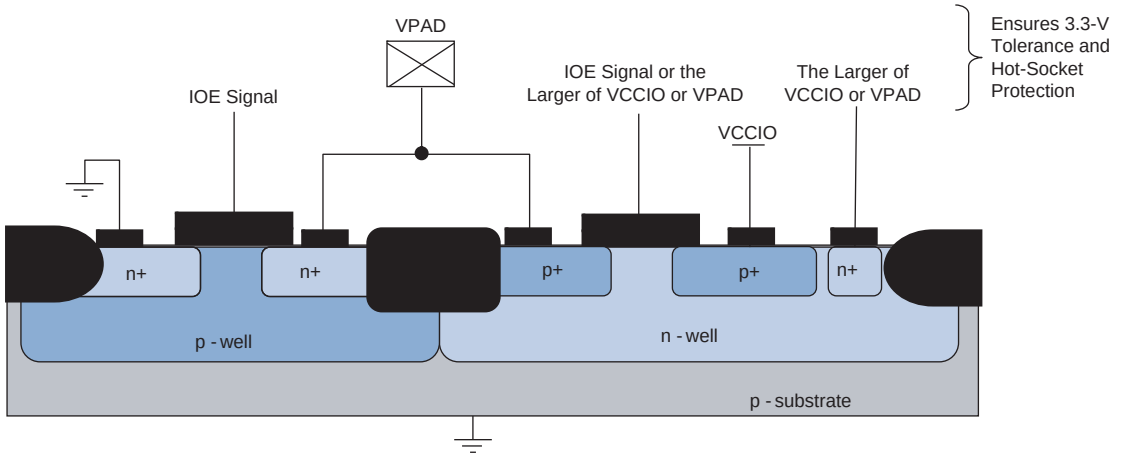
For more information, refer to the *Using Jam STAPL for ISP via an Embedded Processor* chapter in the *MAX II Device Handbook*.

In-System Programming Clamp

By default, the IEEE 1532 instruction used for entering ISP automatically tri-states all I/O pins with weak pull-up resistors for the duration of the ISP sequence. However, some systems may require certain pins on MAX II devices to maintain a specific DC logic level during an in-field update. For these systems, an optional in-system programming clamp instruction exists in MAX II circuitry to control I/O behavior during the ISP sequence. The in-system programming clamp instruction enables the device to sample and sustain the value on an output pin (an input pin would remain tri-stated if sampled) or to explicitly set a logic high, logic low, or tri-state value on any pin. Setting these options is controlled on an individual pin basis using the Quartus II software.

For more information, refer to the *Real-Time ISP and ISP Clamp for MAX II Devices* chapter in the *MAX II Device Handbook*.

Figure 4–2. Transistor-Level Diagram of MAX II Device I/O Buffers



The CMOS output drivers in the I/O pins intrinsically provide electrostatic discharge (ESD) protection. There are two cases to consider for ESD voltage strikes: positive voltage zap and negative voltage zap.

A positive ESD voltage zap occurs when a positive voltage is present on an I/O pin due to an ESD charge event. This can cause the N+ (Drain)/ P-Substrate junction of the N-channel drain to break down and the N+ (Drain)/P-Substrate/N+ (Source) intrinsic bipolar transistor turn on to discharge ESD current from I/O pin to GND. The dashed line (see Figure 4–3) shows the ESD current discharge path during a positive ESD zap.

Figure 4–3. ESD Protection During Positive Voltage Zap

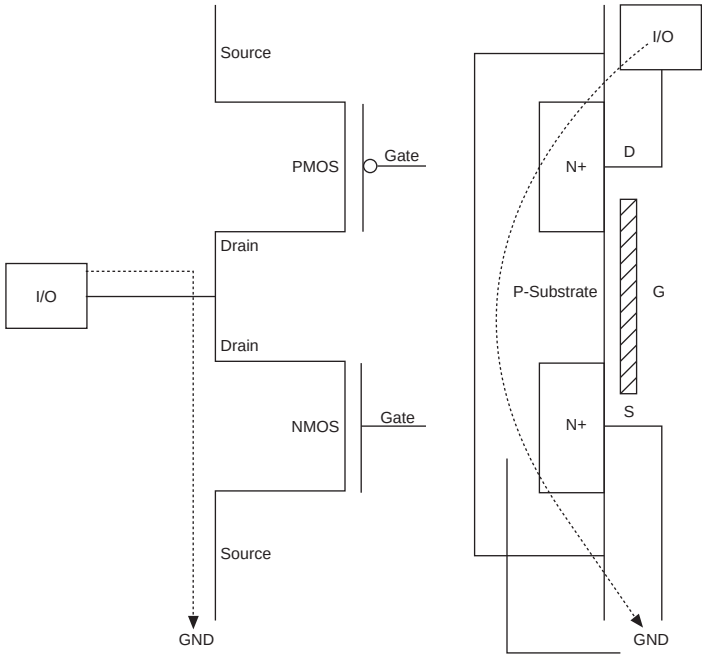


Table 5–4. MAX II Device DC Electrical Characteristics *(Note 1)* (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{PULLUP}	I/O pin pull-up resistor current when I/O is unprogrammed	—	—	—	300	µA
C_{IO}	Input capacitance for user I/O pin	—	—	—	8	pF
C_{GCLK}	Input capacitance for dual-purpose GCLK/user I/O pin	—	—	—	8	pF

Notes to Table 5–4:

(1) Typical values are for T_A = 25°C, V_{CCINT} = 3.3 or 2.5 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, or 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(3) V_I = ground, no load, no toggling inputs.

(4) Commercial temperature ranges from 0°C to 85°C with maximum current at 85°C.

(5) Industrial temperature ranges from –40°C to 100°C with maximum current at 100°C.

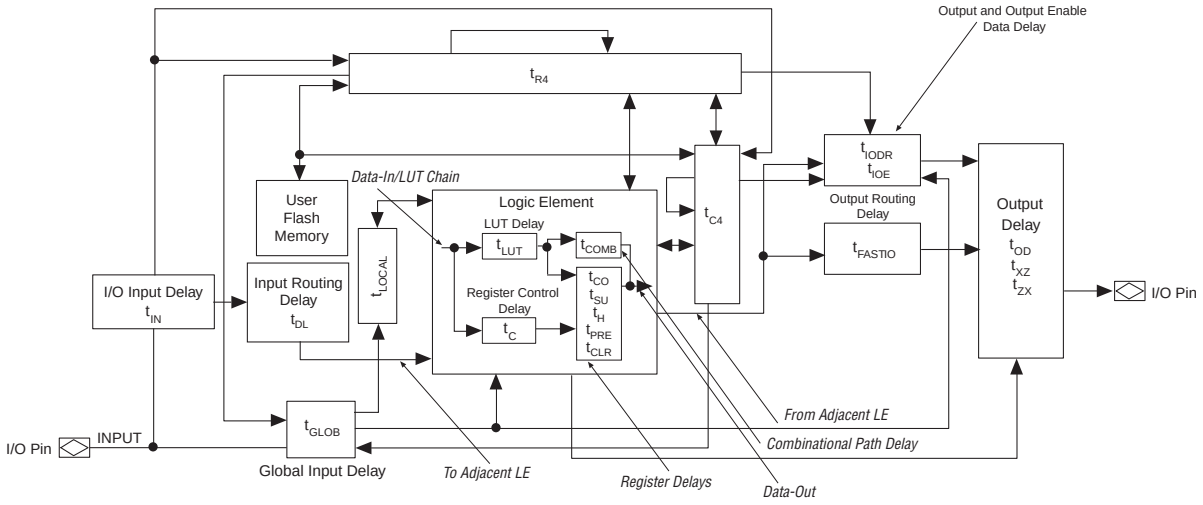
(6) This value applies to commercial and industrial range devices. For extended temperature range devices, the $V_{SCHMITT}$ typical value is 300 mV for V_{CCIO} = 3.3 V and 120 mV for V_{CCIO} = 2.5 V.

(7) The TCK input is susceptible to high pulse glitches when the input signal fall time is greater than 200 ns for all I/O standards.

(8) This is a peak current value with a maximum duration of t_{CONFIG} time.

(9) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.

Figure 5–2. MAX II Device Timing Model



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters.

Refer to the *Understanding Timing in MAX II Devices* chapter in the *MAX II Device Handbook* for more information.

This section describes and specifies the performance, internal, external, and UFM timing specifications. All specifications are representative of the worst-case supply voltage and junction temperature conditions.

Preliminary and Final Timing

Timing models can have either preliminary or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. Table 5–13 shows the status of the MAX II device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under the worst-case voltage and junction temperature conditions.

Table 5–13. MAX II Device Timing Model Status (Part 1 of 2)

Device	Preliminary	Final
EPM240	—	✓
EPM240Z *(1)*	—	✓
EPM570	—	✓
EPM570Z *(1)*	—	✓

Table 5–24. EPM570 Global Clock External I/O Timing Parameters (Part 2 of 2)

Symbol	Parameter	Condition	MAX II / MAX IIG						MAX IIZ						Unit
			–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	304.0 *(1)*	—	247.5	—	201.1	—	184.1	—	123.5	—	118.3	MHz

Note to Table 5–24:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5–25 shows the external I/O timing parameters for EPM1270 devices.

Table 5–25. EPM1270 Global Clock External I/O Timing Parameters

Symbol	Parameter	Condition	MAX II / MAX IIG						Unit
			–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through 1 look-up table (LUT)	10 pF	—	6.2	—	8.1	—	10.0	ns
t_{PD2}	Best case pin-to-pin delay through 1 LUT	10 pF	—	3.7	—	4.8	—	5.9	ns
t_{SU}	Global clock setup time	—	1.2	—	1.5	—	1.9	—	ns
t_{H}	Global clock hold time	—	0	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	4.6	2.0	5.9	2.0	7.3	ns
t_{CH}	Global clock high time	—	166	—	216	—	266	—	ps
t_{CL}	Global clock low time	—	166	—	216	—	266	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	3.3	—	4.0	—	5.0	—	ns
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	304.0 *(1)*	—	247.5	—	201.1	MHz

Note to Table 5–25:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5–27. External Timing Input Delay Adders (Part 2 of 2)

I/O Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVCMOS	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	334	—	434	—	535	—	387	—	434	—	442	ps
2.5-V LVTTL / LVCMOS	Without Schmitt Trigger	—	23	—	30	—	37	—	42	—	43	—	43	ps
	With Schmitt Trigger	—	339	—	441	—	543	—	429	—	476	—	483	ps
1.8-V LVTTL / LVCMOS	Without Schmitt Trigger	—	291	—	378	—	466	—	378	—	373	—	373	ps
1.5-V LVCMOS	Without Schmitt Trigger	—	681	—	885	—	1,090	—	681	—	622	—	658	ps
3.3-V PCI	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	—	0	ps

Table 5–28. External Timing Input Delay t_{GLOB} Adders for GCLK Pins

I/O Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	308	—	400	—	493	—	387	—	434	—	442	ps
3.3-V LVCMOS	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	308	—	400	—	493	—	387	—	434	—	442	ps
2.5-V LVTTL / LVCMOS	Without Schmitt Trigger	—	21	—	27	—	33	—	42	—	43	—	43	ps
	With Schmitt Trigger	—	423	—	550	—	677	—	429	—	476	—	483	ps
1.8-V LVTTL / LVCMOS	Without Schmitt Trigger	—	353	—	459	—	565	—	378	—	373	—	373	ps
1.5-V LVCMOS	Without Schmitt Trigger	—	855	—	1,111	—	1,368	—	681	—	622	—	658	ps
3.3-V PCI	Without Schmitt Trigger	—	6	—	7	—	9	—	0	—	0	—	0	ps

Table 5–35. Document Revision History (Part 2 of 2)

Date and Revision	Changes Made	Summary of Changes
June 2005, version 1.3	■ Updated the R_{PULLUP} parameter in Table 5-4. ■ Added Note 2 to Tables 5-8 and 5-9. ■ Updated Table 5-13. ■ Added "Output Drive Characteristics" section. ■ Added I^2C mode and Notes 5 and 6 to Table 5-14. ■ Updated timing values to Tables 5-14 through 5-33.	—
December 2004, version 1.2	■ Updated timing Tables 5-2, 5-4, 5-12, and Tables 15-14 through 5-34. ■ Table 5-31 is new.	—
June 2004, version 1.1	■ Updated timing Tables 5-15 through 5-32.	—

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Software

MAX® II devices are supported by the Altera® Quartus® II design software with new, optional MAX+PLUS® II look and feel, which provides HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, and device programming. Refer to the Design Software Selector Guide for more details about the Quartus II software features.

The Quartus II software supports the Windows XP/2000/NT, Sun Solaris, Linux Red Hat v8.0, and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink interface.

Device Pin-Outs

Printed device pin-outs for MAX II devices are available on the Altera website (www.altera.com).

Ordering Information

Figure 6–1 describes the ordering codes for MAX II devices. For more information about a specific package, refer to the *Package Information* chapter in the *MAX II Device Handbook*.

Figure 6–1. MAX II Device Packaging Ordering Information