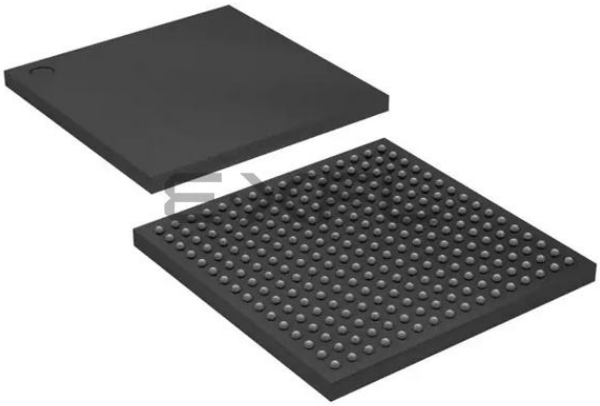

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.4 ns
Voltage Supply - Internal	1.71V ~ 1.89V
Number of Logic Elements/Blocks	570
Number of Macrocells	440
Number of Gates	-
Number of I/O	160
Operating Temperature	0°C ~ 85°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm570gf256c4

Table 1–1 shows the MAX II family features.

Table 1–1. MAX II Family Features

Feature	EPM240 EPM240G	EPM570 EPM570G	EPM1270 EPM1270G	EPM2210 EPM2210G	EPM240Z	EPM570Z
LEs	240	570	1,270	2,210	240	570
Typical Equivalent Macrocells	192	440	980	1,700	192	440
Equivalent Macrocell Range	128 to 240	240 to 570	570 to 1,270	1,270 to 2,210	128 to 240	240 to 570
UFM Size (bits)	8,192	8,192	8,192	8,192	8,192	8,192
Maximum User I/O pins	80	160	212	272	80	160
t_{PD1} (ns) *(1)*	4.7	5.4	6.2	7.0	7.5	9.0
f_{CNT} (MHz) *(2)*	304	304	304	304	152	152
t_{SU} (ns)	1.7	1.2	1.2	1.2	2.3	2.2
t_{CO} (ns)	4.3	4.5	4.6	4.6	6.5	6.7

Notes to Table 1–1:

(1) t_{PD1} represents a pin-to-pin delay for the worst case I/O placement with a full diagonal path across the device and combinational logic implemented in a single LUT and LAB that is adjacent to the output pin.

(2) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay will run faster than this number.

For more information about equivalent macrocells, refer to the *MAX II Logic Element to Macrocell Conversion Methodology* white paper.

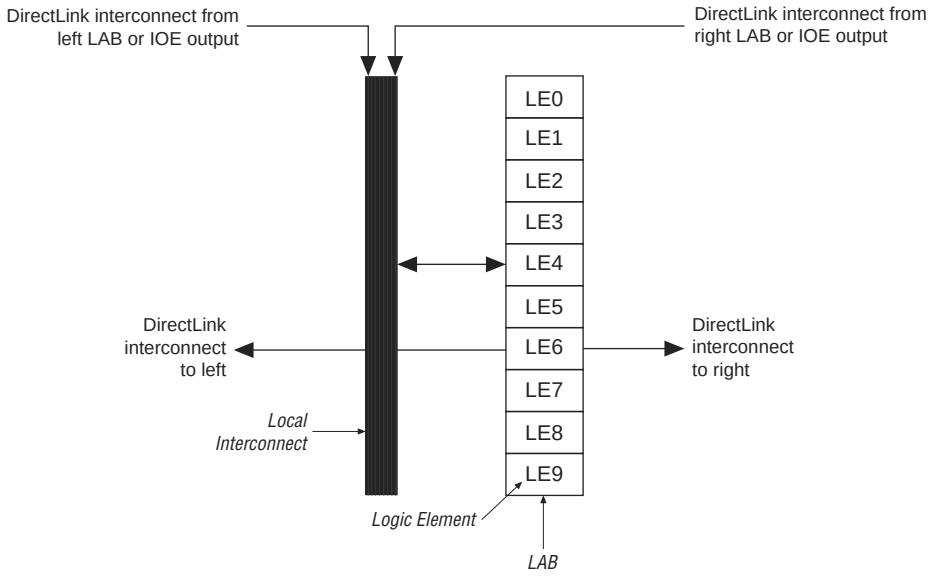
MAX II and MAX IIG devices are available in three speed grades: –3, –4, and –5, with –3 being the fastest. Similarly, MAX IIZ devices are available in three speed grades: –6, –7, and –8, with –6 being the fastest. These speed grades represent the overall relative performance, not any specific timing parameter. For propagation delay timing numbers within each speed grade and density, refer to the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*.

Table 1–2 shows MAX II device speed-grade offerings.

Table 1–2. MAX II Speed Grades

Device	Speed Grade					
	–3	–4	–5	–6	–7	–8
EPM240 EPM240G	✓	✓	✓	—	—	—
EPM570 EPM570G	✓	✓	✓	—	—	—
EPM1270 EPM1270G	✓	✓	✓	—	—	—
EPM2210 EPM2210G	✓	✓	✓	—	—	—
EPM240Z	—	—	—	✓	✓	✓
EPM570Z	—	—	—	✓	✓	✓

Figure 2–4. DirectLink Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, a synchronous clear, an asynchronous preset/load, a synchronous load, and add/subtract control signals, providing a maximum of 10 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. Deasserting the clock enable signal turns off the LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. By default, the Quartus II software uses a `NOT` gate push-back technique to achieve preset. If you disable the `NOT` gate push-back option or assign a given register to power-up high using the Quartus II software, the preset is then achieved using the asynchronous load signal with asynchronous load data input tied high.

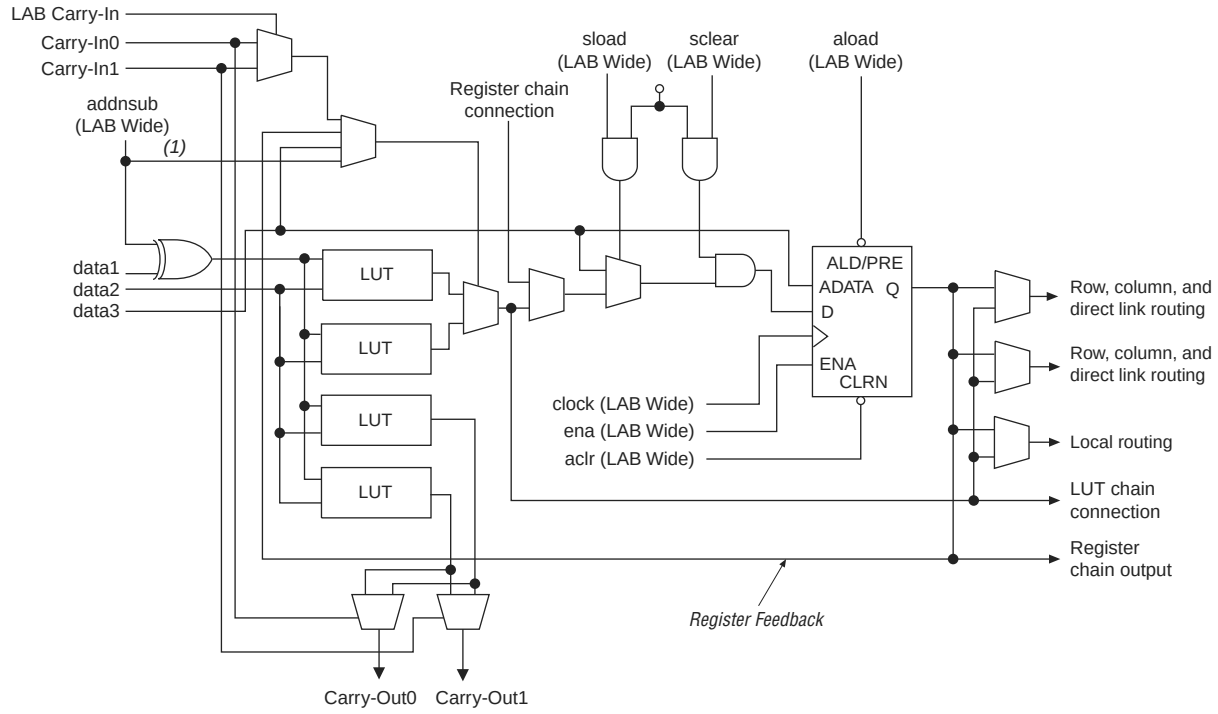
With the LAB-wide addnsub control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB column clocks [3..0], driven by the global clock network, and LAB local interconnect generate the LAB-wide control signals. The MultiTrack interconnect structure drives the LAB local interconnect for non-global control signal generation. The MultiTrack interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 2–5 shows the LAB control signal generation circuit.

The other two LUTs use the data1 and data2 signals to generate two possible carry-out signals: one for a carry of 1 and the other for a carry of 0. The `carry-in0` signal acts as the carry-select for the `carry-out0` output and `carry-in1` acts as the carry-select for the `carry-out1` output. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The dynamic arithmetic mode also offers clock enable, counter enable, synchronous up/down control, synchronous clear, synchronous load, and dynamic adder/subtractor options. The LAB local interconnect data inputs generate the counter enable and synchronous up/down control signals. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs. The addnsub LAB-wide signal controls whether the LE acts as an adder or subtractor.

Figure 2–8. LE in Dynamic Arithmetic Mode



Note to Figure 2–8:

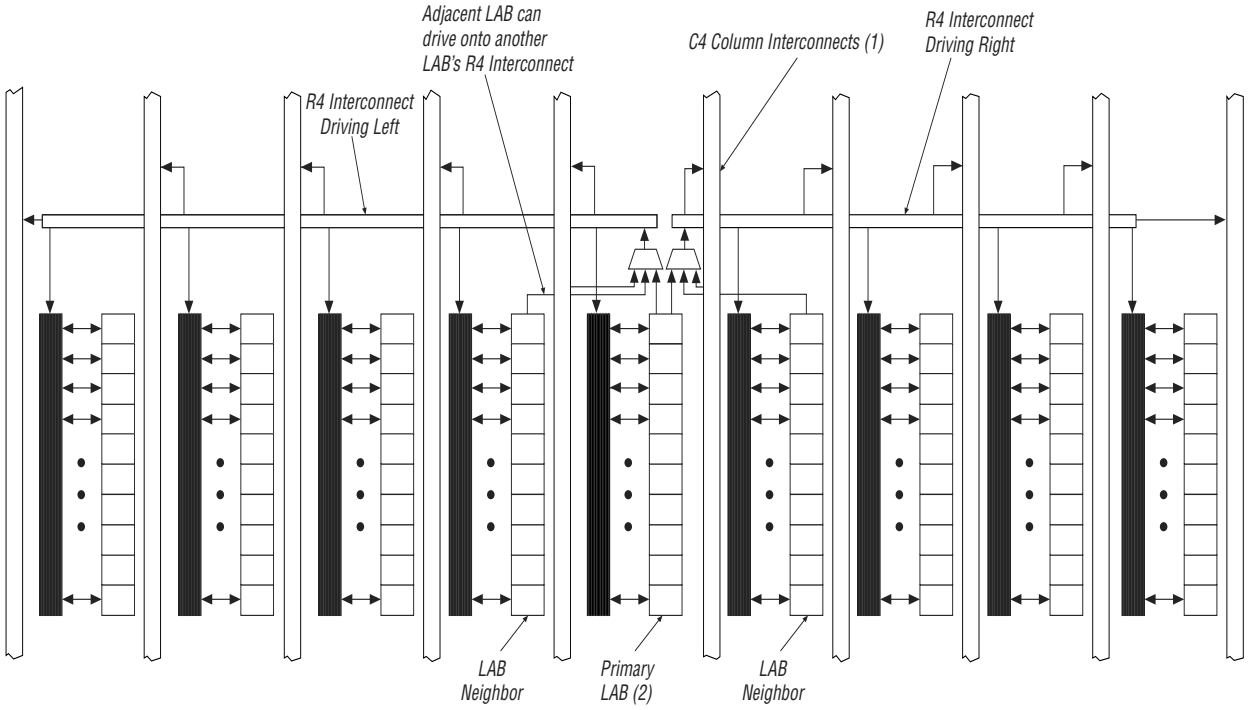
(1) The addnsub signal is tied to the carry input for the first LE of a carry chain only.

Carry-Select Chain

The carry-select chain provides a very fast carry-select function between LEs in dynamic arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 0 and carry-in of 1 in parallel. The `carry-in0` and `carry-in1` signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

The R4 interconnects span four LABs and are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–10 shows R4 interconnect connections from an LAB. R4 interconnects can drive and be driven by row IOEs. For LAB interfacing, a primary LAB or horizontal LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 interconnects for connections from one row to another.

Figure 2–10. R4 Interconnect Connections



Notes to Figure 2–10:

(1) C4 interconnects can drive R4 interconnects.

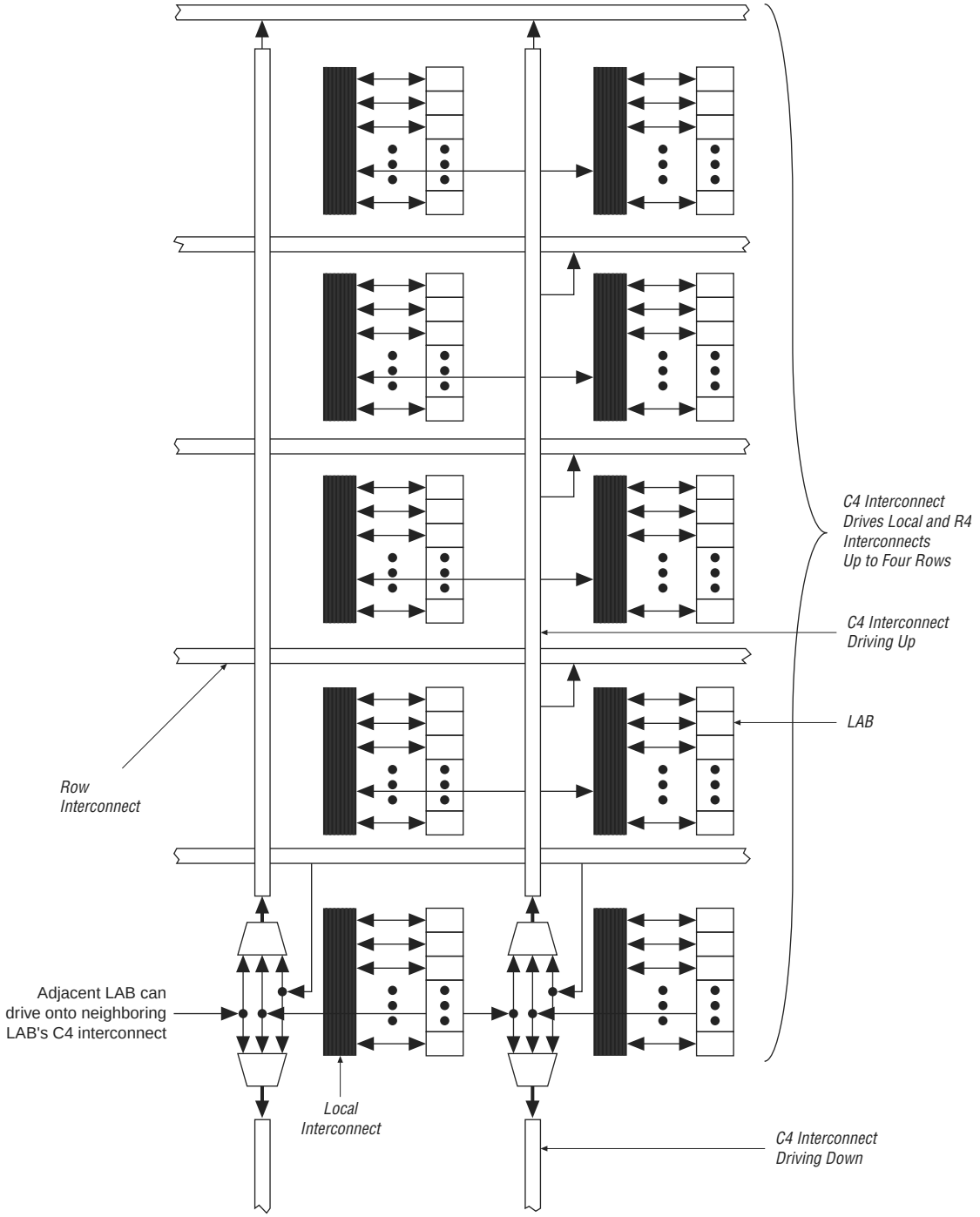
(2) This pattern is repeated for every LAB in the LAB row.

The column interconnect operates similarly to the row interconnect. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs and row and column IOEs. These column resources include:

- LUT chain interconnects within an LAB
- Register chain interconnects within an LAB
- C4 interconnects traversing a distance of four LABs in an up and down direction

MAX II devices include an enhanced interconnect structure within LABs for routing LE output to LE input connections faster using LUT chain connections and register chain connections. The LUT chain connection allows the combinational output of an LE to directly drive the fast input of the LE right below it, bypassing the local interconnect. These resources can be used as a high-speed connection for wide fan-in

Figure 2–12. C4 Interconnect Connections *(Note 1)*



Note to Figure 2–12:

(1) Each C4 interconnect can drive either up or down four rows.

The UFM block communicates with the logic array similar to LAB-to-LAB interfaces. The UFM block connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. This block also has DirectLink interconnects for fast connections to and from a neighboring LAB. For more information about the UFM interface to the logic array, see "User Flash Memory Block" on page 2–18.

Table 2–2 shows the MAX II device routing scheme.

Table 2–2. MAX II Device Routing Scheme

Source	Destination										
	LUT Chain	**Register Chain**	**Local *(1)***	**DirectLink *(1)***	**R4 *(1)***	**C4 *(1)***	**LE**	**UFM Block**	**Column IOE**	**Row IOE**	**Fast I/O *(1)***
LUT Chain	—	—	—	—	—	—	✓	—	—	—	—
Register Chain	—	—	—	—	—	—	✓	—	—	—	—
Local Interconnect	—	—	—	—	—	—	✓	✓	✓	✓	—
DirectLink Interconnect	—	—	✓	—	—	—	—	—	—	—	—
R4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
C4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
LE	✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓
UFM Block	—	—	✓	✓	✓	✓	—	—	—	—	—
Column IOE	—	—	—	—	—	✓	—	—	—	—	—
Row IOE	—	—	—	✓	✓	✓	—	—	—	—	—

Note to Table 2–2:

(1) These categories are interconnects.

Global Signals

Each MAX II device has four dual-purpose dedicated clock pins (`GCLK[3..0]`, two pins on the left side and two pins on the right side) that drive the global clock network for clocking, as shown in Figure 2–13. These four pins can also be used as general-purpose I/O if they are not used to drive the global clock network.

The four global clock lines in the global clock network drive throughout the entire device. The global clock network can provide clocks for all resources within the device including LEs, LAB local interconnect, IOEs, and the UFM block. The global clock lines can also be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, or protocol control signals such as `TRDY` and `IRDY` for PCI. Internal logic can drive the global clock network for internally-generated global clocks and control signals. Figure 2–13 shows the various sources that drive the global clock network.

I/O Structure

IOEs support many features, including:

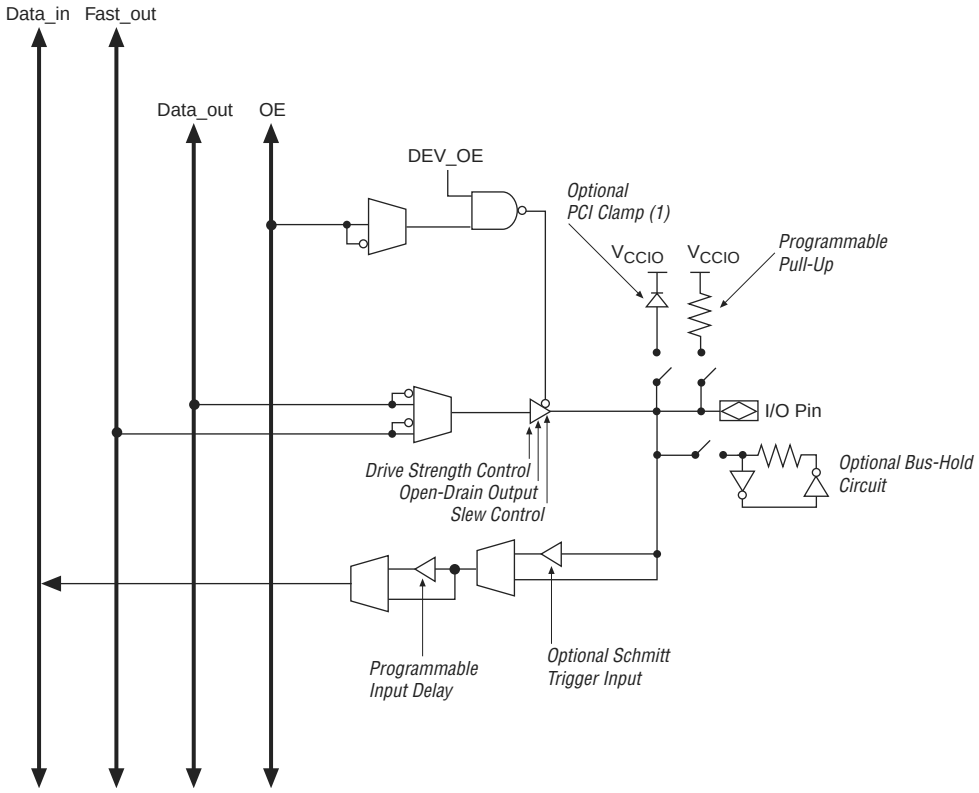
- LVTTL and LVCMOS I/O standards
- 3.3-V, 32-bit, 66-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Programmable drive strength control
- Weak pull-up resistors during power-up and in system programming
- Slew-rate control
- Tri-state buffers with individual output enable control
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Unique output enable per pin
- Open-drain outputs
- Schmitt trigger inputs
- Fast I/O connection
- Programmable input delay

MAX II device IOEs contain a bidirectional I/O buffer. Figure 2–19 shows the MAX II IOE structure. Registers from adjacent LABs can drive to or be driven from the IOE's bidirectional I/O buffers. The Quartus II software automatically attempts to place registers in the adjacent LAB with fast I/O connection to achieve the fastest possible clock-to-output and registered output enable timing. For input registers, the Quartus II software automatically routes the register to guarantee zero hold time. You can set timing assignments in the Quartus II software to achieve desired I/O timing.

Fast I/O Connection

A dedicated fast I/O connection from the adjacent LAB to the IOEs within an I/O block provides faster output delays for clock-to-output and t_{PD} propagation delays. This connection exists for data output signals, not output enable signals or input signals. Figure 2–20, Figure 2–21, and Figure 2–22 illustrate the fast I/O connection.

Figure 2–19. MAX II IOE Structure



Note to Figure 2–19:

(1) Available in EPM1270 and EPM2210 devices only.

I/O Blocks

The IOEs are located in I/O blocks around the periphery of the MAX II device. There are up to seven IOEs per row I/O block (5 maximum in the EPM240 device) and up to four IOEs per column I/O block. Each column or row I/O block interfaces with its adjacent LAB and MultiTrack interconnect to distribute signals throughout the device. The row I/O blocks drive row, column, or DirectLink interconnects. The column I/O blocks drive column interconnects.

Connect VCCIO pins to either a 1.5-V, 1.8 V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (that is, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems. Table 2–7 summarizes MAX II MultiVolt I/O support.

Table 2–7. MAX II MultiVolt I/O Support *(Note 1)*

	Input Signal					Output Signal				
VCCIO (V)	**1.5 V**	**1.8 V**	**2.5 V**	**3.3 V**	**5.0 V**	**1.5 V**	**1.8 V**	**2.5 V**	**3.3 V**	**5.0 V**
1.5	✓	✓	✓	✓	—	✓	—	—	—	—
1.8	✓	✓	✓	✓	—	✓ *(2)*	✓	—	—	—
2.5	—	—	✓	✓	—	✓ *(3)*	✓ *(3)*	✓	—	—
3.3	—	—	✓ *(4)*	✓	✓ *(5)*	✓ *(6)*	✓ *(6)*	✓ *(6)*	✓	✓ *(7)*

Notes to Table 2–7:

(1) To drive inputs higher than V_{CCIO} but less than 4.0 V including the overshoot, disable the I/O clamp diode. However, to drive 5.0-V inputs to the device, enable the I/O clamp diode to prevent V_I from rising above 4.0 V.

(2) When V_{CCIO} = 1.8 V, a MAX II device can drive a 1.5-V device with 1.8-V tolerant inputs.

(3) When V_{CCIO} = 2.5 V, a MAX II device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.

(4) When V_{CCIO} = 3.3 V and a 2.5-V input signal feeds an input pin, the VCCIO supply current will be slightly larger than expected.

(5) MAX II devices can be 5.0-V tolerant with the use of an external resistor and the internal I/O clamp diode on the EPM1270 and EPM2210 devices.

(6) When V_{CCIO} = 3.3 V, a MAX II device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

(7) When V_{CCIO} = 3.3 V, a MAX II device can drive a device with 5.0-V TTL inputs but not 5.0-V CMOS inputs. In the case of 5.0-V CMOS, open-drain setting with internal I/O clamp diode (available only on EPM1270 and EPM2210 devices) and external resistor is required.

For information about output pin source and sink current guidelines, refer to the *AN 428: MAX II CPLD Design Guidelines*.

Referenced Documents

This chapter referenced the following documents:

- *AN 428: MAX II CPLD Design Guidelines*
- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *Hot Socketing and Power-On Reset in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Using User Flash Memory in MAX II Devices* chapter in the *MAX II Device Handbook*

Document Revision History

Table 3–5 shows the revision history for this chapter.

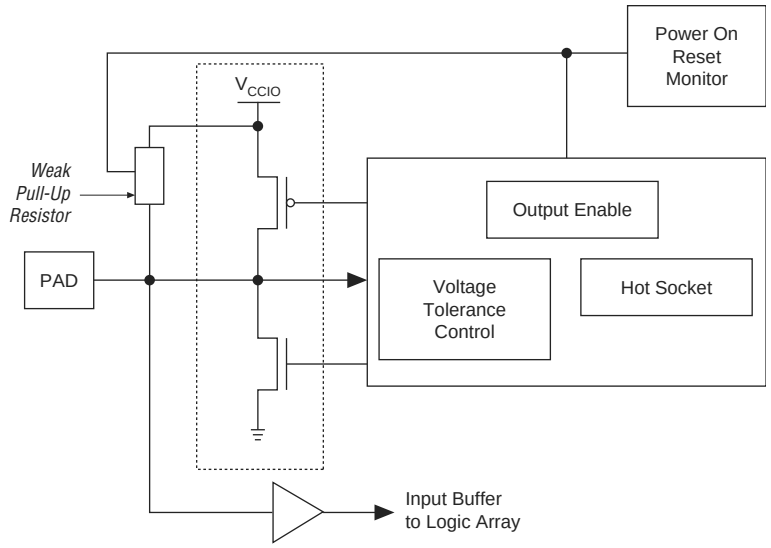
Table 3–5. Document Revision History

Date and Revision	Changes Made	Summary of Changes
October 2008, version 1.6	■ Updated New Document Format.	—
December 2007, version 1.5	■ Added warning note after Table 3–1. ■ Updated Table 3–3 and Table 3–4. ■ Added "Referenced Documents" section.	—
December 2006, version 1.4	■ Added document revision history.	—
June 2005, version 1.3	■ Added text and Table 3-4.	—
June 2005, version 1.3	■ Updated text on pages 3-5 to 3-8.	—
June 2004, version 1.1	■ Corrected Figure 3-1. Added CFM acronym.	—

☞ Make sure that the V_{CCINT} is within the recommended operating range even though SRAM download has completed.

Each I/O and clock pin has the circuitry shown in Figure 4–1.

Figure 4–1. Hot Socketing Circuit Block Diagram for MAX II Devices

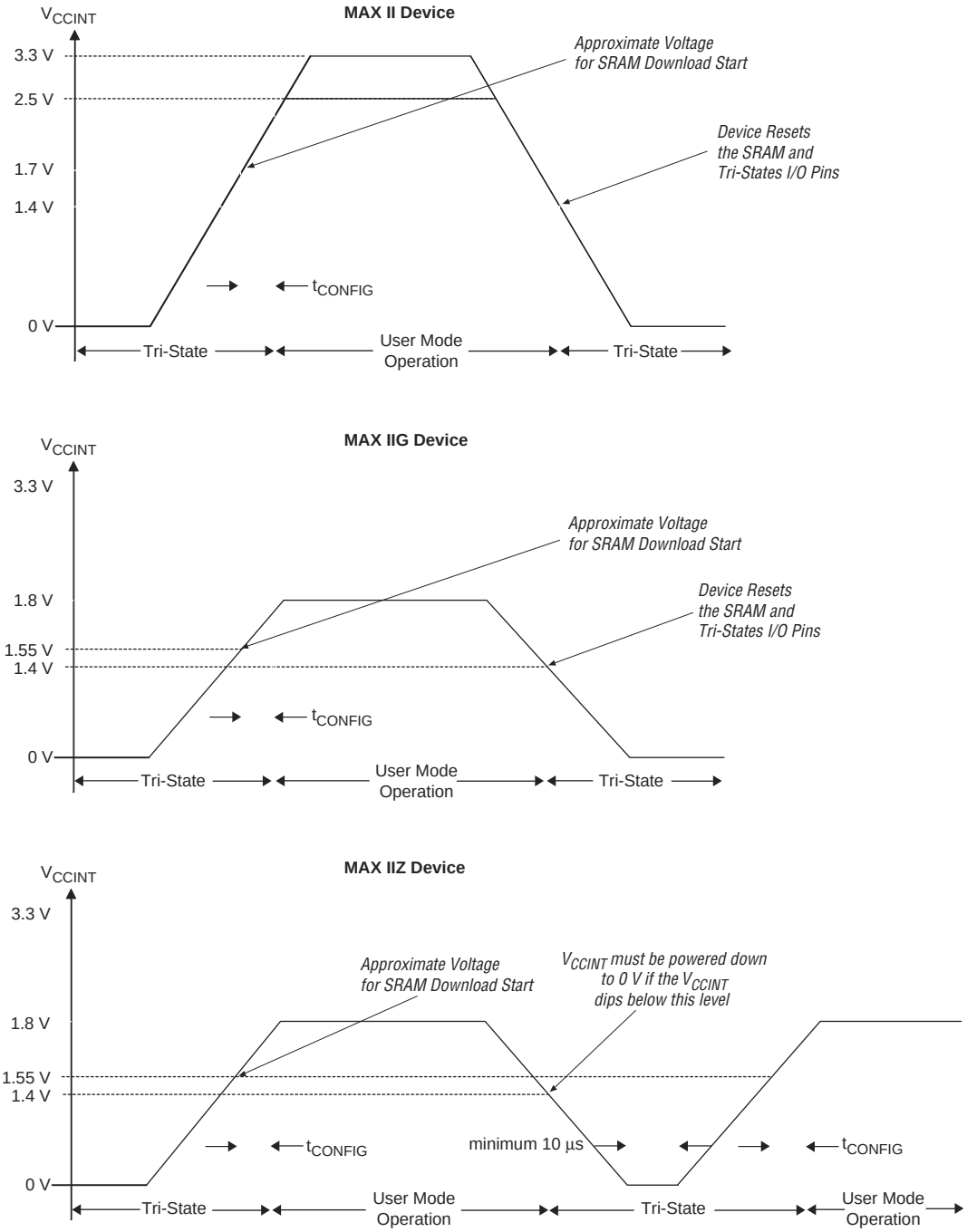


The POR circuit monitors V_{CCINT} and V_{CCIO} voltage levels and keeps I/O pins tri-stated until the device has completed its flash memory configuration of the SRAM logic. The weak pull-up resistor (R) from the I/O pin to V_{CCIO} is enabled during download to keep the I/O pins from floating. The 3.3-V tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO} and/or V_{CCINT} are powered, and it prevents the I/O pins from driving out when the device is not fully powered or operational. The hot socket circuit prevents I/O pins from internally powering V_{CCIO} and V_{CCINT} when driven by external signals before the device is powered.

For information about 5.0-V tolerance, refer to the *Using MAX II Devices in Multi-Voltage Systems* chapter in the *MAX II Device Handbook*.

Figure 4–2 shows a transistor-level cross section of the MAX II device I/O buffers. This design ensures that the output buffers do not drive when V_{CCIO} is powered before V_{CCINT} or if the I/O pad voltage is higher than V_{CCIO}. This also applies for sudden voltage spikes during hot insertion. The V_{PAD} leakage current charges the 3.3-V tolerant circuit capacitance.

Figure 4–5. Power-Up Characteristics for MAX II, MAX IIG, and MAX IIZ Devices *(Note 1), (2)*



Notes to Figure 4–5:

(1) Time scale is relative.

(2) Figure 4–5 assumes all V_{CCIO} banks power up simultaneously with the V_{CCINT} profile shown. If not, t_{CONFIG} stretches out until all V_{CCIO} banks are powered.

☞ After SRAM configuration, all registers in the device are cleared and released into user function before I/O tri-states are released. To release clears after tri-states are released, use the DEV_CLRn pin option. To hold the tri-states beyond the power-up configuration time, use the DEV_OE pin option.

Recommended Operating Conditions

Table 5–2 shows the MAX II device family recommended operating conditions.

Table 5–2. MAX II Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT} *(1)*	3.3-V supply voltage for internal logic and ISP	MAX II devices	3.00	3.60	V
	2.5-V supply voltage for internal logic and ISP	MAX II devices	2.375	2.625	V
	1.8-V supply voltage for internal logic and ISP	MAX IIG and MAX IIZ devices	1.71	1.89	V
V_{CCIO} *(1)*	Supply voltage for I/O buffers, 3.3-V operation	—	3.00	3.60	V
	Supply voltage for I/O buffers, 2.5-V operation	—	2.375	2.625	V
	Supply voltage for I/O buffers, 1.8-V operation	—	1.71	1.89	V
	Supply voltage for I/O buffers, 1.5-V operation	—	1.425	1.575	V
V_I	Input voltage	*(2)*, *(3)*, *(4)*	–0.5	4.0	V
V_O	Output voltage	—	0	V_{CCIO}	V
T_J	Operating junction temperature	Commercial range	0	85	°C
		Industrial range	–40	100	°C
		Extended range *(5)*	–40	125	°C

Notes to Table 5–2:

(1) MAX II device in-system programming and/or user flash memory (UFM) programming via JTAG or logic array is not guaranteed outside the recommended operating conditions (for example, if brown-out occurs in the system during a potential write/program sequence to the UFM, users are recommended to read back UFM contents and verify against the intended write data).

(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

(3) During transitions, the inputs may overshoot to the voltages shown in the following table based upon input duty cycle. The DC case is equivalent to 100% duty cycle. For more information about 5.0-V tolerance, refer to the *Using MAX II Devices in Multi-Voltage Systems* chapter in the *MAX II Device Handbook*.

V_{IN}	Max. Duty Cycle
4.0 V	100% (DC)
4.1	90%
4.2	50%
4.3	30%
4.4	17%
4.5	10%

(4) All pins, including clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(5) For the extended temperature range of 100 to 125° C, MAX II UFM programming (erase/write) is only supported via the JTAG interface. UFM programming via the logic array interface is not guaranteed in this range.

Programming/Erasure Specifications

Table 5–3 shows the MAX II device family programming/erasure specifications.

Table 5–3. MAX II Device Programming/Erasure Specifications

Parameter	Minimum	Typical	Maximum	Unit
Erase and reprogram cycles	—	—	100 *(1)*	Cycles

Note to Table 5–3:

(1) This specification applies to the UFM and configuration flash memory (CFM) blocks.

DC Electrical Characteristics

Table 5–4 shows the MAX II device family DC electrical characteristics.

Table 5–4. MAX II Device DC Electrical Characteristics *(Note 1)* (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIO}$ max to 0 V *(2)*	–10	—	10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIO}$ max to 0 V *(2)*	–10	—	10	µA
$I_{CCSTANDBY}$	V_{CCINT} supply current (standby) *(3)*	MAX II devices	—	12	—	mA
		MAX IIG devices	—	2	—	mA
		EPM240Z (Commercial grade) *(4)*	—	25	90	µA
		EPM240Z (Industrial grade) *(5)*	—	25	139	µA
		EPM570Z (Commercial grade) *(4)*	—	27	96	µA
		EPM570Z (Industrial grade) *(5)*	—	27	152	µA
$V_{SCHMITT}$ *(6)*	Hysteresis for Schmitt trigger input *(7)*	V_{CCIO} = 3.3 V	—	400	—	mV
		V_{CCIO} = 2.5 V	—	190	—	mV
$I_{CCPOWERUP}$	V_{CCINT} supply current during power-up *(8)*	MAX II devices	—	55	—	mA
		MAX IIG and MAX IIZ devices	—	40	—	mA
R_{PULLUP}	Value of I/O pin pull-up resistor during user mode and in-system programming	V_{CCIO} = 3.3 V *(9)*	5	—	25	kΩ
		V_{CCIO} = 2.5 V *(9)*	10	—	40	kΩ
		V_{CCIO} = 1.8 V *(9)*	25	—	60	kΩ
		V_{CCIO} = 1.5 V *(9)*	45	—	95	kΩ

Table 5–6. 3.3-V LVCMOS Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, IOH = –0.1 mA *(1)*	V_{CCIO} – 0.2	—	V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, IOL = 0.1 mA *(1)*	—	0.2	V

Table 5–7. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	2.375	2.625	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.5	0.7	V
V_{OH}	High-level output voltage	IOH = –0.1 mA *(1)*	2.1	—	V
		IOH = –1 mA *(1)*	2.0	—	V
		IOH = –2 mA *(1)*	1.7	—	V
V_{OL}	Low-level output voltage	IOL = 0.1 mA *(1)*	—	0.2	V
		IOL = 1 mA *(1)*	—	0.4	V
		IOL = 2 mA *(1)*	—	0.7	V

Table 5–8. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	1.71	1.89	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	2.25 *(2)*	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	IOH = –2 mA *(1)*	V_{CCIO} – 0.45	—	V
V_{OL}	Low-level output voltage	IOL = 2 mA *(1)*	—	0.45	V

Table 5–9. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	1.425	1.575	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	V_{CCIO} + 0.3 *(2)*	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	IOH = –2 mA *(1)*	0.75 × V_{CCIO}	—	V
V_{OL}	Low-level output voltage	IOL = 2 mA *(1)*	—	0.25 × V_{CCIO}	V

Notes to Table 5–5 through Table 5–9:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX II Architecture* chapter (*I/O Structure section*) in the *MAX II Device Handbook*.

(2) This maximum V_{IH} reflects the JEDEC specification. The MAX II input buffer can tolerate a V_{IH} maximum of 4.0, as specified by the V_I parameter in Table 5–2.

Table 5–10. 3.3-V PCI Specifications *(Note 1)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	—	0.5 × V_{CCIO}	—	V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage	—	–0.5	—	0.3 × V_{CCIO}	V
V_{OH}	High-level output voltage	IOH = –500 µA	0.9 × V_{CCIO}	—	—	V
V_{OL}	Low-level output voltage	IOL = 1.5 mA	—	—	0.1 × V_{CCIO}	V

Note to Table 5–10:

(1) 3.3-V PCI I/O standard is only supported in Bank 3 of the EPM1270 and EPM2210 devices.

Bus Hold Specifications

Table 5–11 shows the MAX II device family bus hold specifications.

Table 5–11. Bus Hold Specifications

Parameter	Conditions	V_{CCIO} Level								Unit
		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	V_{IN} > V_{IL} (maximum)	20	—	30	—	50	—	70	—	µA
High sustaining current	V_{IN} < V_{IH} (minimum)	–20	—	–30	—	–50	—	–70	—	µA
Low overdrive current	0 V < V_{IN} < V_{CCIO}	—	160	—	200	—	300	—	500	µA
High overdrive current	0 V < V_{IN} < V_{CCIO}	—	–160	—	–200	—	–300	—	–500	µA

Table 5–16. IOE Internal Timing Microparameters

Symbol	Parameter	MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{FASTIO}	Data output delay from adjacent LE to I/O block	—	159	—	207	—	254	—	170	—	348	—	428	ps
t_{IN}	I/O input pad and buffer delay	—	708	—	920	—	1,132	—	907	—	970	—	986	ps
t_{GLOB} *(1)*	I/O input pad and buffer delay used as global signal pin	—	1,519	—	1,974	—	2,430	—	2,261	—	2,670	—	3,322	ps
t_{IOE}	Internally generated output enable delay	—	354	—	374	—	460	—	530	—	966	—	1,410	ps
t_{DL}	Input routing delay	—	224	—	291	—	358	—	318	—	410	—	509	ps
t_{OD} *(2)*	Output delay buffer and pad delay	—	1,064	—	1,383	—	1,702	—	1,319	—	1,526	—	1,543	ps
t_{XZ} *(3)*	Output buffer disable delay	—	756	—	982	—	1,209	—	1,045	—	1,264	—	1,276	ps
t_{ZX} *(4)*	Output buffer enable delay	—	1,003	—	1,303	—	1,604	—	1,160	—	1,325	—	1,353	ps

Notes to Table 5–16:

(1) Delay numbers for t_{GLOB} differ for each device density and speed grade. The delay numbers for t_{GLOB}, shown in Table 5–16, are based on an EPM240 device target.

(2) Refer to Table 5–32 and 5–24 for delay adders associated with different I/O standards, drive strengths, and slew rates.

(3) Refer to Table 5–19 and 5–14 for t_{XZ} delay adders associated with different I/O standards, drive strengths, and slew rates.

(4) Refer to Table 5–17 and 5–13 for t_{ZX} delay adders associated with different I/O standards, drive strengths, and slew rates.

Table 5–17 through Table 5–20 show the adder delays for t_{ZX} and t_{XZ} microparameters when using an I/O standard other than 3.3-V LVTTL with 16 mA drive strength.

Table 5–17. t_{ZX} IOE Microparameter Adders for Fast Slew Rate (Part 1 of 2)

Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	8 mA	—	28	—	37	—	45	—	72	—	71	—	74	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	4 mA	—	28	—	37	—	45	—	72	—	71	—	74	ps
2.5-V LVTTL / LVCMOS	14 mA	—	14	—	19	—	23	—	75	—	87	—	90	ps
	7 mA	—	314	—	409	—	503	—	162	—	174	—	177	ps
1.8-V LVTTL / LVCMOS	6 mA	—	450	—	585	—	720	—	279	—	289	—	291	ps
	3 mA	—	1,443	—	1,876	—	2,309	—	499	—	508	—	512	ps

Table 5–20. t_{XZ} IOE Microparameter Adders for Slow Slew Rate

Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	206	—	–20	—	–247	—	1,433	—	1,446	—	1,454	ps
	8 mA	—	891	—	665	—	438	—	1,332	—	1,345	—	1,348	ps
3.3-V LVCMOS	8 mA	—	206	—	–20	—	–247	—	1,433	—	1,446	—	1,454	ps
	4 mA	—	891	—	665	—	438	—	1,332	—	1,345	—	1,348	ps
2.5-V LVTTL / LVCMOS	14 mA	—	222	—	–4	—	–231	—	213	—	208	—	213	ps
	7 mA	—	943	—	717	—	490	—	166	—	161	—	166	ps
3.3-V PCI	20 mA	—	161	—	210	—	258	—	1,332	—	1,345	—	1,348	ps

☞ The default slew rate setting for MAX II devices in the Quartus II design software is "fast".

Table 5–21. UFM Block Internal Timing Microparameters (Part 1 of 3)

Symbol	Parameter	MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACLK}	Address register clock period	100	—	100	—	100	—	100	—	100	—	100	—	ns
t_{ASU}	Address register shift signal setup to address register clock	20	—	20	—	20	—	20	—	20	—	20	—	ns
t_{AH}	Address register shift signal hold to address register clock	20	—	20	—	20	—	20	—	20	—	20	—	ns
t_{ADS}	Address register data in setup to address register clock	20	—	20	—	20	—	20	—	20	—	20	—	ns
t_{ADH}	Address register data in hold from address register clock	20	—	20	—	20	—	20	—	20	—	20	—	ns
t_{DCLK}	Data register clock period	100	—	100	—	100	—	100	—	100	—	100	—	ns
t_{DSS}	Data register shift signal setup to data register clock	60	—	60	—	60	—	60	—	60	—	60	—	ns
t_{DSH}	Data register shift signal hold from data register clock	20	—	20	—	20	—	20	—	20	—	20	—	ns

Table 5–21. UFM Block Internal Timing Microparameters (Part 2 of 3)

Symbol	Parameter	MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{DDS}	Data register data in setup to data register clock	20	—	20	—	20	—	20	—	20	—	20	—	ns
t_{DDH}	Data register data in hold from data register clock	20	—	20	—	20	—	20	—	20	—	20	—	ns
t_{DP}	Program signal to data clock hold time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PB}	Maximum delay between program rising edge to UFM busy signal rising edge	—	960	—	960	—	960	—	960	—	960	—	960	ns
t_{BP}	Minimum delay allowed from UFM busy signal going low to program signal going low	20	—	20	—	20	—	20	—	20	—	20	—	ns
t_{PPMX}	Maximum length of busy pulse during a program	—	100	—	100	—	100	—	100	—	100	—	100	µs
t_{AE}	Minimum erase signal to address clock hold time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{EB}	Maximum delay between the erase rising edge to the UFM busy signal rising edge	—	960	—	960	—	960	—	960	—	960	—	960	ns
t_{BE}	Minimum delay allowed from the UFM busy signal going low to erase signal going low	20	—	20	—	20	—	20	—	20	—	20	—	ns
t_{EPMX}	Maximum length of busy pulse during an erase	—	500	—	500	—	500	—	500	—	500	—	500	ms
t_{DCO}	Delay from data register clock to data register output	—	5	—	5	—	5	—	5	—	5	—	5	ns

Table 5–29. External Timing Output Delay and t_{OD} Adders for Fast Slew Rate

I/O Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	8 mA	—	65	—	84	—	104	—	–6	—	–2	—	–3	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	4 mA	—	65	—	84	—	104	—	–6	—	–2	—	–3	ps
2.5-V LVTTL / LVCMOS	14 mA	—	122	—	158	—	195	—	–63	—	–71	—	–88	ps
	7 mA	—	193	—	251	—	309	—	10	—	–1	—	1	ps
1.8-V LVTTL / LVCMOS	6 mA	—	568	—	738	—	909	—	128	—	118	—	118	ps
	3 mA	—	654	—	850	—	1,046	—	352	—	327	—	332	ps
1.5-V LVCMOS	4 mA	—	1,059	—	1,376	—	1,694	—	421	—	400	—	400	ps
	2 mA	—	1,167	—	1,517	—	1,867	—	757	—	743	—	743	ps
3.3-V PCI	20 mA	—	3	—	4	—	5	—	–6	—	–2	—	–3	ps

Table 5–30. External Timing Output Delay and t_{OD} Adders for Slow Slew Rate

I/O Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	7,064	—	6,745	—	6,426	—	5,966	—	5,992	—	6,118	ps
	8 mA	—	7,946	—	7,627	—	7,308	—	6,541	—	6,570	—	6,720	ps
3.3-V LVCMOS	8 mA	—	7,064	—	6,745	—	6,426	—	5,966	—	5,992	—	6,118	ps
	4 mA	—	7,946	—	7,627	—	7,308	—	6,541	—	6,570	—	6,720	ps
2.5-V LVTTL / LVCMOS	14 mA	—	10,434	—	10,115	—	9,796	—	9,141	—	9,154	—	9,297	ps
	7 mA	—	11,548	—	11,229	—	10,910	—	9,861	—	9,874	—	10,037	ps
1.8-V LVTTL / LVCMOS	6 mA	—	22,927	—	22,608	—	22,289	—	21,811	—	21,854	—	21,857	ps
	3 mA	—	24,731	—	24,412	—	24,093	—	23,081	—	23,034	—	23,107	ps
1.5-V LVCMOS	4 mA	—	38,723	—	38,404	—	38,085	—	39,121	—	39,124	—	39,124	ps
	2 mA	—	41,330	—	41,011	—	40,692	—	40,631	—	40,634	—	40,634	ps
3.3-V PCI	20 mA	—	261	—	339	—	418	—	6,644	—	6,627	—	6,914	ps