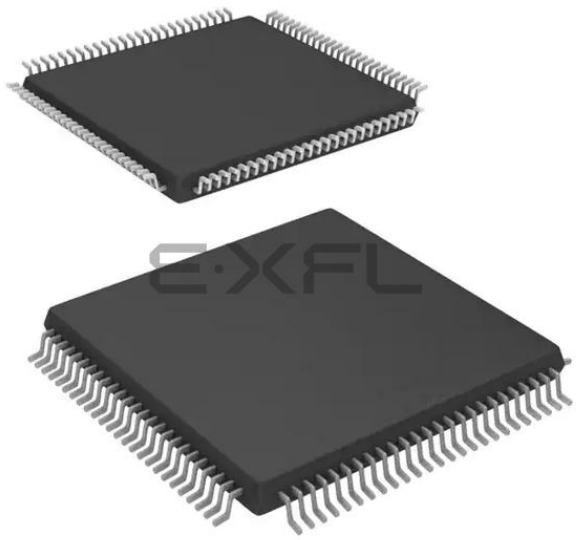


Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

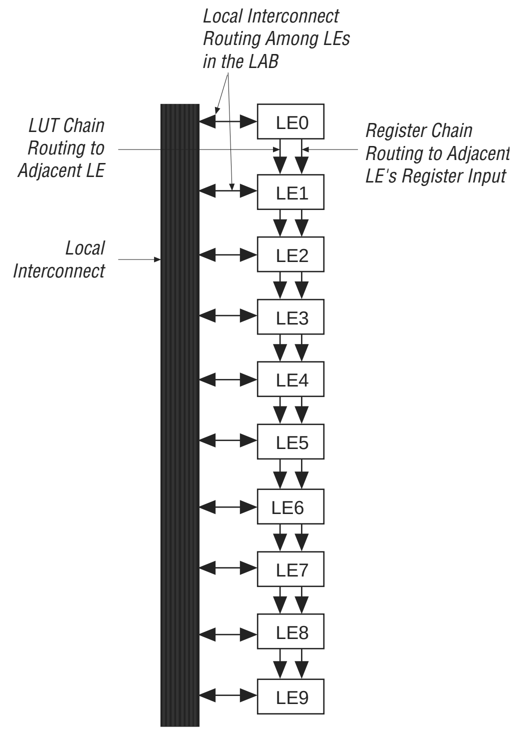
Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.4 ns
Voltage Supply - Internal	1.71V ~ 1.89V
Number of Logic Elements/Blocks	570
Number of Macrocells	440
Number of Gates	-
Number of I/O	76
Operating Temperature	0°C ~ 85°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm570gt100c3n

Table 1–6. Document Revision History

Date and Revision	Changes Made	Summary of Changes
June 2005, version 1.3	■ Updated timing numbers in Table 1-1.	—
December 2004, version 1.2	■ Updated timing numbers in Table 1-1.	—
June 2004, version 1.1	■ Updated timing numbers in Table 1-1.	—

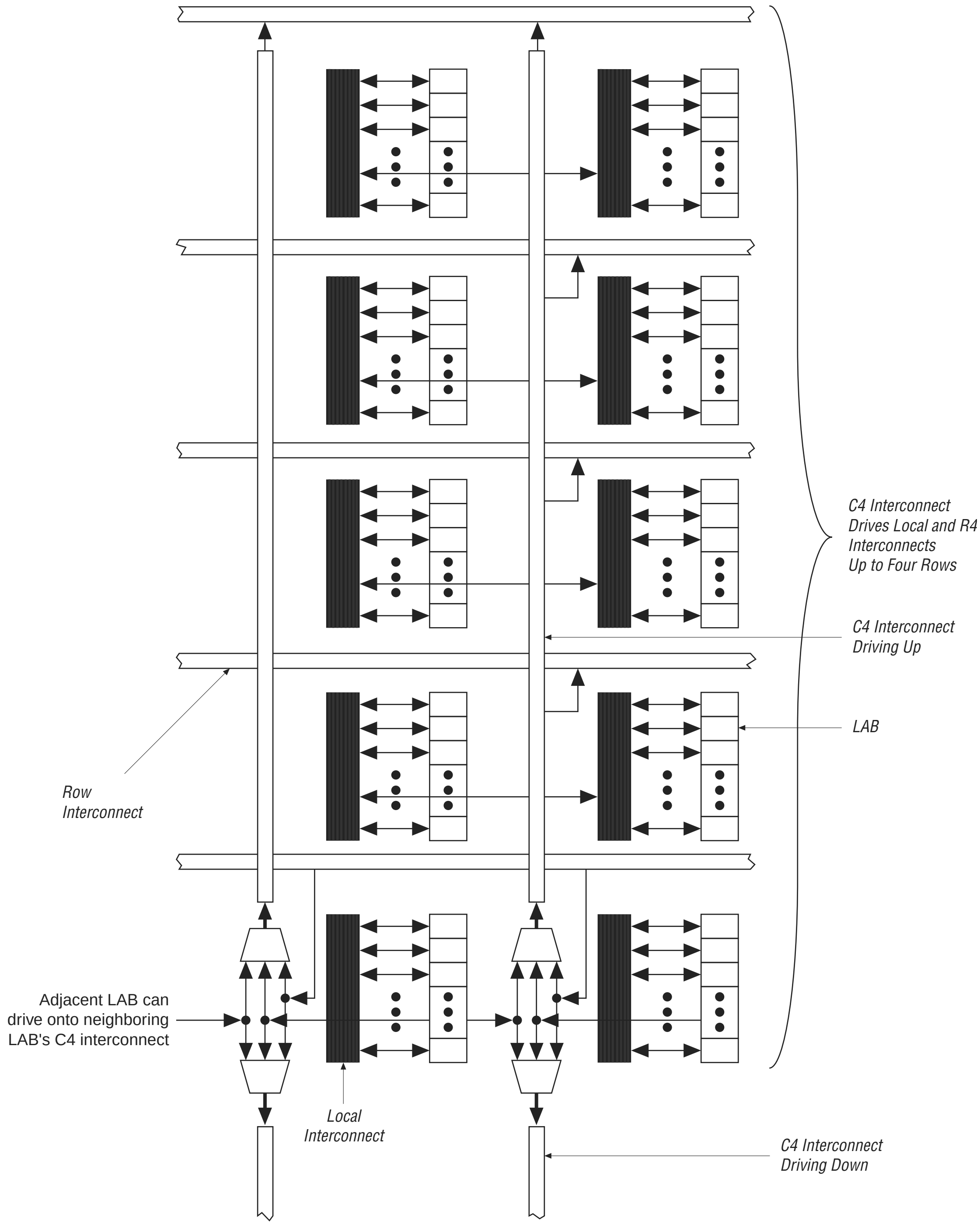
functions from LE 1 to LE 10 in the same LAB. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–11 shows the LUT chain and register chain interconnects.

Figure 2–11. LUT Chain and Register Chain Interconnects



The C4 interconnects span four LABs up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–12 shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by column and row IOEs. For LAB interconnection, a primary LAB or its vertical LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Figure 2–12. C4 Interconnect Connections *(Note 1)*

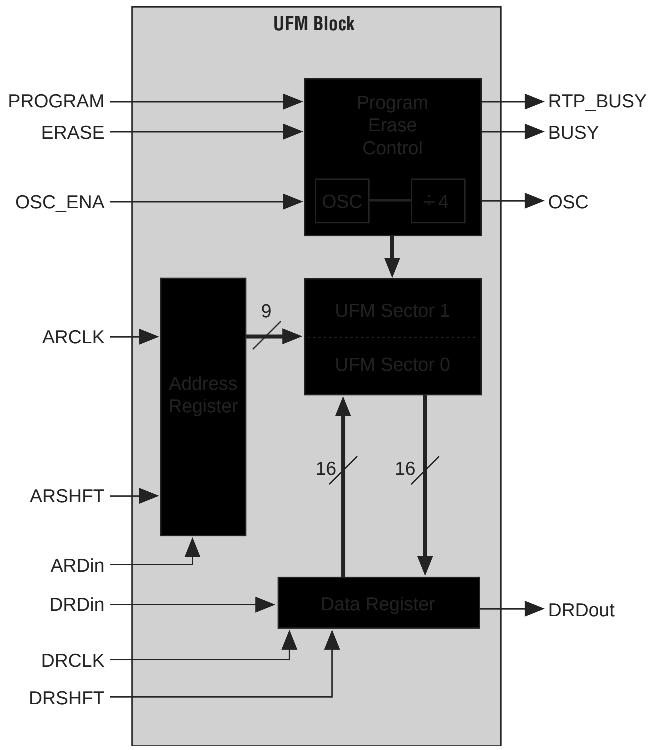


Note to Figure 2–12:

(1) Each C4 interconnect can drive either up or down four rows.

- Auto-increment addressing
- Serial interface to logic array with programmable interface

Figure 2–15. UFM Block and Interface Signals



UFM Storage

Each device stores up to 8,192 bits of data in the UFM block. Table 2–3 shows the data size, sector, and address sizes for the UFM block.

Table 2–3. UFM Array Size

Device	Total Bits	Sectors	Address Bits	Data Width
EPM240 EPM570 EPM1270 EPM2210	8,192	2 (4,096 bits/sector)	9	16

There are 512 locations with 9-bit addressing ranging from `000h` to `1FFh`. Sector 0 address space is `000h` to `0FFh` and Sector 1 address space is from `100h` to `1FFh`. The data width is up to 16 bits of data. The Quartus II software automatically creates logic to accommodate smaller read or program data widths. Erasure of the UFM involves individual sector erasing (that is, one erase of sector 0 and one erase of sector 1 is required to erase the entire UFM block). Since sector erase is required before a program or write, having two sectors enables a sector size of data to be left untouched while the other sector is erased and programmed with new data.

Internal Oscillator

As shown in Figure 2–15, the dedicated circuitry within the UFM block contains an oscillator. The dedicated circuitry uses this internally for its read and program operations. This oscillator's divide by 4 output can drive out of the UFM block as a logic interface clock source or for general-purpose logic clocking. The typical `OSC` output signal frequency ranges from 3.3 to 5.5 MHz, and its exact frequency of operation is not programmable.

Program, Erase, and Busy Signals

The UFM block's dedicated circuitry automatically generates the necessary internal program and erase algorithm once the `PROGRAM` or `ERASE` input signals have been asserted. The `PROGRAM` or `ERASE` signal must be asserted until the busy signal deasserts, indicating the UFM internal program or erase operation has completed. The UFM block also supports JTAG as the interface for programming and/or reading.

For more information about programming and erasing the UFM block, refer to the *Using User Flash Memory in MAX II Devices* chapter in the *MAX II Device Handbook*.

Auto-Increment Addressing

The UFM block supports standard read or stream read operations. The stream read is supported with an auto-increment address feature. Deasserting the `ARSHIFT` signal while clocking the `ARCLK` signal increments the address register value to read consecutive locations from the UFM array.

Serial Interface

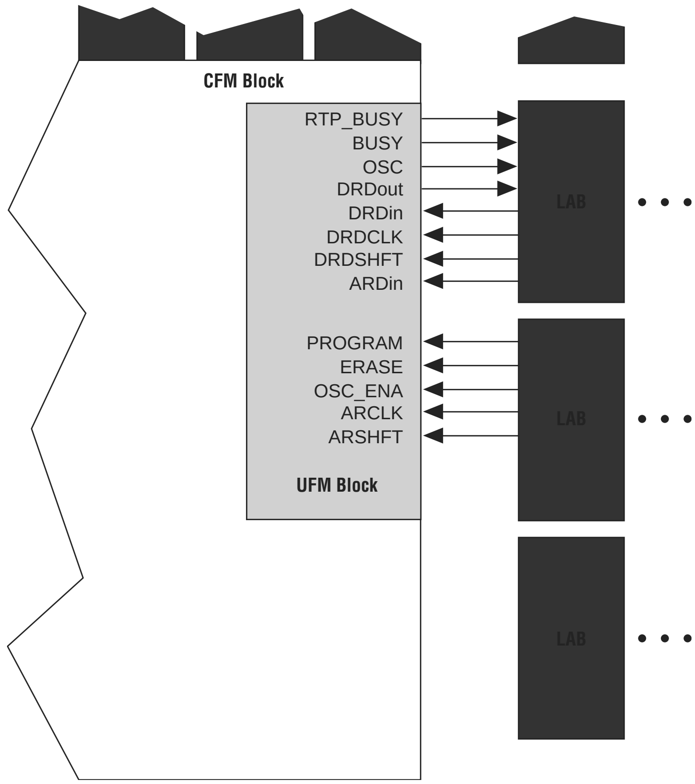
The UFM block supports a serial interface with serial address and data signals. The internal shift registers within the UFM block for address and data are 9 bits and 16 bits wide, respectively. The Quartus II software automatically generates interface logic in LEs for a parallel address and data interface to the UFM block. Other standard protocol interfaces such as SPI are also automatically generated in LE logic by the Quartus II software.

For more information about the UFM interface signals and the Quartus II LE-based alternate interfaces, refer to the *Using User Flash Memory in MAX II Devices* chapter in the *MAX II Device Handbook*.

UFM Block to Logic Array Interface

The UFM block is a small partition of the flash memory that contains the CFM block, as shown in Figure 2–1 and Figure 2–2. The UFM block for the EPM240 device is located on the left side of the device adjacent to the left most LAB column. The UFM block for the EPM570, EPM1270, and EPM2210 devices is located at the bottom left of the device. The UFM input and output signals interface to all types of interconnects (R4 interconnect, C4 interconnect, and DirectLink interconnect to/from adjacent LAB rows). The UFM signals can also be driven from global clocks, `GCLK[3..0]`. The interface region for the EPM240 device is shown in Figure 2–16. The interface regions for EPM570, EPM1270, and EPM2210 devices are shown in Figure 2–17.

Figure 2–17. EPM570, EPM1270, and EPM2210 UFM Block LAB Row Interface



MultiVolt Core

The MAX II architecture supports the MultiVolt core feature, which allows MAX II devices to support multiple V_{CC} levels on the V_{CCINT} supply. An internal linear voltage regulator provides the necessary 1.8-V internal voltage supply to the device. The voltage regulator supports 3.3-V or 2.5-V supplies on its inputs to supply the 1.8-V internal voltage to the device, as shown in Figure 2–18. The voltage regulator is not guaranteed for voltages that are between the maximum recommended 2.5-V operating voltage and the minimum recommended 3.3-V operating voltage.

The MAX IIG and MAX IIZ devices use external 1.8-V supply. The 1.8-V V_{CC} external supply powers the device core directly.

Figure 2–18. MultiVolt Core Feature in MAX II Devices

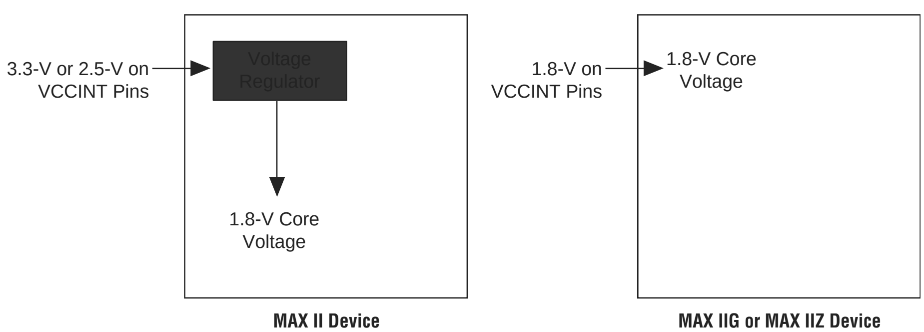
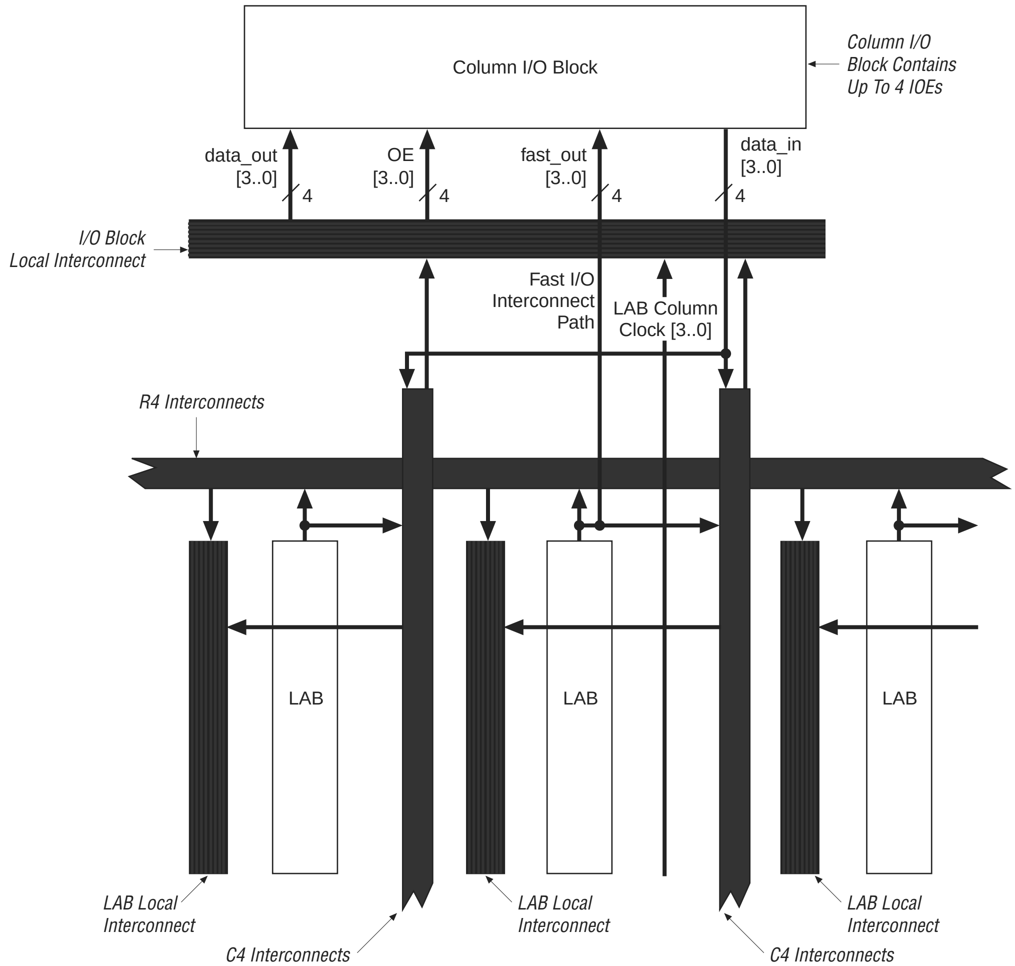


Figure 2–21 shows how a column I/O block connects to the logic array.

Figure 2–21. Column I/O Block Connection to the Interconnect *(Note 1)*



Note to Figure 2–21:

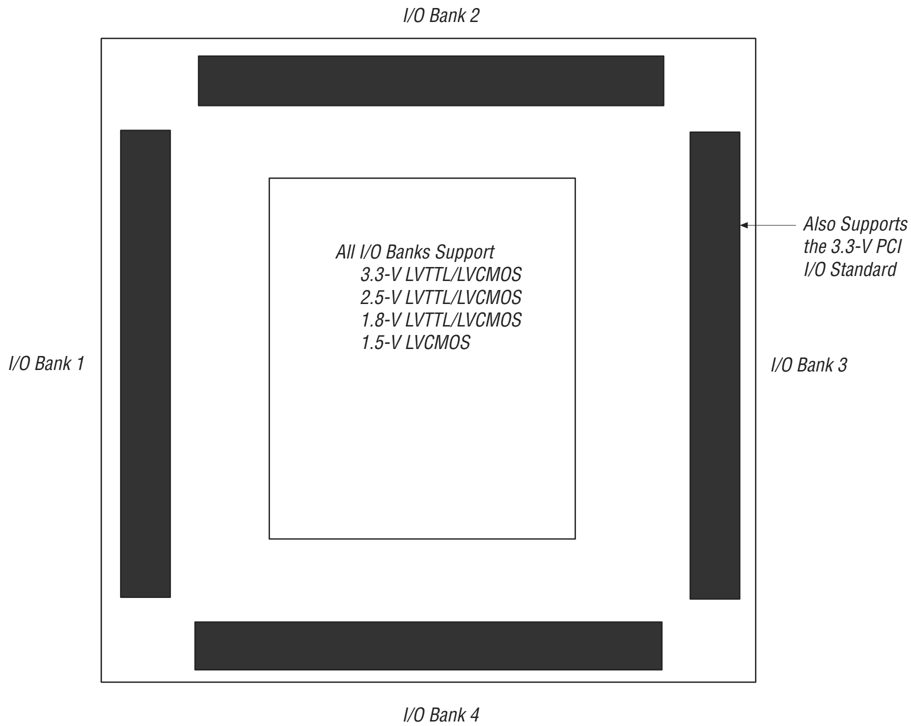
(1) Each of the four IOEs in the column I/O block can have one `data_out` or `fast_out` output, one `OE` output, and one `data_in` input.

I/O Standards and Banks

MAX II device IOEs support the following I/O standards:

- 3.3-V LVTTL/LVCMOS
- 2.5-V LVTTL/LVCMOS
- 1.8-V LVTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI

Figure 2–23. MAX II I/O Banks for EPM1270 and EPM2210 *(Note 1)*, *(2)*



Notes to Figure 2–23:

(1) Figure 2–23 is a top view of the silicon die.

(2) Figure 2–23 is a graphical representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Each I/O bank has dedicated V_{CCIO} pins that determine the voltage standard support in that bank. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each individual bank can support a different standard. Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3 V, Bank 3 can support LVTTL, LVCMOS, and 3.3-V PCI. V_{CCIO} powers both the input and output buffers in MAX II devices.

The JTAG pins for MAX II devices are dedicated pins that cannot be used as regular I/O pins. The pins `TMS`, `TDI`, `TDO`, and `TCK` support all the I/O standards shown in Table 2–4 on page 2–27 except for PCI. These pins reside in Bank 1 for all MAX II devices and their I/O standard support is controlled by the V_{CCIO} setting for Bank 1.

PCI Compliance

The MAX II EPM1270 and EPM2210 devices are compliant with PCI applications as well as all 3.3-V electrical specifications in the *PCI Local Bus Specification Revision 2.2*. These devices are also large enough to support PCI intellectual property (IP) cores. Table 2–5 shows the MAX II device speed grades that meet the PCI timing specifications.

Bus Hold

Each MAX II device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. The designer can select this feature individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the device cannot use the programmable pull-up option.

The bus-hold circuitry uses a resistor to pull the signal level to the last driven state. The *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* gives the specific sustaining current for each V_{CCIO} voltage level driven through this resistor and overdrive current used to identify the next-driven input level.

The bus-hold circuitry is only active after the device has fully initialized. The bus-hold circuit captures the value on the pin present at the moment user mode is entered.

Programmable Pull-Up Resistor

Each MAX II device I/O pin provides an optional programmable pull-up resistor during user mode. If the designer enables this feature for an I/O pin, the pull-up resistor holds the output to the V_{CCIO} level of the output pin's bank.

☞ The programmable pull-up resistor feature should not be used at the same time as the bus-hold feature on a given I/O pin.

Programmable Input Delay

The MAX II IOE includes a programmable input delay that is activated to ensure zero hold times. A path where a pin directly drives a register, with minimal routing between the two, may require the delay to ensure zero hold time. However, a path where a pin drives a register through long routing or through combinational logic may not require the delay to achieve a zero hold time. The Quartus II software uses this delay to ensure zero hold times when needed.

MultiVolt I/O Interface

The MAX II architecture supports the MultiVolt I/O interface feature, which allows MAX II devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation (V_{CCINT}), and up to four sets for input buffers and I/O output driver buffers (V_{CCIO}), depending on the number of I/O banks available in the devices where each set of VCC pins powers one I/O bank. The EPM240 and EPM570 devices have two I/O banks respectively while the EPM1270 and EPM2210 devices have four I/O banks respectively.

Document Revision History

Table 2–8 shows the revision history for this chapter.

Table 2–8. Document Revision History

Date and Revision	Changes Made	Summary of Changes
October 2008, version 2.2	■ Updated Table 2–4 and Table 2–6. ■ Updated "I/O Standards and Banks" section. ■ Updated New Document Format.	—
March 2008, version 2.1	■ Updated "Schmitt Trigger" section.	—
December 2007, version 2.0	■ Updated "Clear and Preset Logic Control" section. ■ Updated "MultiVolt Core" section. ■ Updated "MultiVolt I/O Interface" section. ■ Updated Table 2–7. ■ Added "Referenced Documents" section.	Updated document with MAX IIZ information.
December 2006, version 1.7	■ Minor update in "Internal Oscillator" section. Added document revision history.	—
August 2006, version 1.6	■ Updated functional description and I/O structure sections.	—
July 2006, vervion 1.5	■ Minor content and table updates.	—
February 2006, version 1.4	■ Updated "LAB Control Signals" section. ■ Updated "Clear and Preset Logic Control" section. ■ Updated "Internal Oscillator" section. ■ Updated Table 2–5.	—
August 2005, version 1.3	■ Removed Note 2 from Table 2-7.	—
December 2004, version 1.2	■ Added a paragraph to page 2-15.	—
June 2004, version 1.1	■ Added CFM acronym. Corrected Figure 2-19.	—

3. JTAG and In-System Programmability

MII51003-1.6

Introduction

This chapter discusses how to use the IEEE Standard 1149.1 Boundary-Scan Test (BST) circuitry in MAX II devices and includes the following sections:

- "IEEE Std. 1149.1 (JTAG) Boundary-Scan Support" on page 3–1
- "In System Programmability" on page 3–4

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All MAX® II devices provide Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry that complies with the IEEE Std. 1149.1-2001 specification. JTAG boundary-scan testing can only be performed at any time after V_{CCINT} and all V_{CCIO} banks have been fully powered and a t_{CONFIG} amount of time has passed. MAX II devices can also use the JTAG port for in-system programming together with either the Quartus® II software or hardware using Programming Object Files (**.pof**), JamTM Standard Test and Programming Language (STAPL) Files (**.jam**), or Jam Byte-Code Files (**.jbc**).

The JTAG pins support 1.5-V, 1.8-V, 2.5-V, or 3.3-V I/O standards. The supported voltage level and standard are determined by the V_{CCIO} of the bank where it resides. The dedicated JTAG pins reside in Bank 1 of all MAX II devices.

MAX II devices support the JTAG instructions shown in Table 3–1.

Table 3–1. MAX II JTAG Instructions (Part 1 of 2)

JTAG Instruction	Instruction Code	Description
`SAMPLE/PRELOAD`	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
`EXTEST` *(1)*	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
`BYPASS`	11 1111 1111	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
`USERCODE`	00 0000 0111	Selects the 32-bit `USERCODE` register and places it between the `TDI` and `TDO` pins, allowing the `USERCODE` to be serially shifted out of `TDO`. This register defaults to all 1's if not specified in the Quartus II software.
`IDCODE`	00 0000 0110	Selects the `IDCODE` register and places it between `TDI` and `TDO`, allowing the `IDCODE` to be serially shifted out of `TDO`.
`HIGHZ` *(1)*	00 0000 1011	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the boundary scan test data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.

Table 3–1. MAX II JTAG Instructions (Part 2 of 2)

JTAG Instruction	Instruction Code	Description
`CLAMP` *(1)*	`00 0000 1010`	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the boundary scan test data to pass synchronously through selected devices to adjacent devices during normal device operation, while holding I/O pins to a state defined by the data in the boundary-scan register.
`USER0`	`00 0000 1100`	This instruction allows you to define the scan chain between `TDI` and `TDO` in the MAX II logic array. This instruction is also used for custom logic and JTAG interfaces.
`USER1`	`00 0000 1110`	This instruction allows you to define the scan chain between `TDI` and `TDO` in the MAX II logic array. This instruction is also used for custom logic and JTAG interfaces.
`IEEE 1532 instructions`	*(2)*	IEEE 1532 ISC instructions used when programming a MAX II device via the JTAG port.

Notes to Table 3–1:

(1) `HIGHZ`, `CLAMP`, and `EXTEST` instructions do not disable weak pull-up resistors or bus hold features.

(2) These instructions are shown in the 1532 BSDL files, which will be posted on the Altera® website at www.altera.com when they are available.

Unsupported JTAG instructions should not be issued to the MAX II device as this may put the device into an unknown state, requiring a power cycle to recover device operation.

The MAX II device instruction register length is 10 bits and the `USERCODE` register length is 32 bits. Table 3–2 and Table 3–3 show the boundary-scan register length and device `IDCODE` information for MAX II devices.

Table 3–2. MAX II Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM240	240
EPM570	480
EPM1270	636
EPM2210	816

Table 3–3. 32-Bit MAX II Device IDCODE (Part 1 of 2)

Device	Binary IDCODE (32 Bits) *(1)*				HEX IDCODE
	Version (4 Bits)	Part Number	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*	
EPM240 EPM240G	`0000`	`0010 0000 1010 0001`	`000 0110 1110`	1	0x020A10DD
EPM570 EPM570G	`0000`	`0010 0000 1010 0010`	`000 0110 1110`	1	0x020A20DD
EPM1270 EPM1270G	`0000`	`0010 0000 1010 0011`	`000 0110 1110`	1	0x020A30DD
EPM2210 EPM2210G	`0000`	`0010 0000 1010 0100`	`000 0110 1110`	1	0x020A40DD

IEEE 1532 Support

The JTAG circuitry and ISP instruction set in MAX II devices is compliant to the IEEE 1532-2002 programming specification. This provides industry-standard hardware and software for in-system programming among multiple vendor programmable logic devices (PLDs) in a JTAG chain.

The MAX II 1532 BSDL files will be released on the Altera website when available.

Jam Standard Test and Programming Language (STAPL)

The Jam STAPL JEDEC standard, JESD71, can be used to program MAX II devices with in-circuit testers, PCs, or embedded processors. The Jam byte code is also supported for MAX II devices. These software programming protocols provide a compact embedded solution for programming MAX II devices.

For more information, refer to the *Using Jam STAPL for ISP via an Embedded Processor* chapter in the *MAX II Device Handbook*.

Programming Sequence

During in-system programming, 1532 instructions, addresses, and data are shifted into the MAX II device through the `TDI` input pin. Data is shifted out through the `TDO` output pin and compared against the expected data. Programming a pattern into the device requires the following six ISP steps. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6. These steps are automatically executed by third-party programmers, the Quartus II software, or the Jam STAPL and Jam Byte-Code Players.

1. *Enter ISP*—The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode.
2. *Check ID*—Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Sector Erase*—Erasing the device in-system involves shifting in the instruction to erase the device and applying an erase pulse(s). The erase pulse is automatically generated internally by waiting in the run/test/idle state for the specified erase pulse time of 500 ms for the CFM block and 500 ms for each sector of the UFM block.
4. *Program*—Programming the device in-system involves shifting in the address, data, and program instruction and generating the program pulse to program the flash cells. The program pulse is automatically generated internally by waiting in the run/test/idle state for the specified program pulse time of 75 µs. This process is repeated for each address in the CFM and UFM blocks.
5. *Verify*—Verifying a MAX II device in-system involves shifting in addresses, applying the verify instruction to generate the read pulse, and shifting out the data for comparison. This process is repeated for each CFM and UFM address.
6. *Exit ISP*—An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode.

Table 3–4 shows the programming times for MAX II devices using in-circuit testers to execute the algorithm vectors in hardware. Software-based programming tools used with download cables are slightly slower because of data processing and transfer limitations.

Table 3–4. MAX II Device Family Programming Times

Description	EPM240 EPM240G EPM240Z	EPM570 EPM570G EPM570Z	EPM1270 EPM1270G	EPM2210 EPM2210G	Unit
Erase + Program (1 MHz)	1.72	2.16	2.90	3.92	sec
Erase + Program (10 MHz)	1.65	1.99	2.58	3.40	sec
Verify (1 MHz)	0.09	0.17	0.30	0.49	sec
Verify (10 MHz)	0.01	0.02	0.03	0.05	sec
Complete Program Cycle (1 MHz)	1.81	2.33	3.20	4.41	sec
Complete Program Cycle (10 MHz)	1.66	2.01	2.61	3.45	sec

UFM Programming

The Quartus II software, with the use of POF, Jam, or JBC files, supports programming of the user flash memory (UFM) block independent of the logic array design pattern stored in the CFM block. This allows updating or reading UFM contents through ISP without altering the current logic array design, or vice versa. By default, these programming files and methods will program the entire flash memory contents, which includes the CFM block and UFM contents. The stand-alone embedded Jam STAPL player and Jam Byte-Code Player provides action commands for programming or reading the entire flash memory (UFM and CFM together) or each independently.

For more information, refer to the *Using Jam STAPL for ISP via an Embedded Processor* chapter in the *MAX II Device Handbook*.

In-System Programming Clamp

By default, the IEEE 1532 instruction used for entering ISP automatically tri-states all I/O pins with weak pull-up resistors for the duration of the ISP sequence. However, some systems may require certain pins on MAX II devices to maintain a specific DC logic level during an in-field update. For these systems, an optional in-system programming clamp instruction exists in MAX II circuitry to control I/O behavior during the ISP sequence. The in-system programming clamp instruction enables the device to sample and sustain the value on an output pin (an input pin would remain tri-stated if sampled) or to explicitly set a logic high, logic low, or tri-state value on any pin. Setting these options is controlled on an individual pin basis using the Quartus II software.

For more information, refer to the *Real-Time ISP and ISP Clamp for MAX II Devices* chapter in the *MAX II Device Handbook*.

I/O Pins Remain Tri-Stated during Power-Up

A device that does not support hot-socketing may interrupt system operation or cause contention by driving out before or during power-up. In a hot socketing situation, the MAX II device's output buffers are turned off during system power-up. MAX II devices do not drive out until the device attains proper operating conditions and is fully configured. Refer to "Power-On Reset Circuitry" on page 4–5 for information about turn-on voltages.

Signal Pins Do Not Drive the V_{CCIO} or V_{CCINT} Power Supplies

MAX II devices do not have a current path from I/O pins or `GCLK[3..0]` pins to the V_{CCIO} or V_{CCINT} pins before or during power-up. A MAX II device may be inserted into (or removed from) a system board that was powered up without damaging or interfering with system-board operation. When hot socketing, MAX II devices may have a minimal effect on the signal integrity of the backplane.

AC and DC Specifications

You can power up or power down the V_{CCIO} and V_{CCINT} pins in any sequence. During hot socketing, the I/O pin capacitance is less than 8 pF. MAX II devices meet the following hot socketing specifications:

- The hot socketing DC specification is: $| I_{IOPIN} | < 300\ \mu A$.
- The hot socketing AC specification is: $| I_{IOPIN} | < 8$ mA for 10 ns or less.

☞ MAX II devices are immune to latch-up when hot socketing. If the `TCK` JTAG input pin is driven high during hot socketing, the current on that pin might exceed the specifications above.

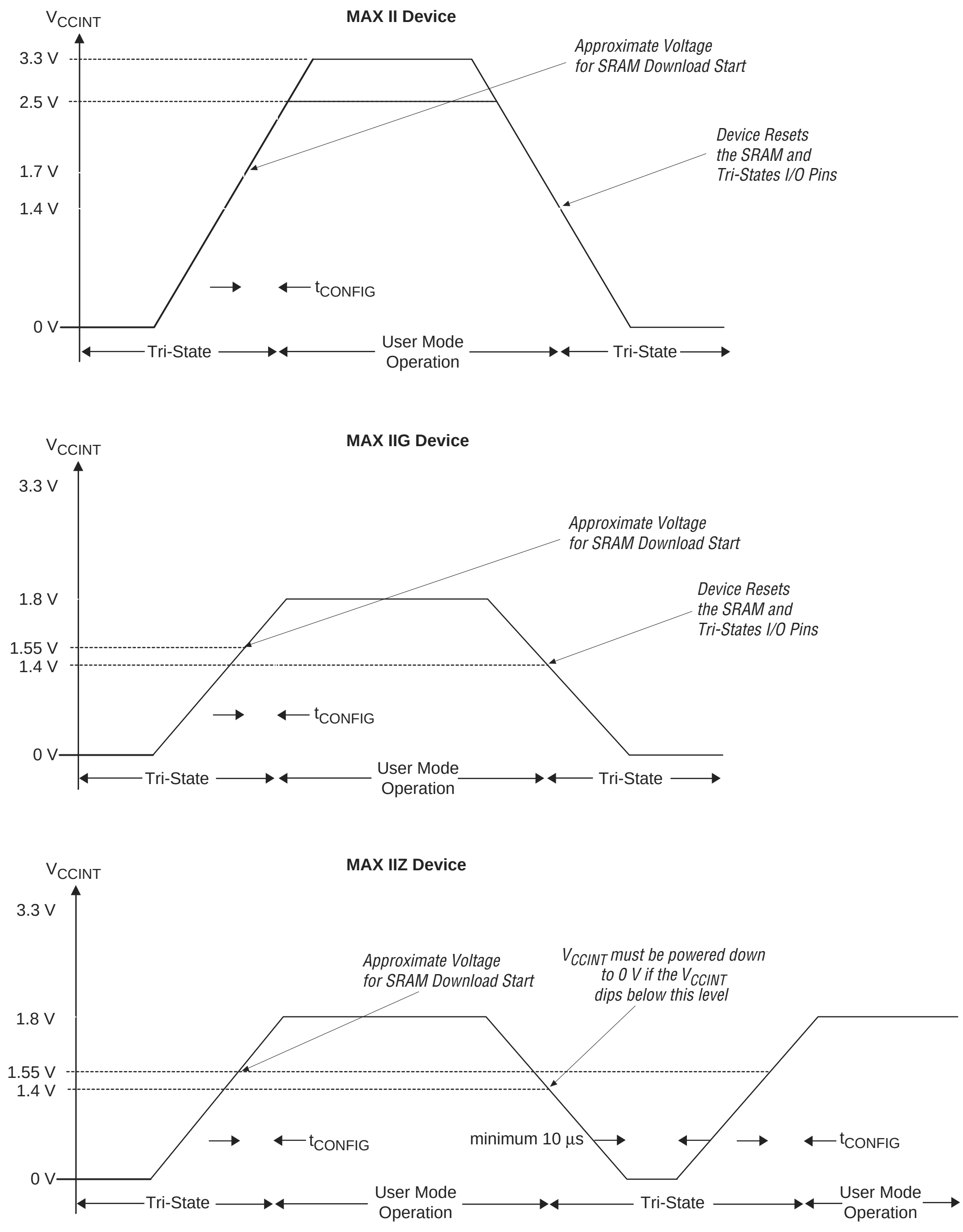
I_{IOPIN} is the current at any user I/O pin on the device. The AC specification applies when the device is being powered up or powered down. This specification takes into account the pin capacitance but not board trace and external loading capacitance. Additional capacitance for trace, connector, and loading must be taken into consideration separately. The peak current duration due to power-up transients is 10 ns or less.

The DC specification applies when all V_{CC} supplies to the device are stable in the powered-up or powered-down conditions.

Hot Socketing Feature Implementation in MAX II Devices

The hot socketing feature turns off (tri-states) the output buffer during the power-up event (either V_{CCINT} or V_{CCIO} supplies) or power-down event. The hot-socket circuit generates an internal `HOTSCKT` signal when either V_{CCINT} or V_{CCIO} is below the threshold voltage during power-up or power-down. The `HOTSCKT` signal cuts off the output buffer to make sure that no DC current (except for weak pull-up leaking) leaks through the pin. When V_{CC} ramps up very slowly during power-up, V_{CC} may still be relatively low even after the power-on reset (POR) signal is released and device configuration is complete.

Figure 4–5. Power-Up Characteristics for MAX II, MAX IIG, and MAX IIZ Devices *(Note 1)*, *(2)*



Notes to Figure 4–5:

(1) Time scale is relative.

(2) Figure 4–5 assumes all V_{CCIO} banks power up simultaneously with the V_{CCINT} profile shown. If not, t_{CONFIG} stretches out until all V_{CCIO} banks are powered.

☞ After SRAM configuration, all registers in the device are cleared and released into user function before I/O tri-states are released. To release clears after tri-states are released, use the `DEV_CLRn` pin option. To hold the tri-states beyond the power-up configuration time, use the `DEV_OE` pin option.

Programming/Erasure Specifications

Table 5–3 shows the MAX II device family programming/erasure specifications.

Table 5–3. MAX II Device Programming/Erasure Specifications

Parameter	Minimum	Typical	Maximum	Unit
Erase and reprogram cycles	—	—	100 *(1)*	Cycles

Note to Table 5–3:

(1) This specification applies to the UFM and configuration flash memory (CFM) blocks.

DC Electrical Characteristics

Table 5–4 shows the MAX II device family DC electrical characteristics.

Table 5–4. MAX II Device DC Electrical Characteristics *(Note 1)* (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIO}$max to 0 V *(2)*	–10	—	10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIO}$max to 0 V *(2)*	–10	—	10	µA
$I_{CCSTANDBY}$	V_{CCINT} supply current (standby) *(3)*	MAX II devices	—	12	—	mA
		MAX IIG devices	—	2	—	mA
		EPM240Z (Commercial grade) *(4)*	—	25	90	µA
		EPM240Z (Industrial grade) *(5)*	—	25	139	µA
		EPM570Z (Commercial grade) *(4)*	—	27	96	µA
		EPM570Z (Industrial grade) *(5)*	—	27	152	µA
$V_{SCHMITT}$ *(6)*	Hysteresis for Schmitt trigger input *(7)*	V_{CCIO} = 3.3 V	—	400	—	mV
		V_{CCIO} = 2.5 V	—	190	—	mV
$I_{CCPOWERUP}$	V_{CCINT} supply current during power-up *(8)*	MAX II devices	—	55	—	mA
		MAX IIG and MAX IIZ devices	—	40	—	mA
R_{PULLUP}	Value of I/O pin pull-up resistor during user mode and in-system programming	V_{CCIO} = 3.3 V *(9)*	5	—	25	kΩ
		V_{CCIO} = 2.5 V *(9)*	10	—	40	kΩ
		V_{CCIO} = 1.8 V *(9)*	25	—	60	kΩ
		V_{CCIO} = 1.5 V *(9)*	45	—	95	kΩ

Table 5–21. UFM Block Internal Timing Microparameters (Part 3 of 3)

Symbol	Parameter	MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{OE}	Delay from data register clock to data register output	180	—	180	—	180	—	180	—	180	—	180	—	ns
t_{RA}	Maximum read access time	—	65	—	65	—	65	—	65	—	65	—	65	ns
t_{OSCS}	Maximum delay between the OSC_ENA rising edge to the erase/program signal rising edge	250	—	250	—	250	—	250	—	250	—	250	—	ns
t_{OSCH}	Minimum delay allowed from the erase/program signal going low to OSC_ENA signal going low	250	—	250	—	250	—	250	—	250	—	250	—	ns

Figure 5–3 through Figure 5–5 show the read, program, and erase waveforms for UFM block timing parameters shown in Table 5–21.

Figure 5–3. UFM Read Waveforms

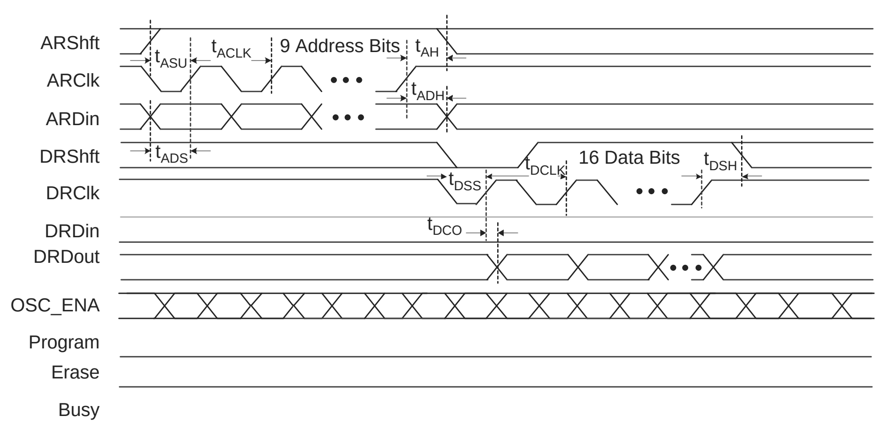


Table 5–23. EPM240 Global Clock External I/O Timing Parameters (Part 2 of 2)

Symbol	Parameter	Condition	MAX II / MAX IIG						MAX IIZ						Unit
			–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	304.0 *(1)*	—	247.5	—	201.1	—	184.1	—	123.5	—	118.3	MHz

Note to Table 5–23:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5–24 shows the external I/O timing parameters for EPM570 devices.

Table 5–24. EPM570 Global Clock External I/O Timing Parameters (Part 1 of 2)

Symbol	Parameter	Condition	MAX II / MAX IIG						MAX IIZ						Unit
			–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through 1 look-up table (LUT)	10 pF	—	5.4	—	7.0	—	8.7	—	9.5	—	15.1	—	17.7	ns
t_{PD2}	Best case pin-to-pin delay through 1 LUT	10 pF	—	3.7	—	4.8	—	5.9	—	5.7	—	7.7	—	8.5	ns
t_{SU}	Global clock setup time	—	1.2	—	1.5	—	1.9	—	2.2	—	3.9	—	4.4	—	ns
t_H	Global clock hold time	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	4.5	2.0	5.8	2.0	7.1	2.0	6.7	2.0	8.2	2.0	8.7	ns
t_{CH}	Global clock high time	—	166	—	216	—	266	—	253	—	335	—	339	—	ps
t_{CL}	Global clock low time	—	166	—	216	—	266	—	253	—	335	—	339	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	3.3	—	4.0	—	5.0	—	5.4	—	8.1	—	8.4	—	ns

Table 5–27. External Timing Input Delay Adders (Part 2 of 2)

I/O Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVCMOS	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	334	—	434	—	535	—	387	—	434	—	442	ps
2.5-V LVTTL / LVCMOS	Without Schmitt Trigger	—	23	—	30	—	37	—	42	—	43	—	43	ps
	With Schmitt Trigger	—	339	—	441	—	543	—	429	—	476	—	483	ps
1.8-V LVTTL / LVCMOS	Without Schmitt Trigger	—	291	—	378	—	466	—	378	—	373	—	373	ps
1.5-V LVCMOS	Without Schmitt Trigger	—	681	—	885	—	1,090	—	681	—	622	—	658	ps
3.3-V PCI	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	—	0	ps

Table 5–28. External Timing Input Delay t_{GLOB} Adders for GCLK Pins

I/O Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	308	—	400	—	493	—	387	—	434	—	442	ps
3.3-V LVCMOS	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	308	—	400	—	493	—	387	—	434	—	442	ps
2.5-V LVTTL / LVCMOS	Without Schmitt Trigger	—	21	—	27	—	33	—	42	—	43	—	43	ps
	With Schmitt Trigger	—	423	—	550	—	677	—	429	—	476	—	483	ps
1.8-V LVTTL / LVCMOS	Without Schmitt Trigger	—	353	—	459	—	565	—	378	—	373	—	373	ps
1.5-V LVCMOS	Without Schmitt Trigger	—	855	—	1,111	—	1,368	—	681	—	622	—	658	ps
3.3-V PCI	Without Schmitt Trigger	—	6	—	7	—	9	—	0	—	0	—	0	ps

