Welcome to E-XFL.COM

Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.4 ns
Voltage Supply - Internal	1.71V ~ 1.89V
Number of Logic Elements/Blocks	570
Number of Macrocells	440
Number of Gates	-
Number of I/O	76
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epm570gt100i5

Table 1–6. Document Revision History

Date and Revision	Changes Made	Summary of Changes
June 2005, version 1.3	■ Updated timing numbers in Table 1-1.	—
December 2004, version 1.2	■ Updated timing numbers in Table 1-1.	—
June 2004, version 1.1	■ Updated timing numbers in Table 1-1.	—

Table 2–1. MAX II Device Resources

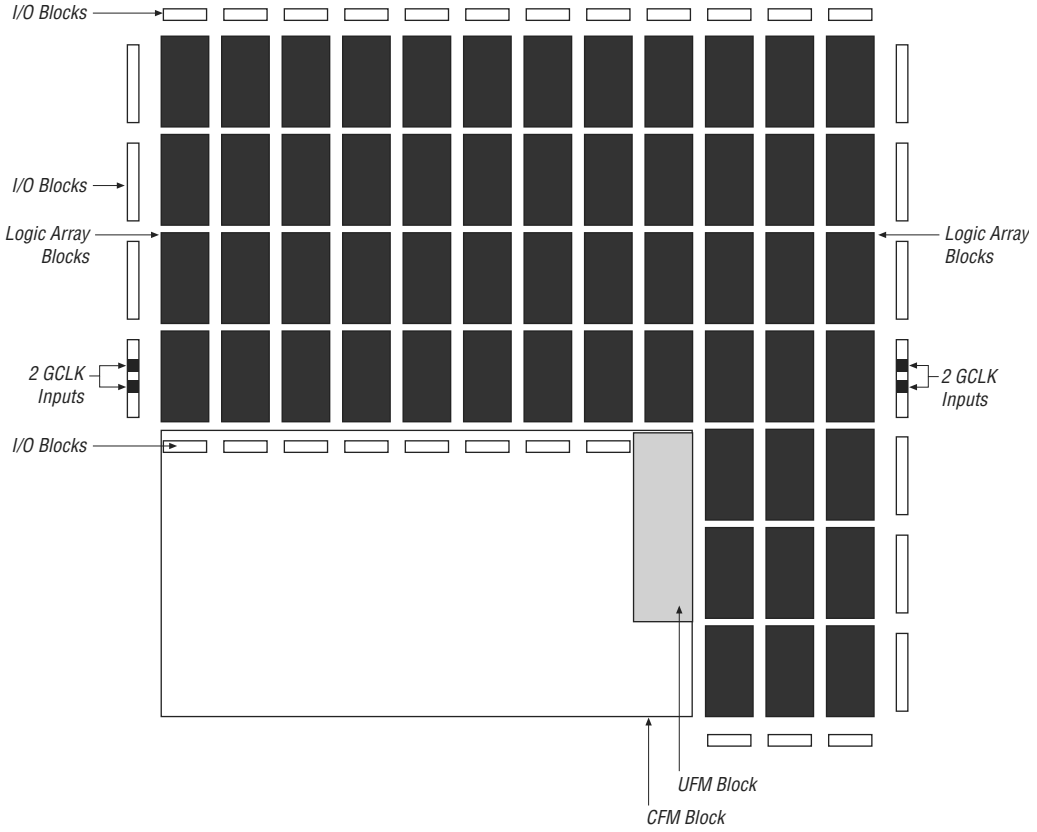
Devices	UFM Blocks	LAB Columns	LAB Rows		Total LABs
			Long LAB Rows	Short LAB Rows (Width) *(1)*	
EPM240	1	6	4	—	24
EPM570	1	12	4	3 (3)	57
EPM1270	1	16	7	3 (5)	127
EPM2210	1	20	10	3 (7)	221

Note to Table 2–1:

(1) The width is the number of LAB columns in length.

Figure 2–2 shows a floorplan of a MAX II device.

Figure 2–2. MAX II Device Floorplan *(Note 1)*



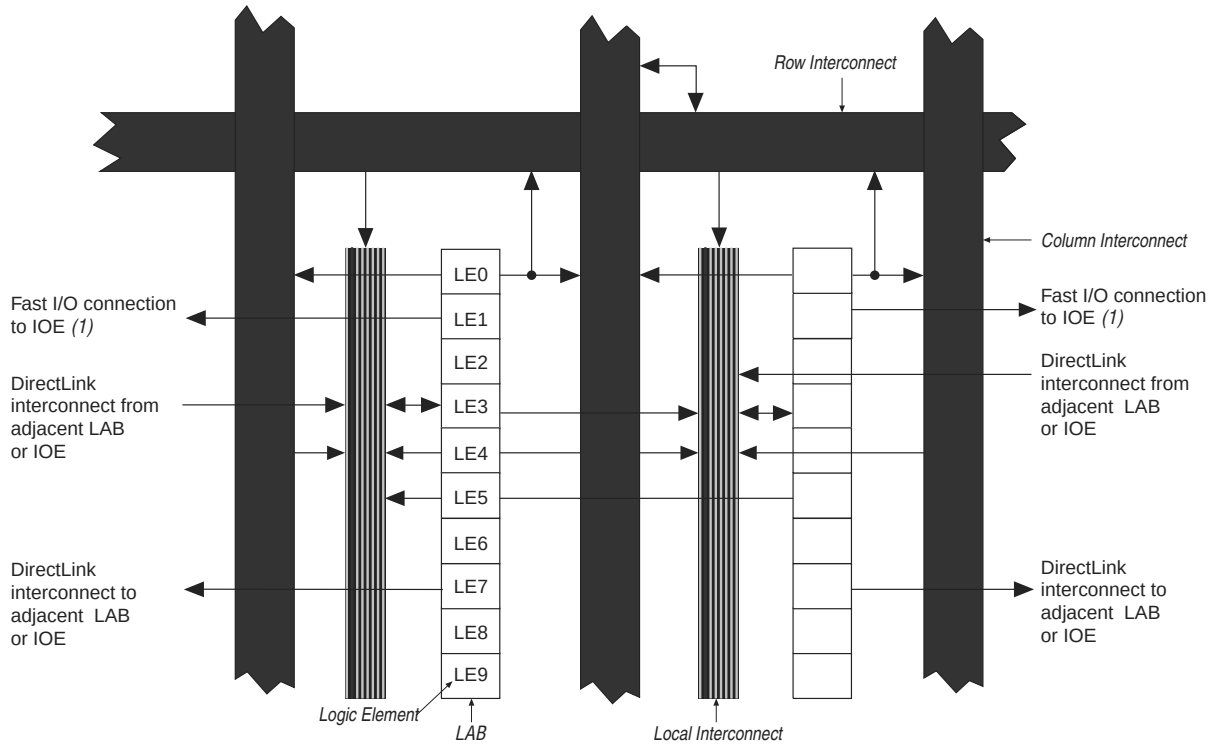
Note to Figure 2–2:

(1) The device shown is an EPM570 device. EPM1270 and EPM2210 devices have a similar floorplan with more LABs. For EPM240 devices, the CFM and UFM blocks are located on the left side of the device.

Logic Array Blocks

Each LAB consists of 10 LEs, LE carry chains, LAB control signals, a local interconnect, a look-up table (LUT) chain, and register chain connection lines. There are 26 possible unique inputs into an LAB, with an additional 10 local feedback input lines fed by LE outputs in the same LAB. The local interconnect transfers signals between LEs in the same LAB. LUT chain connections transfer the output of one LE's LUT to the adjacent LE for fast sequential LUT connections within the same LAB. Register chain connections transfer the output of one LE's register to the adjacent LE's register within an LAB. The Quartus® II software places associated logic within an LAB or adjacent LABs, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency. Figure 2–3 shows the MAX II LAB.

Figure 2–3. MAX II LAB Structure



Note to Figure 2–3:

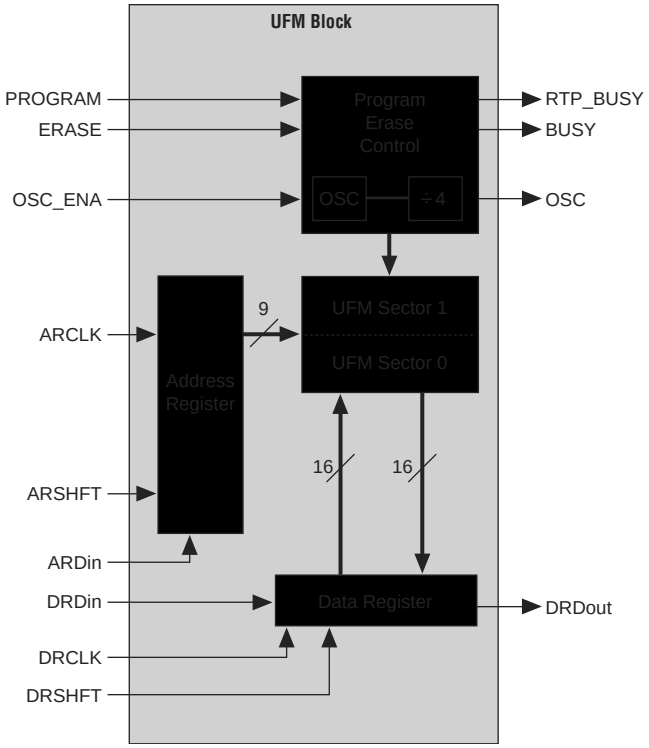
(1) Only from LABs adjacent to IOEs.

LAB Interconnects

The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, from the left and right, can also drive an LAB's local interconnect through the DirectLink connection. The DirectLink connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive 30 other LEs through fast local and DirectLink interconnects. Figure 2–4 shows the DirectLink connection.

- Auto-increment addressing
- Serial interface to logic array with programmable interface

Figure 2–15. UFM Block and Interface Signals



UFM Storage

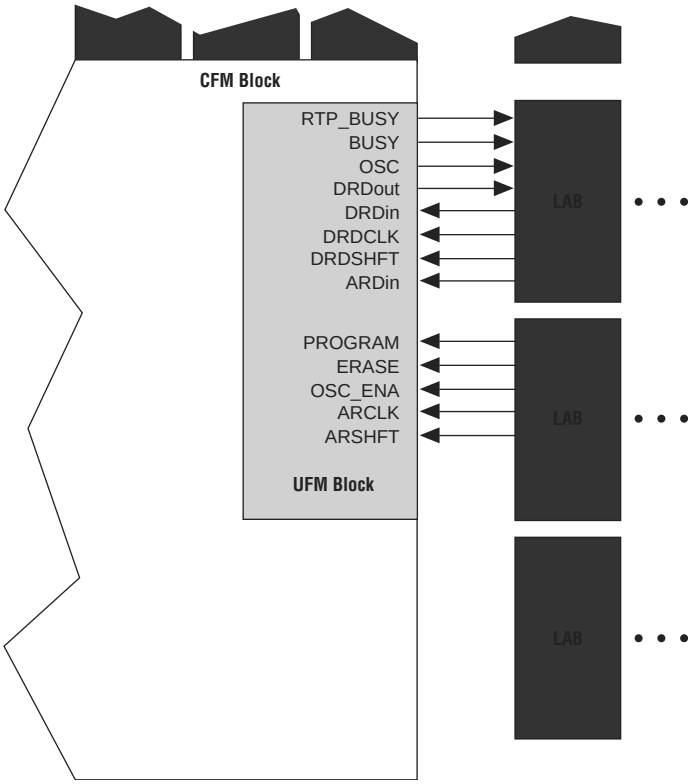
Each device stores up to 8,192 bits of data in the UFM block. Table 2–3 shows the data size, sector, and address sizes for the UFM block.

Table 2–3. UFM Array Size

Device	Total Bits	Sectors	Address Bits	Data Width
EPM240 EPM570 EPM1270 EPM2210	8,192	2 (4,096 bits/sector)	9	16

There are 512 locations with 9-bit addressing ranging from `000h` to `1FFh`. Sector 0 address space is `000h` to `0FFh` and Sector 1 address space is from `100h` to `1FFh`. The data width is up to 16 bits of data. The Quartus II software automatically creates logic to accommodate smaller read or program data widths. Erasure of the UFM involves individual sector erasing (that is, one erase of sector 0 and one erase of sector 1 is required to erase the entire UFM block). Since sector erase is required before a program or write, having two sectors enables a sector size of data to be left untouched while the other sector is erased and programmed with new data.

Figure 2–17. EPM570, EPM1270, and EPM2210 UFM Block LAB Row Interface

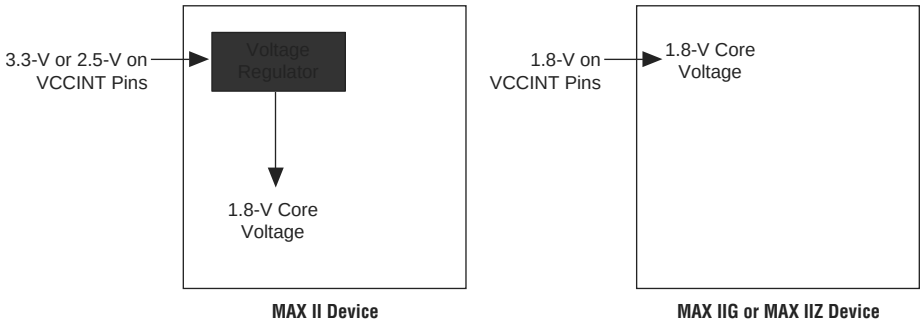


MultiVolt Core

The MAX II architecture supports the MultiVolt core feature, which allows MAX II devices to support multiple V_{CC} levels on the V_{CCINT} supply. An internal linear voltage regulator provides the necessary 1.8-V internal voltage supply to the device. The voltage regulator supports 3.3-V or 2.5-V supplies on its inputs to supply the 1.8-V internal voltage to the device, as shown in Figure 2–18. The voltage regulator is not guaranteed for voltages that are between the maximum recommended 2.5-V operating voltage and the minimum recommended 3.3-V operating voltage.

The MAX IIG and MAX IIZ devices use external 1.8-V supply. The 1.8-V V_{CC} external supply powers the device core directly.

Figure 2–18. MultiVolt Core Feature in MAX II Devices



I/O Structure

IOEs support many features, including:

- LVTTL and LVCMOS I/O standards
- 3.3-V, 32-bit, 66-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Programmable drive strength control
- Weak pull-up resistors during power-up and in system programming
- Slew-rate control
- Tri-state buffers with individual output enable control
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Unique output enable per pin
- Open-drain outputs
- Schmitt trigger inputs
- Fast I/O connection
- Programmable input delay

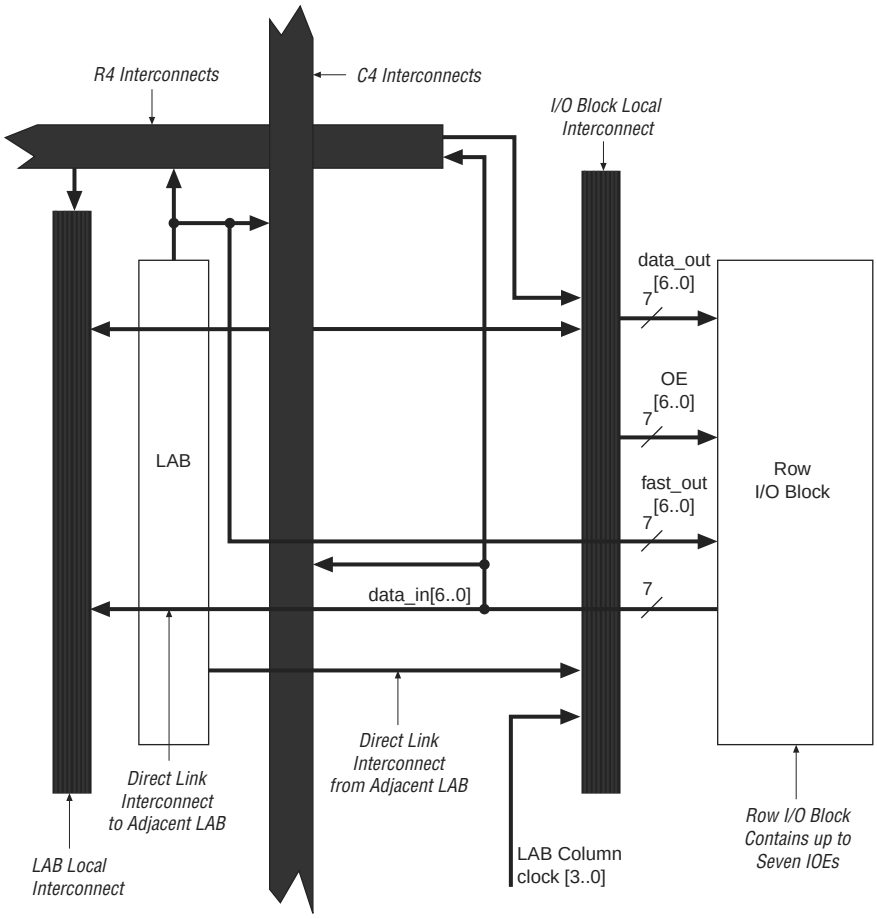
MAX II device IOEs contain a bidirectional I/O buffer. Figure 2–19 shows the MAX II IOE structure. Registers from adjacent LABs can drive to or be driven from the IOE's bidirectional I/O buffers. The Quartus II software automatically attempts to place registers in the adjacent LAB with fast I/O connection to achieve the fastest possible clock-to-output and registered output enable timing. For input registers, the Quartus II software automatically routes the register to guarantee zero hold time. You can set timing assignments in the Quartus II software to achieve desired I/O timing.

Fast I/O Connection

A dedicated fast I/O connection from the adjacent LAB to the IOEs within an I/O block provides faster output delays for clock-to-output and t_{PD} propagation delays. This connection exists for data output signals, not output enable signals or input signals. Figure 2–20, Figure 2–21, and Figure 2–22 illustrate the fast I/O connection.

Figure 2–20 shows how a row I/O block connects to the logic array.

Figure 2–20. Row I/O Block Connection to the Interconnect *(Note 1)*

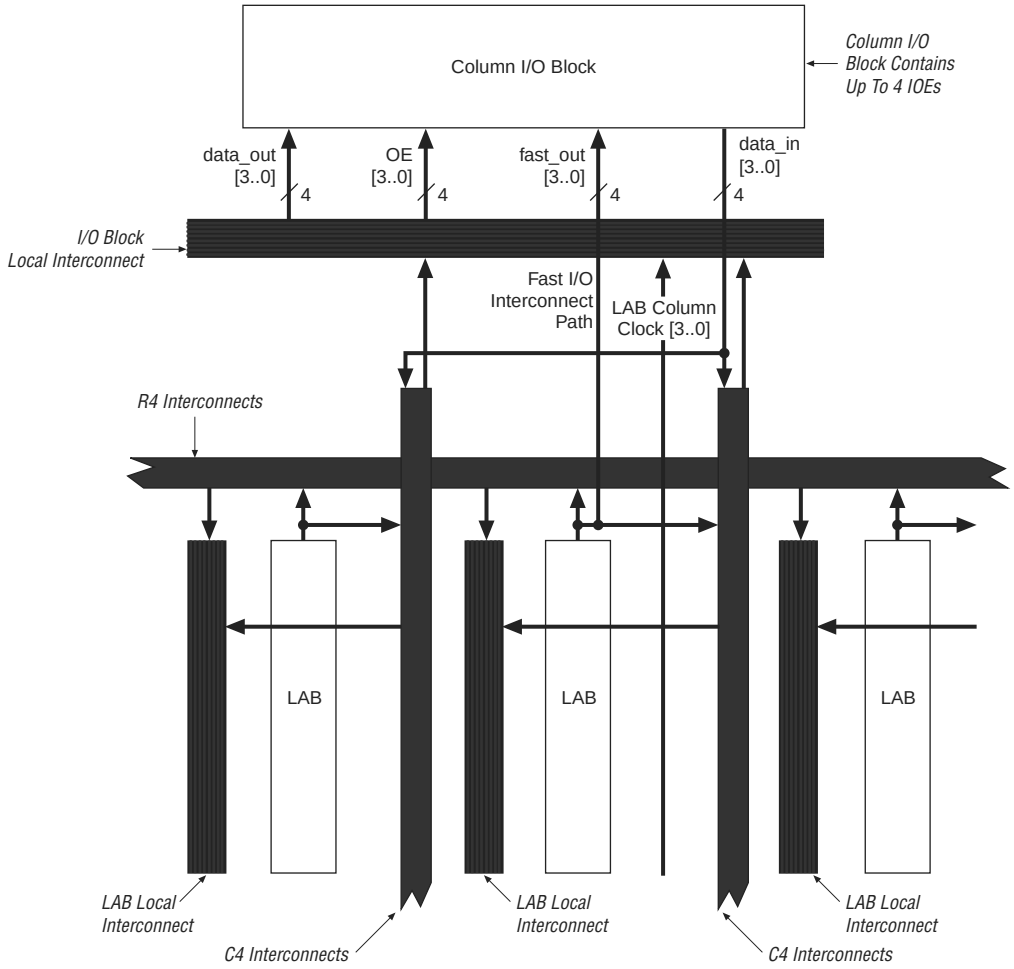


Note to Figure 2–20:

(1) Each of the seven IOEs in the row I/O block can have one `data_out` or `fast_out` output, one `OE` output, and one `data_in` input.

Figure 2–21 shows how a column I/O block connects to the logic array.

Figure 2–21. Column I/O Block Connection to the Interconnect *(Note 1)*



Note to Figure 2–21:

(1) Each of the four IOEs in the column I/O block can have one `data_out` or `fast_out` output, one `OE` output, and one `data_in` input.

I/O Standards and Banks

MAX II device IOEs support the following I/O standards:

- 3.3-V LVTTL/LVCMOS
- 2.5-V LVTTL/LVCMOS
- 1.8-V LVTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI

Table 2–6. Programmable Drive Strength *(Note 1)*

I/O Standard	IOH/IOL Current Strength Setting (mA)
3.3-V LVTTL	16
	8
3.3-V LVCMOS	8
	4
2.5-V LVTTL/LVCMOS	14
	7
1.8-V LVTTL/LVCMOS	6
	3
1.5-V LVCMOS	4
	2

Note to Table 2–6:

(1) The I_{OH} current strength numbers shown are for a condition of a $V_{OUT} = V_{OH}$ minimum, where the V_{OH} minimum is specified by the I/O standard. The I_{OL} current strength numbers shown are for a condition of a $V_{OUT} = V_{OL}$ maximum, where the V_{OL} maximum is specified by the I/O standard. For 2.5-V LVTTL/LVCMOS, the I_{OH} condition is V_{OUT} = 1.7 V and the I_{OL} condition is V_{OUT} = 0.7 V.

Slew-Rate Control

The output buffer for each MAX II device I/O pin has a programmable output slew-rate control that can be configured for low noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal output delay to rising and falling edges. The lower the voltage standard (for example, 1.8-V LVTTL) the larger the output delay when slow slew is enabled. Each I/O pin has an individual slew-rate control, allowing the designer to specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges.

Open-Drain Output

MAX II devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that can be asserted by any of several devices. This output can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX II devices can be used as an additional ground pin. This programmable ground feature does not require the use of the associated LEs in the device. In the Quartus II software, unused pins can be set as programmable GND on a global default basis or they can be individually assigned. Unused pins also have the option of being set as tri-stated input pins.

Connect VCCIO pins to either a 1.5-V, 1.8 V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (that is, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems. Table 2–7 summarizes MAX II MultiVolt I/O support.

Table 2–7. MAX II MultiVolt I/O Support *(Note 1)*

	Input Signal					Output Signal				
VCCIO (V)	**1.5 V**	**1.8 V**	**2.5 V**	**3.3 V**	**5.0 V**	**1.5 V**	**1.8 V**	**2.5 V**	**3.3 V**	**5.0 V**
1.5	✓	✓	✓	✓	—	✓	—	—	—	—
1.8	✓	✓	✓	✓	—	✓ *(2)*	✓	—	—	—
2.5	—	—	✓	✓	—	✓ *(3)*	✓ *(3)*	✓	—	—
3.3	—	—	✓ *(4)*	✓	✓ *(5)*	✓ *(6)*	✓ *(6)*	✓ *(6)*	✓	✓ *(7)*

Notes to Table 2–7:

(1) To drive inputs higher than V_{CCIO} but less than 4.0 V including the overshoot, disable the I/O clamp diode. However, to drive 5.0-V inputs to the device, enable the I/O clamp diode to prevent V_I from rising above 4.0 V.

(2) When V_{CCIO} = 1.8 V, a MAX II device can drive a 1.5-V device with 1.8-V tolerant inputs.

(3) When V_{CCIO} = 2.5 V, a MAX II device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.

(4) When V_{CCIO} = 3.3 V and a 2.5-V input signal feeds an input pin, the VCCIO supply current will be slightly larger than expected.

(5) MAX II devices can be 5.0-V tolerant with the use of an external resistor and the internal I/O clamp diode on the EPM1270 and EPM2210 devices.

(6) When V_{CCIO} = 3.3 V, a MAX II device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

(7) When V_{CCIO} = 3.3 V, a MAX II device can drive a device with 5.0-V TTL inputs but not 5.0-V CMOS inputs. In the case of 5.0-V CMOS, open-drain setting with internal I/O clamp diode (available only on EPM1270 and EPM2210 devices) and external resistor is required.

For information about output pin source and sink current guidelines, refer to the *AN 428: MAX II CPLD Design Guidelines*.

Referenced Documents

This chapter referenced the following documents:

- *AN 428: MAX II CPLD Design Guidelines*
- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *Hot Socketing and Power-On Reset in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Using User Flash Memory in MAX II Devices* chapter in the *MAX II Device Handbook*

Document Revision History

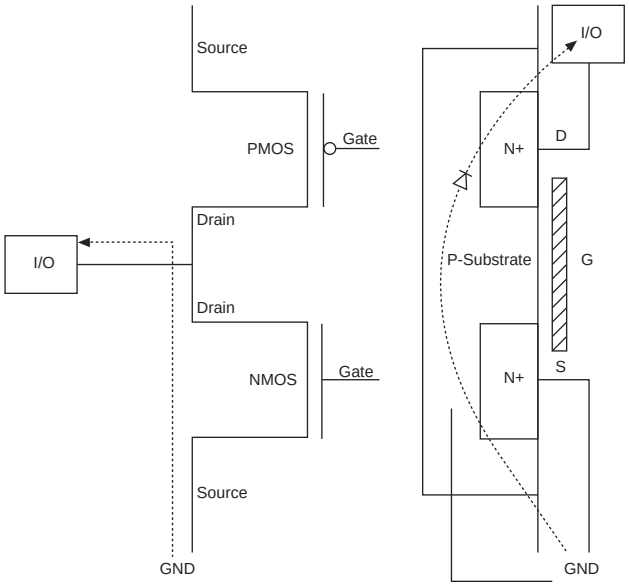
Table 3–5 shows the revision history for this chapter.

Table 3–5. Document Revision History

Date and Revision	Changes Made	Summary of Changes
October 2008, version 1.6	■ Updated New Document Format.	—
December 2007, version 1.5	■ Added warning note after Table 3–1. ■ Updated Table 3–3 and Table 3–4. ■ Added "Referenced Documents" section.	—
December 2006, version 1.4	■ Added document revision history.	—
June 2005, version 1.3	■ Added text and Table 3-4.	—
June 2005, version 1.3	■ Updated text on pages 3-5 to 3-8.	—
June 2004, version 1.1	■ Corrected Figure 3-1. Added CFM acronym.	—

When the I/O pin receives a negative ESD zap at the pin that is less than –0.7 V (0.7 V is the voltage drop across a diode), the intrinsic
P-Substrate/N+ drain diode is forward biased. Therefore, the discharge ESD current path is from GND to the I/O pin, as shown in Figure 4–4.

Figure 4–4. ESD Protection During Negative Voltage Zap



Power-On Reset Circuitry

MAX II devices have POR circuits to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up. The POR circuit monitors these voltages, triggering download from the non-volatile configuration flash memory (CFM) block to the SRAM logic, maintaining tri-state of the I/O pins (with weak pull-up resistors enabled) before and during this process. When the MAX II device enters user mode, the POR circuit releases the I/O pins to user functionality. The POR circuit of the MAX II (except MAX IIZ) device continues to monitor the V_{CCINT} voltage level to detect a brown-out condition. The POR circuit of the MAX IIZ device does not monitor the V_{CCINT} voltage level after the device enters into user mode. More details are provided in the following sub-sections.

Table 5–4. MAX II Device DC Electrical Characteristics *(Note 1)* (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{PULLUP}	I/O pin pull-up resistor current when I/O is unprogrammed	—	—	—	300	µA
C_{IO}	Input capacitance for user I/O pin	—	—	—	8	pF
C_{GCLK}	Input capacitance for dual-purpose GCLK/user I/O pin	—	—	—	8	pF

Notes to Table 5–4:

(1) Typical values are for T_A = 25°C, V_{CCINT} = 3.3 or 2.5 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, or 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(3) V_I = ground, no load, no toggling inputs.

(4) Commercial temperature ranges from 0°C to 85°C with maximum current at 85°C.

(5) Industrial temperature ranges from –40°C to 100°C with maximum current at 100°C.

(6) This value applies to commercial and industrial range devices. For extended temperature range devices, the $V_{SCHMITT}$ typical value is 300 mV for V_{CCIO} = 3.3 V and 120 mV for V_{CCIO} = 2.5 V.

(7) The TCK input is susceptible to high pulse glitches when the input signal fall time is greater than 200 ns for all I/O standards.

(8) This is a peak current value with a maximum duration of t_{CONFIG} time.

(9) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.

Table 5–10. 3.3-V PCI Specifications *(Note 1)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	—	0.5 × V_{CCIO}	—	V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage	—	–0.5	—	0.3 × V_{CCIO}	V
V_{OH}	High-level output voltage	IOH = –500 µA	0.9 × V_{CCIO}	—	—	V
V_{OL}	Low-level output voltage	IOL = 1.5 mA	—	—	0.1 × V_{CCIO}	V

Note to Table 5–10:

(1) 3.3-V PCI I/O standard is only supported in Bank 3 of the EPM1270 and EPM2210 devices.

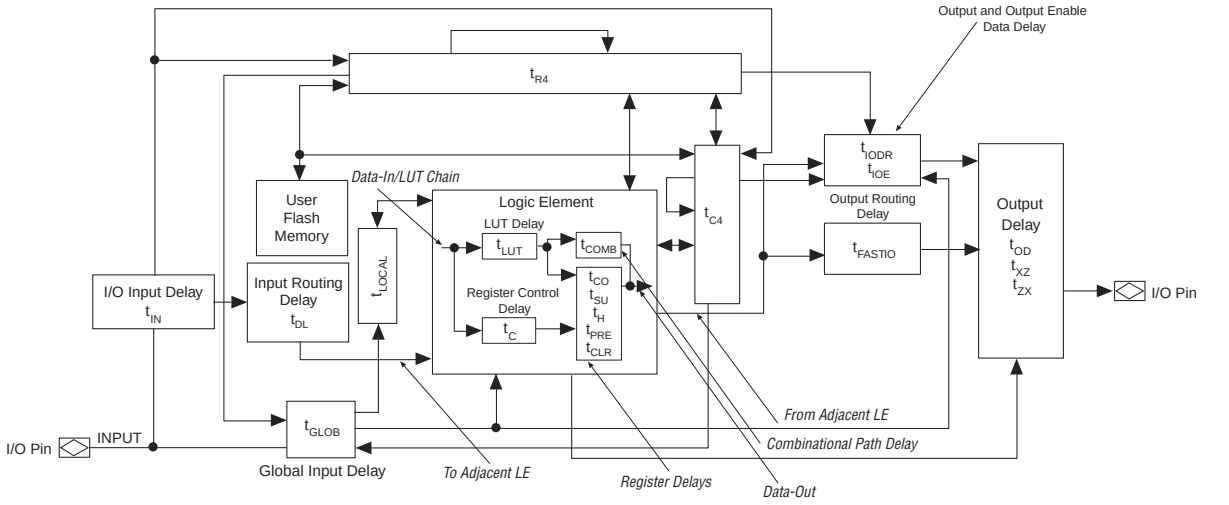
Bus Hold Specifications

Table 5–11 shows the MAX II device family bus hold specifications.

Table 5–11. Bus Hold Specifications

Parameter	Conditions	V_{CCIO} Level								Unit
		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	V_{IN} > V_{IL} (maximum)	20	—	30	—	50	—	70	—	µA
High sustaining current	V_{IN} < V_{IH} (minimum)	–20	—	–30	—	–50	—	–70	—	µA
Low overdrive current	0 V < V_{IN} < V_{CCIO}	—	160	—	200	—	300	—	500	µA
High overdrive current	0 V < V_{IN} < V_{CCIO}	—	–160	—	–200	—	–300	—	–500	µA

Figure 5–2. MAX II Device Timing Model



The timing characteristics of any signal path can be derived from the timing model and parameters of a particular device. External timing parameters, which represent pin-to-pin timing delays, can be calculated as the sum of internal parameters.

Refer to the *Understanding Timing in MAX II Devices* chapter in the *MAX II Device Handbook* for more information.

This section describes and specifies the performance, internal, external, and UFM timing specifications. All specifications are representative of the worst-case supply voltage and junction temperature conditions.

Preliminary and Final Timing

Timing models can have either preliminary or final status. The Quartus II software issues an informational message during the design compilation if the timing models are preliminary. Table 5–13 shows the status of the MAX II device timing models.

Preliminary status means the timing model is subject to change. Initially, timing numbers are created using simulation results, process data, and other known parameters. These tests are used to make the preliminary numbers as close to the actual timing parameters as possible.

Final timing numbers are based on actual device operation and testing. These numbers reflect the actual performance of the device under the worst-case voltage and junction temperature conditions.

Table 5–13. MAX II Device Timing Model Status (Part 1 of 2)

Device	Preliminary	Final
EPM240	—	✓
EPM240Z *(1)*	—	✓
EPM570	—	✓
EPM570Z *(1)*	—	✓

Table 5–17. t_{ZX} IOE Microparameter Adders for Fast Slew Rate (Part 2 of 2)

Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
1.5-V LVCMOS	4 mA	—	1,118	—	1,454	—	1,789	—	580	—	588	—	588	ps
	2 mA	—	2,410	—	3,133	—	3,856	—	915	—	923	—	923	ps
3.3-V PCI	20 mA	—	19	—	25	—	31	—	72	—	71	—	74	ps

Table 5–18. t_{ZX} IOE Microparameter Adders for Slow Slew Rate

Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	6,350	—	6,050	—	5,749	—	5,951	—	5,952	—	6,063	ps
	8 mA	—	9,383	—	9,083	—	8,782	—	6,534	—	6,533	—	6,662	ps
3.3-V LVCMOS	8 mA	—	6,350	—	6,050	—	5,749	—	5,951	—	5,952	—	6,063	ps
	4 mA	—	9,383	—	9,083	—	8,782	—	6,534	—	6,533	—	6,662	ps
2.5-V LVTTL / LVCMOS	14 mA	—	10,412	—	10,112	—	9,811	—	9,110	—	9,105	—	9,237	ps
	7 mA	—	13,613	—	13,313	—	13,012	—	9,830	—	9,835	—	9,977	ps
3.3-V PCI	20 mA	—	–75	—	–97	—	–120	—	6,534	—	6,533	—	6,662	ps

Table 5–19. t_{XZ} IOE Microparameter Adders for Fast Slew Rate

Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	8 mA	—	–56	—	–72	—	–89	—	–69	—	–69	—	–69	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	4 mA	—	–56	—	–72	—	–89	—	–69	—	–69	—	–69	ps
2.5-V LVTTL / LVCMOS	14 mA	—	–3	—	–4	—	–5	—	–7	—	–11	—	–11	ps
	7 mA	—	–47	—	–61	—	–75	—	–66	—	–70	—	–70	ps
1.8-V LVTTL / LVCMOS	6 mA	—	119	—	155	—	191	—	45	—	34	—	37	ps
	3 mA	—	207	—	269	—	331	—	34	—	22	—	25	ps
1.5-V LVCMOS	4 mA	—	606	—	788	—	970	—	166	—	154	—	155	ps
	2 mA	—	673	—	875	—	1,077	—	190	—	177	—	179	ps
3.3-V PCI	20 mA	—	71	—	93	—	114	—	–69	—	–69	—	–69	ps

Table 5–20. t_{XZ} IOE Microparameter Adders for Slow Slew Rate

Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	206	—	–20	—	–247	—	1,433	—	1,446	—	1,454	ps
	8 mA	—	891	—	665	—	438	—	1,332	—	1,345	—	1,348	ps
3.3-V LVCMOS	8 mA	—	206	—	–20	—	–247	—	1,433	—	1,446	—	1,454	ps
	4 mA	—	891	—	665	—	438	—	1,332	—	1,345	—	1,348	ps
2.5-V LVTTL / LVCMOS	14 mA	—	222	—	–4	—	–231	—	213	—	208	—	213	ps
	7 mA	—	943	—	717	—	490	—	166	—	161	—	166	ps
3.3-V PCI	20 mA	—	161	—	210	—	258	—	1,332	—	1,345	—	1,348	ps

☞ The default slew rate setting for MAX II devices in the Quartus II design software is "fast".

Table 5–21. UFM Block Internal Timing Microparameters (Part 1 of 3)

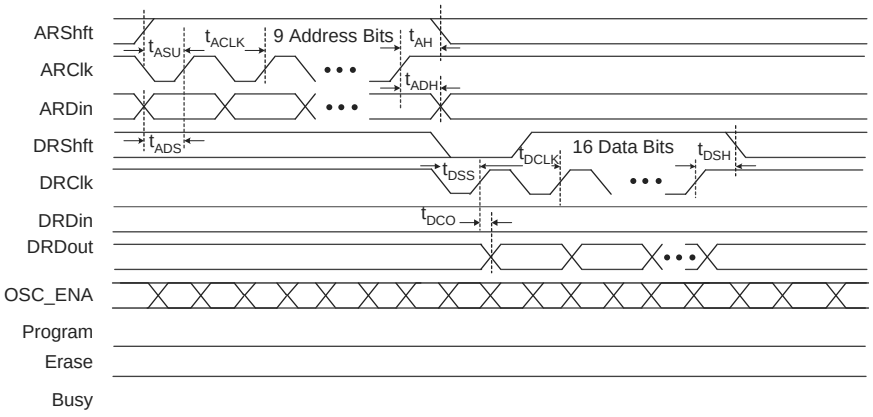
Symbol	Parameter	MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACLK}	Address register clock period	100	—	100	—	100	—	100	—	100	—	100	—	ns
t_{ASU}	Address register shift signal setup to address register clock	20	—	20	—	20	—	20	—	20	—	20	—	ns
t_{AH}	Address register shift signal hold to address register clock	20	—	20	—	20	—	20	—	20	—	20	—	ns
t_{ADS}	Address register data in setup to address register clock	20	—	20	—	20	—	20	—	20	—	20	—	ns
t_{ADH}	Address register data in hold from address register clock	20	—	20	—	20	—	20	—	20	—	20	—	ns
t_{DCLK}	Data register clock period	100	—	100	—	100	—	100	—	100	—	100	—	ns
t_{DSS}	Data register shift signal setup to data register clock	60	—	60	—	60	—	60	—	60	—	60	—	ns
t_{DSH}	Data register shift signal hold from data register clock	20	—	20	—	20	—	20	—	20	—	20	—	ns

Table 5–21. UFM Block Internal Timing Microparameters (Part 3 of 3)

Symbol	Parameter	MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{OE}	Delay from data register clock to data register output	180	—	180	—	180	—	180	—	180	—	180	—	ns
t_{RA}	Maximum read access time	—	65	—	65	—	65	—	65	—	65	—	65	ns
t_{OSCS}	Maximum delay between the OSC_ENA rising edge to the erase/program signal rising edge	250	—	250	—	250	—	250	—	250	—	250	—	ns
t_{OSCH}	Minimum delay allowed from the erase/program signal going low to OSC_ENA signal going low	250	—	250	—	250	—	250	—	250	—	250	—	ns

Figure 5–3 through Figure 5–5 show the read, program, and erase waveforms for UFM block timing parameters shown in Table 5–21.

Figure 5–3. UFM Read Waveforms



6. Reference and Ordering Information

MII51006-1.6

Software

MAX® II devices are supported by the Altera® Quartus® II design software with new, optional MAX+PLUS® II look and feel, which provides HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, and device programming. Refer to the Design Software Selector Guide for more details about the Quartus II software features.

The Quartus II software supports the Windows XP/2000/NT, Sun Solaris, Linux Red Hat v8.0, and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink interface.

Device Pin-Outs

Printed device pin-outs for MAX II devices are available on the Altera website (www.altera.com).

Ordering Information

Figure 6–1 describes the ordering codes for MAX II devices. For more information about a specific package, refer to the *Package Information* chapter in the *MAX II Device Handbook*.

Figure 6–1. MAX II Device Packaging Ordering Information