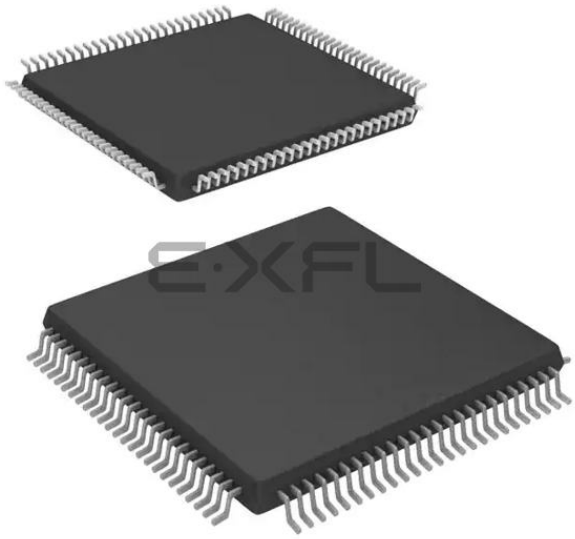

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.4 ns
Voltage Supply - Internal	1.71V ~ 1.89V
Number of Logic Elements/Blocks	570
Number of Macrocells	440
Number of Gates	-
Number of I/O	76
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm570gt100i5n

Table 1–1 shows the MAX II family features.

Table 1–1. MAX II Family Features

Feature	EPM240 EPM240G	EPM570 EPM570G	EPM1270 EPM1270G	EPM2210 EPM2210G	EPM240Z	EPM570Z
LEs	240	570	1,270	2,210	240	570
Typical Equivalent Macrocells	192	440	980	1,700	192	440
Equivalent Macrocell Range	128 to 240	240 to 570	570 to 1,270	1,270 to 2,210	128 to 240	240 to 570
UFM Size (bits)	8,192	8,192	8,192	8,192	8,192	8,192
Maximum User I/O pins	80	160	212	272	80	160
t_{PD1} (ns) *(1)*	4.7	5.4	6.2	7.0	7.5	9.0
f_{CNT} (MHz) *(2)*	304	304	304	304	152	152
t_{SU} (ns)	1.7	1.2	1.2	1.2	2.3	2.2
t_{CO} (ns)	4.3	4.5	4.6	4.6	6.5	6.7

Notes to Table 1–1:

(1) t_{PD1} represents a pin-to-pin delay for the worst case I/O placement with a full diagonal path across the device and combinational logic implemented in a single LUT and LAB that is adjacent to the output pin.

(2) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay will run faster than this number.

For more information about equivalent macrocells, refer to the *MAX II Logic Element to Macrocell Conversion Methodology* white paper.

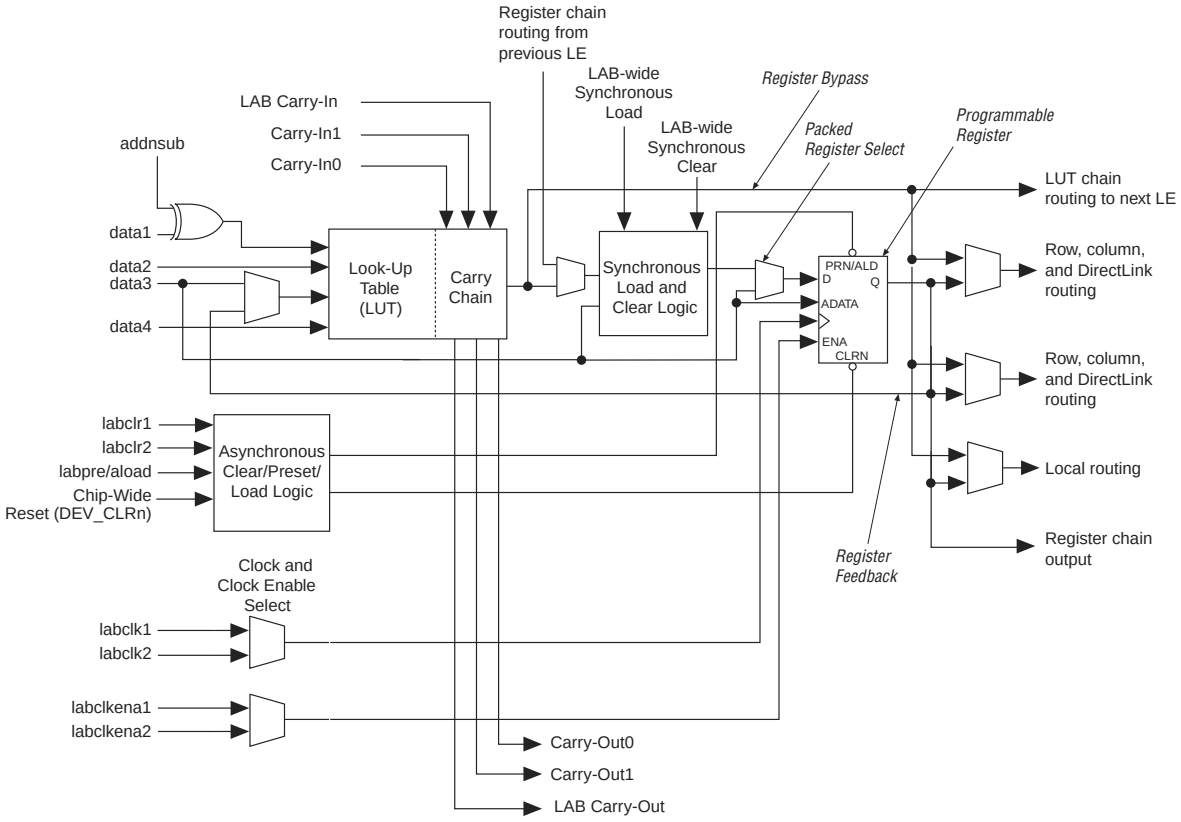
MAX II and MAX IIG devices are available in three speed grades: –3, –4, and –5, with –3 being the fastest. Similarly, MAX IIZ devices are available in three speed grades: –6, –7, and –8, with –6 being the fastest. These speed grades represent the overall relative performance, not any specific timing parameter. For propagation delay timing numbers within each speed grade and density, refer to the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*.

Table 1–2 shows MAX II device speed-grade offerings.

Table 1–2. MAX II Speed Grades

Device	Speed Grade					
	–3	–4	–5	–6	–7	–8
EPM240 EPM240G	✓	✓	✓	—	—	—
EPM570 EPM570G	✓	✓	✓	—	—	—
EPM1270 EPM1270G	✓	✓	✓	—	—	—
EPM2210 EPM2210G	✓	✓	✓	—	—	—
EPM240Z	—	—	—	✓	✓	✓
EPM570Z	—	—	—	✓	✓	✓

Figure 2–6. MAX II LE



Each LE's programmable register can be configured for D, T, JK, or SR operation. Each register has data, true asynchronous load data, clock, clock enable, clear, and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any LE can drive the register's clock and clear control signals. Either general-purpose I/O pins or LEs can drive the clock enable, preset, asynchronous load, and asynchronous data. The asynchronous load data input comes from the data3 input of the LE. For combinational functions, the LUT output bypasses the register and drives directly to the LE outputs.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and DirectLink routing connections and one drives local interconnect resources. This allows the LUT to drive one output while the register drives another output. This register packing feature improves device utilization because the device can use the register and the LUT for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same LE so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

The UFM block communicates with the logic array similar to LAB-to-LAB interfaces. The UFM block connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. This block also has DirectLink interconnects for fast connections to and from a neighboring LAB. For more information about the UFM interface to the logic array, see "User Flash Memory Block" on page 2–18.

Table 2–2 shows the MAX II device routing scheme.

Table 2–2. MAX II Device Routing Scheme

Source	Destination										
	LUT Chain	**Register Chain**	**Local *(1)***	**DirectLink *(1)***	**R4 *(1)***	**C4 *(1)***	**LE**	**UFM Block**	**Column IOE**	**Row IOE**	**Fast I/O *(1)***
LUT Chain	—	—	—	—	—	—	✓	—	—	—	—
Register Chain	—	—	—	—	—	—	✓	—	—	—	—
Local Interconnect	—	—	—	—	—	—	✓	✓	✓	✓	—
DirectLink Interconnect	—	—	✓	—	—	—	—	—	—	—	—
R4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
C4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
LE	✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓
UFM Block	—	—	✓	✓	✓	✓	—	—	—	—	—
Column IOE	—	—	—	—	—	✓	—	—	—	—	—
Row IOE	—	—	—	✓	✓	✓	—	—	—	—	—

Note to Table 2–2:

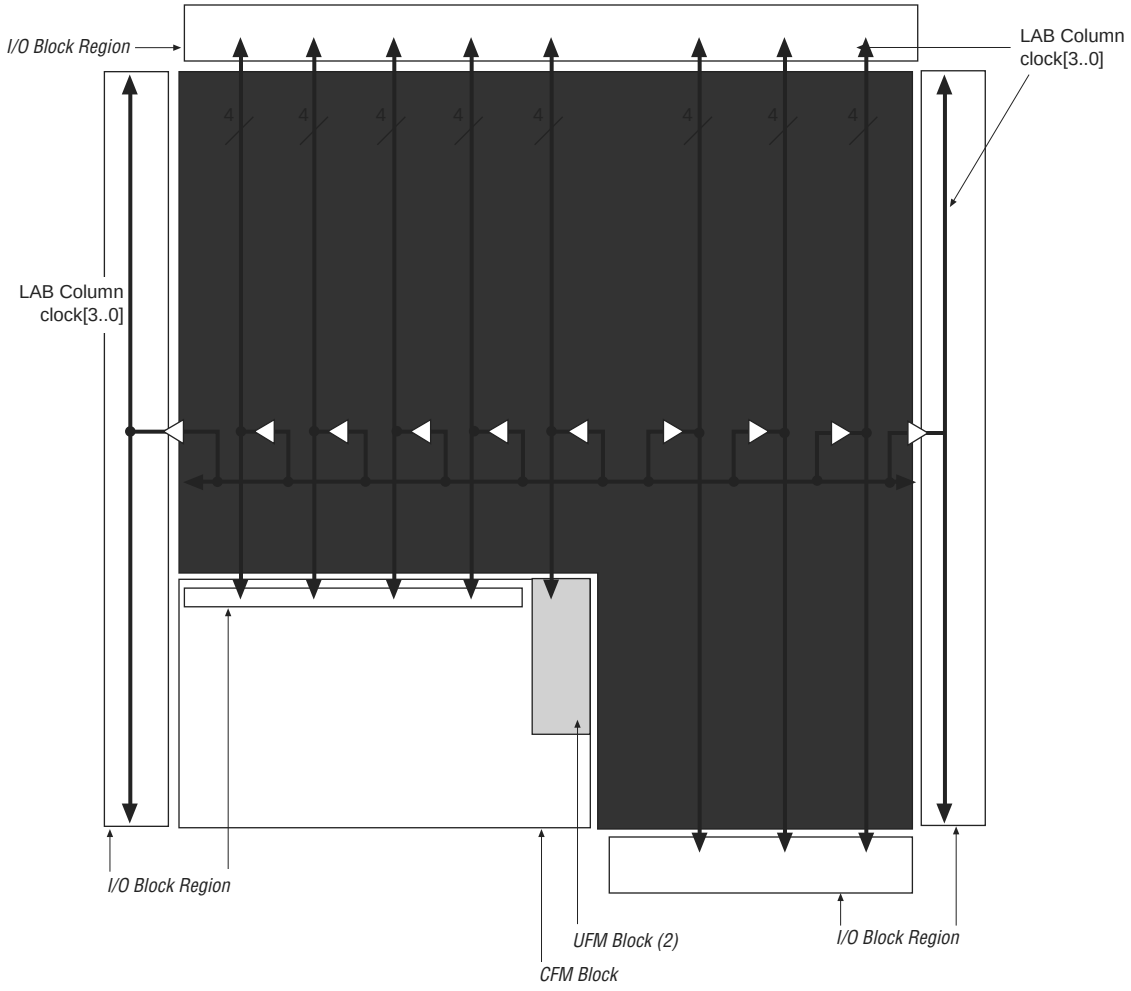
(1) These categories are interconnects.

Global Signals

Each MAX II device has four dual-purpose dedicated clock pins (`GCLK[3..0]`, two pins on the left side and two pins on the right side) that drive the global clock network for clocking, as shown in Figure 2–13. These four pins can also be used as general-purpose I/O if they are not used to drive the global clock network.

The four global clock lines in the global clock network drive throughout the entire device. The global clock network can provide clocks for all resources within the device including LEs, LAB local interconnect, IOEs, and the UFM block. The global clock lines can also be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, or protocol control signals such as `TRDY` and `IRDY` for PCI. Internal logic can drive the global clock network for internally-generated global clocks and control signals. Figure 2–13 shows the various sources that drive the global clock network.

Figure 2–14. Global Clock Network *(Note 1)*



Notes to Figure 2–14:

(1) LAB column clocks in I/O block regions provide high fan-out output enable signals.

(2) LAB column clocks drive to the UFM block.

User Flash Memory Block

MAX II devices feature a single UFM block, which can be used like a serial EEPROM for storing non-volatile information up to 8,192 bits. The UFM block connects to the logic array through the MultiTrack interconnect, allowing any LE to interface to the UFM block. Figure 2–15 shows the UFM block and interface signals. The logic array is used to create customer interface or protocol logic to interface the UFM block data outside of the device. The UFM block offers the following features:

- Non-volatile storage up to 16-bit wide and 8,192 total bits
- Two sectors for partitioned sector erase
- Built-in internal oscillator that optionally drives logic array
- Program, erase, and busy signals

Internal Oscillator

As shown in Figure 2–15, the dedicated circuitry within the UFM block contains an oscillator. The dedicated circuitry uses this internally for its read and program operations. This oscillator's divide by 4 output can drive out of the UFM block as a logic interface clock source or for general-purpose logic clocking. The typical OSC output signal frequency ranges from 3.3 to 5.5 MHz, and its exact frequency of operation is not programmable.

Program, Erase, and Busy Signals

The UFM block's dedicated circuitry automatically generates the necessary internal program and erase algorithm once the PROGRAM or ERASE input signals have been asserted. The PROGRAM or ERASE signal must be asserted until the busy signal deasserts, indicating the UFM internal program or erase operation has completed. The UFM block also supports JTAG as the interface for programming and/or reading.

For more information about programming and erasing the UFM block, refer to the *Using User Flash Memory in MAX II Devices* chapter in the *MAX II Device Handbook*.

Auto-Increment Addressing

The UFM block supports standard read or stream read operations. The stream read is supported with an auto-increment address feature. Deasserting the ARSHIFT signal while clocking the ARCLK signal increments the address register value to read consecutive locations from the UFM array.

Serial Interface

The UFM block supports a serial interface with serial address and data signals. The internal shift registers within the UFM block for address and data are 9 bits and 16 bits wide, respectively. The Quartus II software automatically generates interface logic in LEs for a parallel address and data interface to the UFM block. Other standard protocol interfaces such as SPI are also automatically generated in LE logic by the Quartus II software.

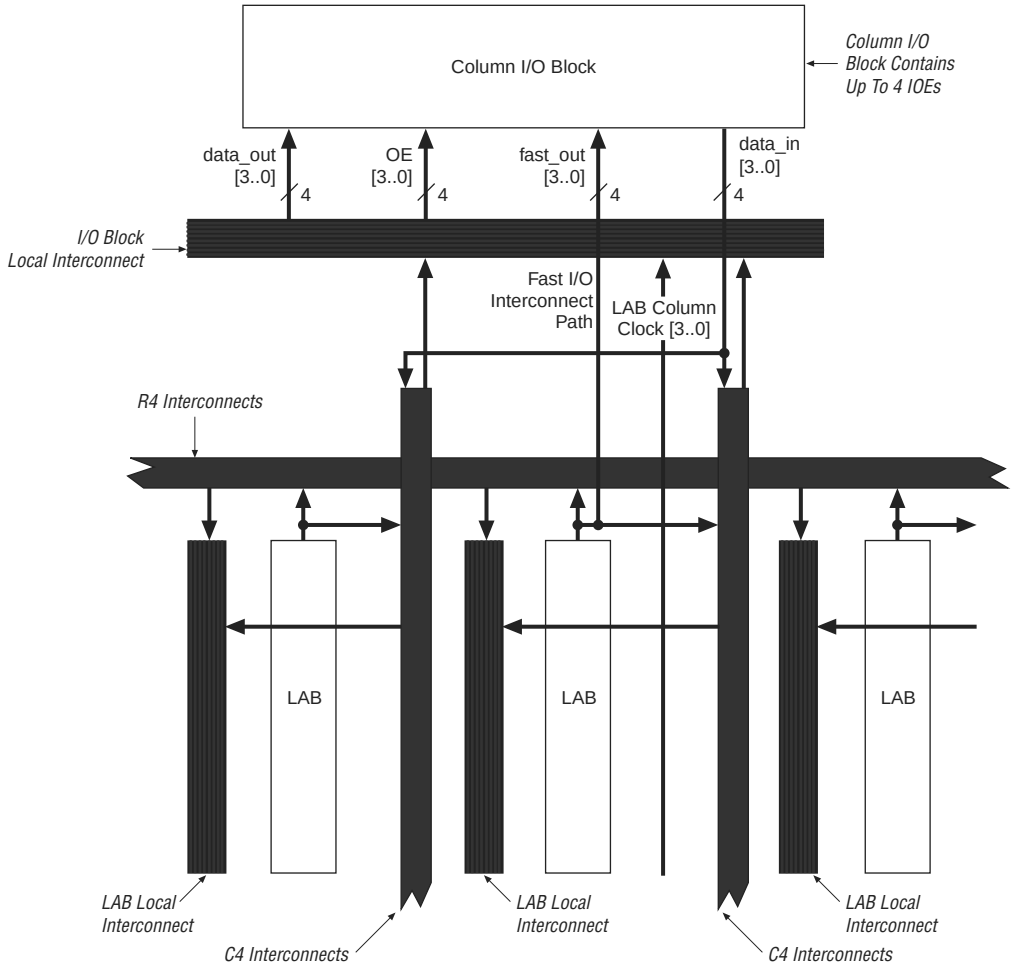
For more information about the UFM interface signals and the Quartus II LE-based alternate interfaces, refer to the *Using User Flash Memory in MAX II Devices* chapter in the *MAX II Device Handbook*.

UFM Block to Logic Array Interface

The UFM block is a small partition of the flash memory that contains the CFM block, as shown in Figure 2–1 and Figure 2–2. The UFM block for the EPM240 device is located on the left side of the device adjacent to the left most LAB column. The UFM block for the EPM570, EPM1270, and EPM2210 devices is located at the bottom left of the device. The UFM input and output signals interface to all types of interconnects (R4 interconnect, C4 interconnect, and DirectLink interconnect to/from adjacent LAB rows). The UFM signals can also be driven from global clocks, GCLK[3..0]. The interface region for the EPM240 device is shown in Figure 2–16. The interface regions for EPM570, EPM1270, and EPM2210 devices are shown in Figure 2–17.

Figure 2–21 shows how a column I/O block connects to the logic array.

Figure 2–21. Column I/O Block Connection to the Interconnect *(Note 1)*



Note to Figure 2–21:

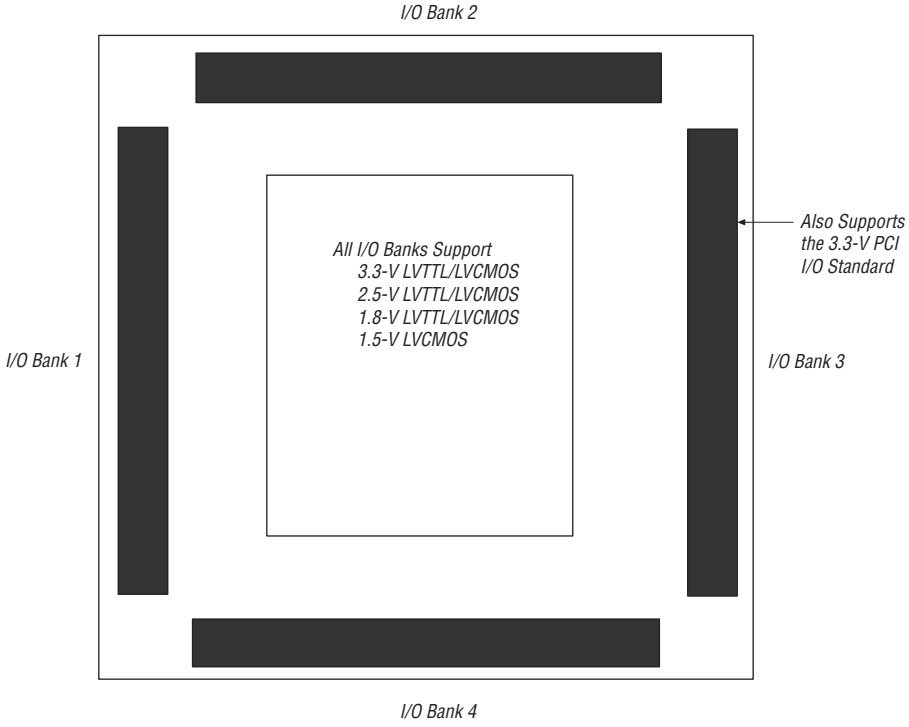
(1) Each of the four IOEs in the column I/O block can have one `data_out` or `fast_out` output, one `OE` output, and one `data_in` input.

I/O Standards and Banks

MAX II device IOEs support the following I/O standards:

- 3.3-V LVTTL/LVCMOS
- 2.5-V LVTTL/LVCMOS
- 1.8-V LVTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI

Figure 2–23. MAX II I/O Banks for EPM1270 and EPM2210 *(Note 1), (2)*



Notes to Figure 2–23:

(1) Figure 2–23 is a top view of the silicon die.

(2) Figure 2–23 is a graphical representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Each I/O bank has dedicated V_{CCIO} pins that determine the voltage standard support in that bank. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each individual bank can support a different standard. Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3 V, Bank 3 can support LVTTL, LVCMOS, and 3.3-V PCI. V_{CCIO} powers both the input and output buffers in MAX II devices.

The JTAG pins for MAX II devices are dedicated pins that cannot be used as regular I/O pins. The pins `TMS`, `TDI`, `TDO`, and `TCK` support all the I/O standards shown in Table 2–4 on page 2–27 except for PCI. These pins reside in Bank 1 for all MAX II devices and their I/O standard support is controlled by the V_{CCIO} setting for Bank 1.

PCI Compliance

The MAX II EPM1270 and EPM2210 devices are compliant with PCI applications as well as all 3.3-V electrical specifications in the *PCI Local Bus Specification Revision 2.2*. These devices are also large enough to support PCI intellectual property (IP) cores. Table 2–5 shows the MAX II device speed grades that meet the PCI timing specifications.

Bus Hold

Each MAX II device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. The designer can select this feature individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the device cannot use the programmable pull-up option.

The bus-hold circuitry uses a resistor to pull the signal level to the last driven state. The *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* gives the specific sustaining current for each V_{CCIO} voltage level driven through this resistor and overdrive current used to identify the next-driven input level.

The bus-hold circuitry is only active after the device has fully initialized. The bus-hold circuit captures the value on the pin present at the moment user mode is entered.

Programmable Pull-Up Resistor

Each MAX II device I/O pin provides an optional programmable pull-up resistor during user mode. If the designer enables this feature for an I/O pin, the pull-up resistor holds the output to the V_{CCIO} level of the output pin's bank.

☞ The programmable pull-up resistor feature should not be used at the same time as the bus-hold feature on a given I/O pin.

Programmable Input Delay

The MAX II IOE includes a programmable input delay that is activated to ensure zero hold times. A path where a pin directly drives a register, with minimal routing between the two, may require the delay to ensure zero hold time. However, a path where a pin drives a register through long routing or through combinational logic may not require the delay to achieve a zero hold time. The Quartus II software uses this delay to ensure zero hold times when needed.

MultiVolt I/O Interface

The MAX II architecture supports the MultiVolt I/O interface feature, which allows MAX II devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation (V_{CCINT}), and up to four sets for input buffers and I/O output driver buffers (V_{CCIO}), depending on the number of I/O banks available in the devices where each set of VCC pins powers one I/O bank. The EPM240 and EPM570 devices have two I/O banks respectively while the EPM1270 and EPM2210 devices have four I/O banks respectively.

Table 3–4 shows the programming times for MAX II devices using in-circuit testers to execute the algorithm vectors in hardware. Software-based programming tools used with download cables are slightly slower because of data processing and transfer limitations.

Table 3–4. MAX II Device Family Programming Times

Description	EPM240 EPM240G EPM240Z	EPM570 EPM570G EPM570Z	EPM1270 EPM1270G	EPM2210 EPM2210G	Unit
Erase + Program (1 MHz)	1.72	2.16	2.90	3.92	sec
Erase + Program (10 MHz)	1.65	1.99	2.58	3.40	sec
Verify (1 MHz)	0.09	0.17	0.30	0.49	sec
Verify (10 MHz)	0.01	0.02	0.03	0.05	sec
Complete Program Cycle (1 MHz)	1.81	2.33	3.20	4.41	sec
Complete Program Cycle (10 MHz)	1.66	2.01	2.61	3.45	sec

UFM Programming

The Quartus II software, with the use of POF, Jam, or JBC files, supports programming of the user flash memory (UFM) block independent of the logic array design pattern stored in the CFM block. This allows updating or reading UFM contents through ISP without altering the current logic array design, or vice versa. By default, these programming files and methods will program the entire flash memory contents, which includes the CFM block and UFM contents. The stand-alone embedded Jam STAPL player and Jam Byte-Code Player provides action commands for programming or reading the entire flash memory (UFM and CFM together) or each independently.

For more information, refer to the *Using Jam STAPL for ISP via an Embedded Processor* chapter in the *MAX II Device Handbook*.

In-System Programming Clamp

By default, the IEEE 1532 instruction used for entering ISP automatically tri-states all I/O pins with weak pull-up resistors for the duration of the ISP sequence. However, some systems may require certain pins on MAX II devices to maintain a specific DC logic level during an in-field update. For these systems, an optional in-system programming clamp instruction exists in MAX II circuitry to control I/O behavior during the ISP sequence. The in-system programming clamp instruction enables the device to sample and sustain the value on an output pin (an input pin would remain tri-stated if sampled) or to explicitly set a logic high, logic low, or tri-state value on any pin. Setting these options is controlled on an individual pin basis using the Quartus II software.

For more information, refer to the *Real-Time ISP and ISP Clamp for MAX II Devices* chapter in the *MAX II Device Handbook*.

Referenced Documents

This chapter refereces the following documents:

- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *Using MAX II Devices in Multi-Voltage Systems* chapter in the *MAX II Device Handbook*

Document Revision History

Table 4–1 shows the revision history for this chapter.

Table 4–1. Document Revision History

Date and Revision	Changes Made	Summary of Changes
October 2008, version2.1	■ Updated "MAX II Hot-Socketing Specifications" and "Power-On Reset Circuitry" sections. ■ Updated New Document Format.	—
December 2007, version 2.0	■ Updated "Hot Socketing Feature Implementation in MAX II Devices" section. ■ Updated "Power-On Reset Circuitry" section. ■ Updated Figure 4–5. ■ Added "Referenced Documents" section.	Updated document with MAX IIZ information.
December 2006, version 1.5	■ Added document revision history.	—
February 2006, version 1.4	■ Updated "MAX II Hot-Socketing Specifications" section. ■ Updated "AC and DC Specifications" section. ■ Updated "Power-On Reset Circuitry" section.	—
June 2005, version 1.3	■ Updated AC and DC specifications on page 4-2.	—
December 2004, version 1.2	■ Added content to Power-Up Characteristics section. ■ Updated Figure 4-5.	—
June 2004, version 1.1	■ Corrected Figure 4-2.	—

Table 5–6. 3.3-V LVCMOS Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, IOH = –0.1 mA *(1)*	V_{CCIO} – 0.2	—	V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, IOL = 0.1 mA *(1)*	—	0.2	V

Table 5–7. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	2.375	2.625	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.5	0.7	V
V_{OH}	High-level output voltage	IOH = –0.1 mA *(1)*	2.1	—	V
		IOH = –1 mA *(1)*	2.0	—	V
		IOH = –2 mA *(1)*	1.7	—	V
V_{OL}	Low-level output voltage	IOL = 0.1 mA *(1)*	—	0.2	V
		IOL = 1 mA *(1)*	—	0.4	V
		IOL = 2 mA *(1)*	—	0.7	V

Table 5–8. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	1.71	1.89	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	2.25 *(2)*	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	IOH = –2 mA *(1)*	V_{CCIO} – 0.45	—	V
V_{OL}	Low-level output voltage	IOL = 2 mA *(1)*	—	0.45	V

Table 5–9. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	1.425	1.575	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	V_{CCIO} + 0.3 *(2)*	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	IOH = –2 mA *(1)*	0.75 × V_{CCIO}	—	V
V_{OL}	Low-level output voltage	IOL = 2 mA *(1)*	—	0.25 × V_{CCIO}	V

Notes to Table 5–5 through Table 5–9:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX II Architecture* chapter (*I/O Structure section*) in the *MAX II Device Handbook*.

(2) This maximum V_{IH} reflects the JEDEC specification. The MAX II input buffer can tolerate a V_{IH} maximum of 4.0, as specified by the V_I parameter in Table 5–2.

Power-Up Timing

Table 5–12 shows the power-up timing characteristics for MAX II devices.

Table 5–12. MAX II Power-Up Timing

Symbol	Parameter	Device	Min	Typ	Max	Unit
t_{CONFIG} *(1)*	The amount of time from when minimum V_{CCINT} is reached until the device enters user mode *(2)*	EPM240	—	—	200	µs
		EPM570	—	—	300	µs
		EPM1270	—	—	300	µs
		EPM2210	—	—	450	µs

Notes to Table 5–12:

(1) Table 5–12 values apply to commercial and industrial range devices. For extended temperature range devices, the t_{CONFIG} maximum values are as follows:

Device	Maximum
EPM240	300 µs
EPM570	400 µs
EPM1270	400 µs
EPM2210	500 µs

(2) For more information about POR trigger voltage, refer to the *Hot Socketing and Power-On Reset in MAX II Devices* chapter in the *MAX II Device Handbook*.

Power Consumption

Designers can use the Altera® PowerPlay Early Power Estimator and PowerPlay Power Analyzer to estimate the device power.

For more information about these power analysis tools, refer to the *Understanding and Evaluating Power in MAX II Devices* chapter in the *MAX II Device Handbook* and the *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*.

Timing Model and Specifications

MAX II devices timing can be analyzed with the Altera Quartus® II software, a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 5–2.

MAX II devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Table 5–13. MAX II Device Timing Model Status (Part 2 of 2)

Device	Preliminary	Final
EPM1270	—	✓
EPM2210	—	✓

Note to Table 5–13:

(1) The MAX IIZ device timing models are only available in the Quartus II software version 8.0 and later.

Performance

Table 5–14 shows the MAX II device performance for some common designs. All performance values were obtained with the Quartus II software compilation of megafunctions. Performance values for –3, –4, and –5 speed grades are based on an EPM1270 device target, while –6, –7, and –8 speed grades are based on an EPM570Z device target.

Table 5–14. MAX II Device Performance

Resource Used	Design Size and Function	Resources Used			Performance						Unit
					MAX II / MAX IIG			MAX IIZ			
		Mode	LEs	UFM Blocks	–3 Speed Grade	–4 Speed Grade	–5 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	
LE	16-bit counter *(1)*	—	16	0	304.0	247.5	201.1	184.1	123.5	118.3	MHz
	64-bit counter *(1)*	—	64	0	201.5	154.8	125.8	83.2	83.2	80.5	MHz
	16-to-1 multiplexer	—	11	0	6.0	8.0	9.3	17.4	17.3	20.4	ns
	32-to-1 multiplexer	—	24	0	7.1	9.0	11.4	12.5	22.8	25.3	ns
	16-bit XOR function	—	5	0	5.1	6.6	8.2	9.0	15.0	16.1	ns
	16-bit decoder with single address line	—	5	0	5.2	6.6	8.2	9.2	15.0	16.1	ns
UFM	512 × 16	None	3	1	10.0	10.0	10.0	10.0	10.0	10.0	MHz
	512 × 16	SPI *(2)*	37	1	8.0	8.0	8.0	9.7	9.7	9.7	MHz
	512 × 8	Parallel *(3)*	73	1	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	MHz
	512 × 16	I^2C *(3)*	142	1	100 *(5)*	100 *(5)*	100 *(5)*	100 *(5)*	100 *(5)*	100 *(5)*	kHz

Notes to Table 5–14:

(1) This design is a binary loadable up counter.

(2) This design is configured for read-only operation in Extended mode. Read and write ability increases the number of LEs used.

(3) This design is configured for read-only operation. Read and write ability increases the number of LEs used.

(4) This design is asynchronous.

(5) The I^2C megafunction is verified in hardware up to 100-kHz serial clock line (SCL) rate.

Table 5–16. IOE Internal Timing Microparameters

Symbol	Parameter	MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{FASTIO}	Data output delay from adjacent LE to I/O block	—	159	—	207	—	254	—	170	—	348	—	428	ps
t_{IN}	I/O input pad and buffer delay	—	708	—	920	—	1,132	—	907	—	970	—	986	ps
t_{GLOB} *(1)*	I/O input pad and buffer delay used as global signal pin	—	1,519	—	1,974	—	2,430	—	2,261	—	2,670	—	3,322	ps
t_{IOE}	Internally generated output enable delay	—	354	—	374	—	460	—	530	—	966	—	1,410	ps
t_{DL}	Input routing delay	—	224	—	291	—	358	—	318	—	410	—	509	ps
t_{OD} *(2)*	Output delay buffer and pad delay	—	1,064	—	1,383	—	1,702	—	1,319	—	1,526	—	1,543	ps
t_{XZ} *(3)*	Output buffer disable delay	—	756	—	982	—	1,209	—	1,045	—	1,264	—	1,276	ps
t_{ZX} *(4)*	Output buffer enable delay	—	1,003	—	1,303	—	1,604	—	1,160	—	1,325	—	1,353	ps

Notes to Table 5–16:

(1) Delay numbers for t_{GLOB} differ for each device density and speed grade. The delay numbers for t_{GLOB}, shown in Table 5–16, are based on an EPM240 device target.

(2) Refer to Table 5–32 and 5–24 for delay adders associated with different I/O standards, drive strengths, and slew rates.

(3) Refer to Table 5–19 and 5–14 for t_{XZ} delay adders associated with different I/O standards, drive strengths, and slew rates.

(4) Refer to Table 5–17 and 5–13 for t_{ZX} delay adders associated with different I/O standards, drive strengths, and slew rates.

Table 5–17 through Table 5–20 show the adder delays for t_{ZX} and t_{XZ} microparameters when using an I/O standard other than 3.3-V LVTTL with 16 mA drive strength.

Table 5–17. t_{ZX} IOE Microparameter Adders for Fast Slew Rate (Part 1 of 2)

Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	8 mA	—	28	—	37	—	45	—	72	—	71	—	74	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	4 mA	—	28	—	37	—	45	—	72	—	71	—	74	ps
2.5-V LVTTL / LVCMOS	14 mA	—	14	—	19	—	23	—	75	—	87	—	90	ps
	7 mA	—	314	—	409	—	503	—	162	—	174	—	177	ps
1.8-V LVTTL / LVCMOS	6 mA	—	450	—	585	—	720	—	279	—	289	—	291	ps
	3 mA	—	1,443	—	1,876	—	2,309	—	499	—	508	—	512	ps

Table 5–23. EPM240 Global Clock External I/O Timing Parameters (Part 2 of 2)

Symbol	Parameter	Condition	MAX II / MAX IIG						MAX IIZ						Unit
			–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	304.0 *(1)*	—	247.5	—	201.1	—	184.1	—	123.5	—	118.3	MHz

Note to Table 5–23:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5–24 shows the external I/O timing parameters for EPM570 devices.

Table 5–24. EPM570 Global Clock External I/O Timing Parameters (Part 1 of 2)

Symbol	Parameter	Condition	MAX II / MAX IIG						MAX IIZ						Unit
			–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through 1 look-up table (LUT)	10 pF	—	5.4	—	7.0	—	8.7	—	9.5	—	15.1	—	17.7	ns
t_{PD2}	Best case pin-to-pin delay through 1 LUT	10 pF	—	3.7	—	4.8	—	5.9	—	5.7	—	7.7	—	8.5	ns
t_{SU}	Global clock setup time	—	1.2	—	1.5	—	1.9	—	2.2	—	3.9	—	4.4	—	ns
t_{H}	Global clock hold time	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	4.5	2.0	5.8	2.0	7.1	2.0	6.7	2.0	8.2	2.0	8.7	ns
t_{CH}	Global clock high time	—	166	—	216	—	266	—	253	—	335	—	339	—	ps
t_{CL}	Global clock low time	—	166	—	216	—	266	—	253	—	335	—	339	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	3.3	—	4.0	—	5.0	—	5.4	—	8.1	—	8.4	—	ns

Table 5–31. MAX II IOE Programmable Delays

Parameter	MAX II / MAX IIG						MAX IIZ						Unit
	–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input Delay from Pin to Internal Cells = 1	—	1,225	—	1,592	—	1,960	—	1,858	—	2,171	—	2,214	ps
Input Delay from Pin to Internal Cells = 0	—	89	—	115	—	142	—	569	—	609	—	616	ps

Maximum Input and Output Clock Rates

Table 5–32 and Table 5–33 show the maximum input and output clock rates for standard I/O pins in MAX II devices.

Table 5–32. MAX II Maximum Input Clock Rate for I/O

I/O Standard		MAX II / MAX IIG			MAX IIZ			Unit
		–3 Speed Grade	–4 Speed Grade	–5 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	
3.3-V LVTTL	Without Schmitt Trigger	304	304	304	304	304	304	MHz
	With Schmitt Trigger	250	250	250	250	250	250	MHz
3.3-V LVCMOS	Without Schmitt Trigger	304	304	304	304	304	304	MHz
	With Schmitt Trigger	250	250	250	250	250	250	MHz
2.5-V LVTTL	Without Schmitt Trigger	220	220	220	220	220	220	MHz
	With Schmitt Trigger	188	188	188	188	188	188	MHz
2.5-V LVCMOS	Without Schmitt Trigger	220	220	220	220	220	220	MHz
	With Schmitt Trigger	188	188	188	188	188	188	MHz
1.8-V LVTTL	Without Schmitt Trigger	200	200	200	200	200	200	MHz
1.8-V LVCMOS	Without Schmitt Trigger	200	200	200	200	200	200	MHz
1.5-V LVCMOS	Without Schmitt Trigger	150	150	150	150	150	150	MHz
3.3-V PCI	Without Schmitt Trigger	304	304	304	304	304	304	MHz

Document Revision History

Table 5–35 shows the revision history for this chapter.

Table 5–35. Document Revision History (Part 1 of 2)

Date and Revision	Changes Made	Summary of Changes
August 2009, version 2.5	■ Added Table 5–28, Table 5–29, and Table 5–30. ■ Updated Table 5–2, Table 5–4, Table 5–14, Table 5–15, Table 5–16, Table 5–17, Table 5–18, Table 5–19, Table 5–20, Table 5–21, Table 5–22, Table 5–23, Table 5–24, Table 5–27, Table 5–31, Table 5–32, and Table 5–33.	Added information for speed grade –8
November 2008, version 2.4	■ Updated Table 5–2. ■ Updated "Internal Timing Parameters" section.	—
October 2008, version 2.3	■ Updated New Document Format. ■ Updated Figure 5–1.	—
July 2008, version 2.2	■ Updated Table 5–14 , Table 5–23 , and Table 5–24.	—
March 2008, version 2.1	■ Added (Note 5) to Table 5–4.	—
December 2007, version 2.0	■ Updated (Note 3) and (4) to Table 5–1. ■ Updated Table 5–2 and added (Note 5). ■ Updated ICCSTANDBY and ICCPOWERUP information and added IPULLUP information in Table 5–4. ■ Added (Note 1) to Table 5–10. ■ Updated Figure 5–2. ■ Added (Note 1) to Table 5–13. ■ Updated Table 5–13 through Table 5–24, and Table 5–27 through Table 5–30. ■ Added tCOMB information to Table 5–15. ■ Updated Figure 5–6. ■ Added "Referenced Documents" section.	Updated document with MAX IIZ information.
December 2006, version 1.8	■ Added note to Table 5–1. ■ Added document revision history.	—
July 2006, version 1.7	■ Minor content and table updates.	—
February 2006, version 1.6	■ Updated "External Timing I/O Delay Adders" section. ■ Updated Table 5–29. ■ Updated Table 5–30.	—
November 2005, version 1.5	■ Updated Tables 5-2, 5-4, and 5-12.	—
August 2005, version 1.4	■ Updated Figure 5-1. ■ Updated Tables 5-13, 5-16, and 5-26. ■ Removed Note 1 from Table 5-12.	—

6. Reference and Ordering Information

MII51006-1.6

Software

MAX® II devices are supported by the Altera® Quartus® II design software with new, optional MAX+PLUS® II look and feel, which provides HDL and schematic design entry, compilation and logic synthesis, full simulation and advanced timing analysis, and device programming. Refer to the Design Software Selector Guide for more details about the Quartus II software features.

The Quartus II software supports the Windows XP/2000/NT, Sun Solaris, Linux Red Hat v8.0, and HP-UX operating systems. It also supports seamless integration with industry-leading EDA tools through the NativeLink interface.

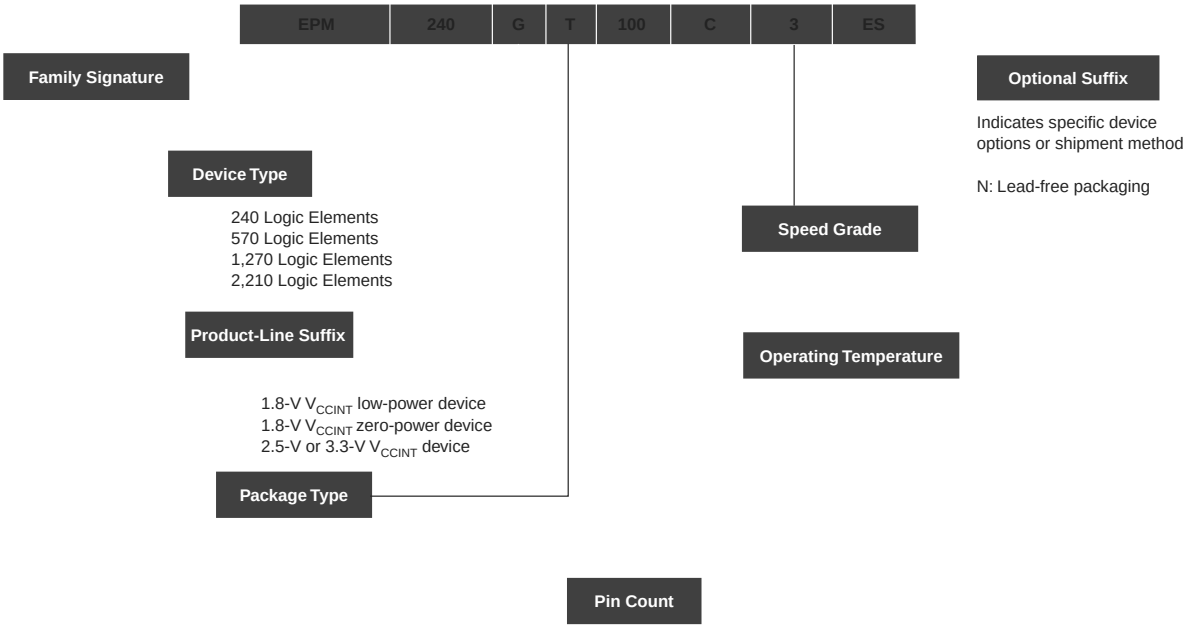
Device Pin-Outs

Printed device pin-outs for MAX II devices are available on the Altera website (www.altera.com).

Ordering Information

Figure 6–1 describes the ordering codes for MAX II devices. For more information about a specific package, refer to the *Package Information* chapter in the *MAX II Device Handbook*.

Figure 6–1. MAX II Device Packaging Ordering Information



Referenced Documents

This chapter references the following document:

- *Package Information* chapter in the *MAX II Device Handbook*

Document Revision History

Table 6–1 shows the revision history for this chapter.

Table 6–1. Document Revision History

Date and Revision	Changes Made	Summary of Changes
August 2009, version 1.6	■ Updated Figure 6–1.	Added information for speed grade –8
October 2008, version 1.5	■ Updated New Document Format.	—
December 2007, version 1.4	■ Added "Referenced Documents" section. ■ Updated Figure 6–1.	Updated document with MAX IIZ information.
December 2006, version 1.3	■ Added document revision history.	—
October 2006, version 1.2	■ Updated Figure 6-1.	—
June 2005, version 1.1	■ Removed Dual Marking section.	—