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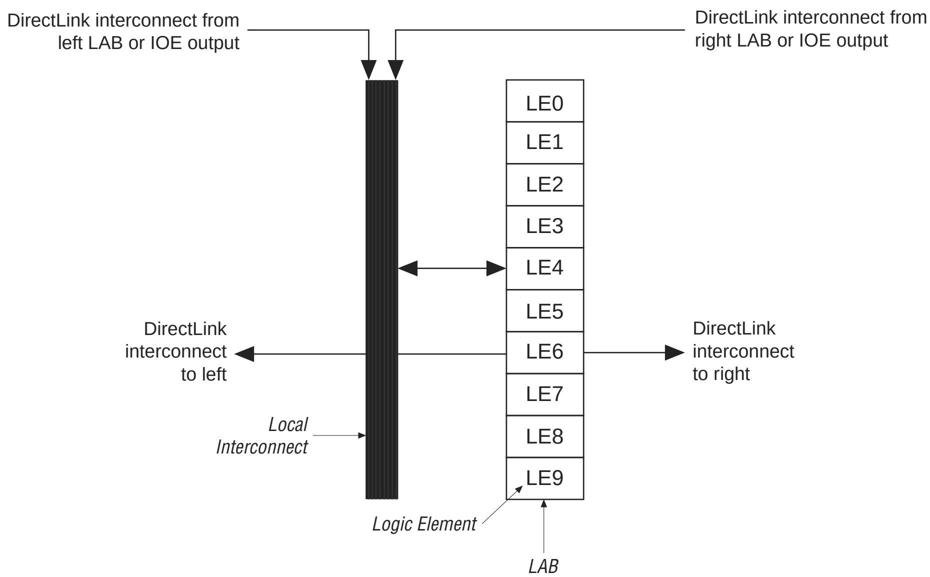
Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.4 ns
Voltage Supply - Internal	1.71V ~ 1.89V
Number of Logic Elements/Blocks	570
Number of Macrocells	440
Number of Gates	-
Number of I/O	116
Operating Temperature	0°C ~ 85°C (TJ)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm570gt144c4

Figure 2–4. DirectLink Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, a synchronous clear, an asynchronous preset/load, a synchronous load, and add/subtract control signals, providing a maximum of 10 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

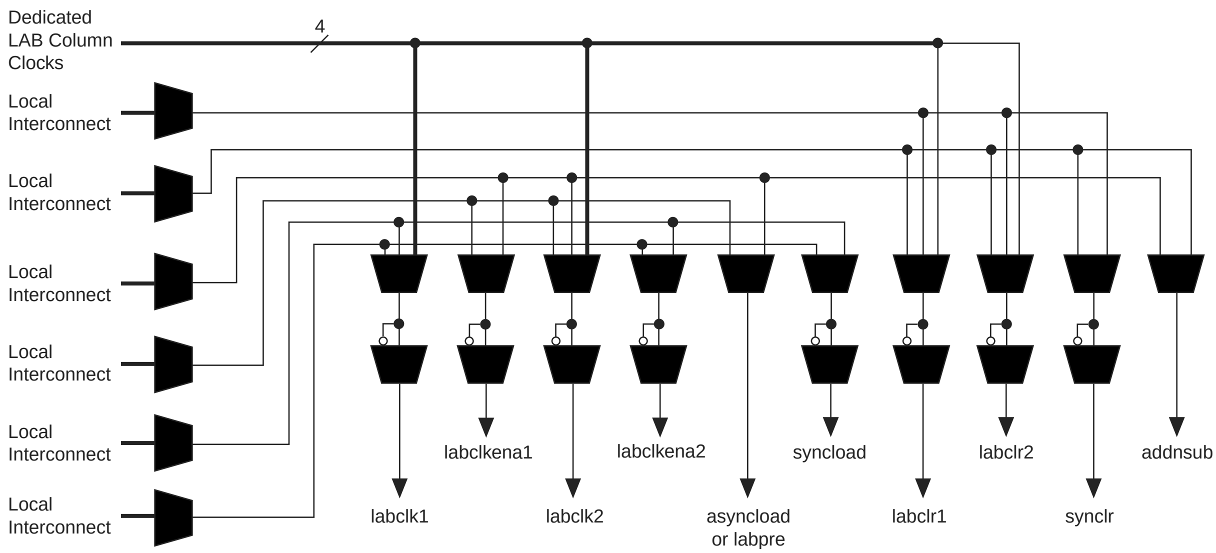
Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. Deasserting the clock enable signal turns off the LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. By default, the Quartus II software uses a `NOT` gate push-back technique to achieve preset. If you disable the `NOT` gate push-back option or assign a given register to power-up high using the Quartus II software, the preset is then achieved using the asynchronous load signal with asynchronous load data input tied high.

With the LAB-wide addnsub control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB column clocks [3..0], driven by the global clock network, and LAB local interconnect generate the LAB-wide control signals. The MultiTrack interconnect structure drives the LAB local interconnect for non-global control signal generation. The MultiTrack interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 2–5 shows the LAB control signal generation circuit.

Figure 2–5. LAB-Wide Control Signals



Logic Elements

The smallest unit of logic in the MAX II architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry-select capability. A single LE also supports dynamic single-bit addition or subtraction mode selectable by an LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and DirectLink interconnects. See Figure 2–6.

The UFM block communicates with the logic array similar to LAB-to-LAB interfaces. The UFM block connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. This block also has DirectLink interconnects for fast connections to and from a neighboring LAB. For more information about the UFM interface to the logic array, see “User Flash Memory Block” on page 2–18.

Table 2–2 shows the MAX II device routing scheme.

Table 2–2. MAX II Device Routing Scheme

Source	Destination										
	LUT Chain	**Register Chain**	**Local** *(1)*	**DirectLink** *(1)*	**R4** *(1)*	**C4** *(1)*	**LE**	**UFM Block**	**Column IOE**	**Row IOE**	**Fast I/O** *(1)*
LUT Chain	—	—	—	—	—	—	✓	—	—	—	—
Register Chain	—	—	—	—	—	—	✓	—	—	—	—
Local Interconnect	—	—	—	—	—	—	✓	✓	✓	✓	—
DirectLink Interconnect	—	—	✓	—	—	—	—	—	—	—	—
R4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
C4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
LE	✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓
UFM Block	—	—	✓	✓	✓	✓	—	—	—	—	—
Column IOE	—	—	—	—	—	✓	—	—	—	—	—
Row IOE	—	—	—	✓	✓	✓	—	—	—	—	—

Note to Table 2–2:

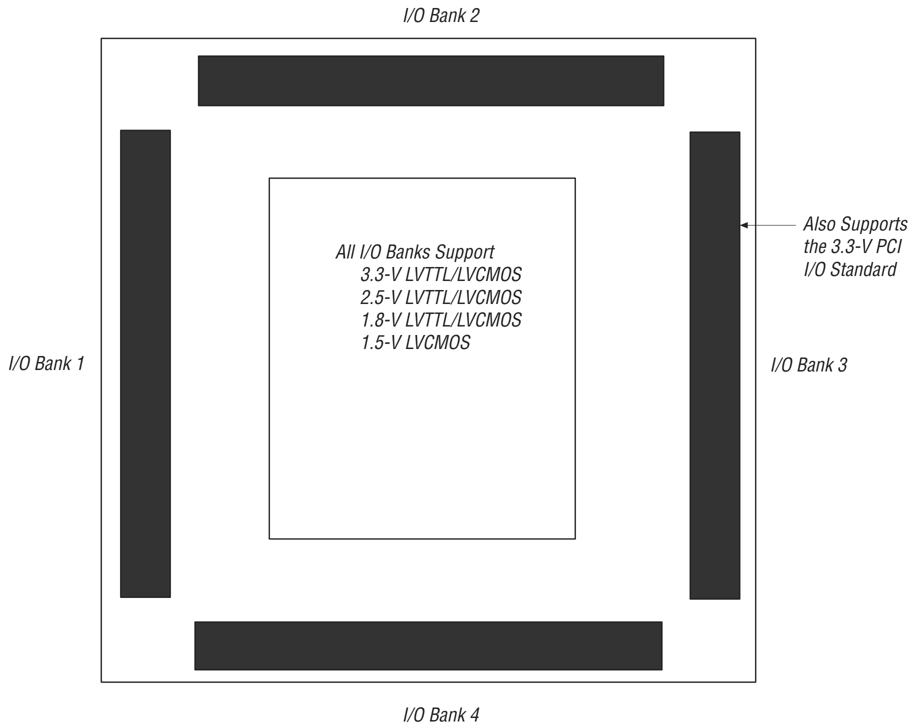
(1) These categories are interconnects.

Global Signals

Each MAX II device has four dual-purpose dedicated clock pins (`GCLK[3..0]`, two pins on the left side and two pins on the right side) that drive the global clock network for clocking, as shown in Figure 2–13. These four pins can also be used as general-purpose I/O if they are not used to drive the global clock network.

The four global clock lines in the global clock network drive throughout the entire device. The global clock network can provide clocks for all resources within the device including LEs, LAB local interconnect, IOEs, and the UFM block. The global clock lines can also be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, or protocol control signals such as `TRDY` and `IRDY` for PCI. Internal logic can drive the global clock network for internally-generated global clocks and control signals. Figure 2–13 shows the various sources that drive the global clock network.

Figure 2–23. MAX II I/O Banks for EPM1270 and EPM2210 *(Note 1)*, *(2)*



Notes to Figure 2–23:

(1) Figure 2–23 is a top view of the silicon die.

(2) Figure 2–23 is a graphical representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Each I/O bank has dedicated V_{CCIO} pins that determine the voltage standard support in that bank. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each individual bank can support a different standard. Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3 V, Bank 3 can support LVTTL, LVCMOS, and 3.3-V PCI. V_{CCIO} powers both the input and output buffers in MAX II devices.

The JTAG pins for MAX II devices are dedicated pins that cannot be used as regular I/O pins. The pins `TMS`, `TDI`, `TDO`, and `TCK` support all the I/O standards shown in Table 2–4 on page 2–27 except for PCI. These pins reside in Bank 1 for all MAX II devices and their I/O standard support is controlled by the V_{CCIO} setting for Bank 1.

PCI Compliance

The MAX II EPM1270 and EPM2210 devices are compliant with PCI applications as well as all 3.3-V electrical specifications in the *PCI Local Bus Specification Revision 2.2*. These devices are also large enough to support PCI intellectual property (IP) cores. Table 2–5 shows the MAX II device speed grades that meet the PCI timing specifications.

Table 2–5. MAX II Devices and Speed Grades that Support 3.3-V PCI Electrical Specifications and Meet PCI Timing

Device	33-MHz PCI	66-MHz PCI
EPM1270	All Speed Grades	–3 Speed Grade
EPM2210	All Speed Grades	–3 Speed Grade

Schmitt Trigger

The input buffer for each MAX II device I/O pin has an optional Schmitt trigger setting for the 3.3-V and 2.5-V standards. The Schmitt trigger allows input buffers to respond to slow input edge rates with a fast output edge rate. Most importantly, Schmitt triggers provide hysteresis on the input buffer, preventing slow-rising noisy input signals from ringing or oscillating on the input signal driven into the logic array. This provides system noise tolerance on MAX II inputs, but adds a small, nominal input delay.

The JTAG input pins (`TMS`, `TCK`, and `TDI`) have Schmitt trigger buffers that are always enabled.

☞ The `TCK` input is susceptible to high pulse glitches when the input signal fall time is greater than 200 ns for all I/O standards.

Output Enable Signals

Each MAX II IOE output buffer supports output enable signals for tri-state control. The output enable signal can originate from the `GCLK[3..0]` global signals or from the MultiTrack interconnect. The MultiTrack interconnect routes output enable signals and allows for a unique output enable for each output or bidirectional pin.

MAX II devices also provide a chip-wide output enable pin (`DEV_OE`) to control the output enable for every output pin in the design. An option set before compilation in the Quartus II software controls this pin. This chip-wide output enable uses its own routing resources and does not use any of the four global resources. If this option is turned on, all outputs on the chip operate normally when `DEV_OE` is asserted. When the pin is deasserted, all outputs are tri-stated. If this option is turned off, the `DEV_OE` pin is disabled when the device operates in user mode and is available as a user I/O pin.

Programmable Drive Strength

The output buffer for each MAX II device I/O pin has two levels of programmable drive strength control for each of the LVTTL and LVCMOS I/O standards. Programmable drive strength provides system noise reduction control for high performance I/O designs. Although a separate slew-rate control feature exists, using the lower drive strength setting provides signal slew-rate control to reduce system noise and signal overshoot without the large delay adder associated with the slew-rate control feature. Table 2–6 shows the possible settings for the I/O standards with drive strength control. The Quartus II software uses the maximum current strength as the default setting. The PCI I/O standard is always set at 20 mA with no alternate setting.

Table 2–6. Programmable Drive Strength *(Note 1)*

I/O Standard	IOH/IOL Current Strength Setting (mA)
3.3-V LVTTL	16
	8
3.3-V LVCMOS	8
	4
2.5-V LVTTL/LVCMOS	14
	7
1.8-V LVTTL/LVCMOS	6
	3
1.5-V LVCMOS	4
	2

Note to Table 2–6:

(1) The I_{OH} current strength numbers shown are for a condition of a $V_{OUT} = V_{OH}$ minimum, where the V_{OH} minimum is specified by the I/O standard. The I_{OL} current strength numbers shown are for a condition of a $V_{OUT} = V_{OL}$ maximum, where the V_{OL} maximum is specified by the I/O standard. For 2.5-V LVTTL/LVCMOS, the I_{OH} condition is V_{OUT} = 1.7 V and the I_{OL} condition is V_{OUT} = 0.7 V.

Slew-Rate Control

The output buffer for each MAX II device I/O pin has a programmable output slew-rate control that can be configured for low noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal output delay to rising and falling edges. The lower the voltage standard (for example, 1.8-V LVTTL) the larger the output delay when slow slew is enabled. Each I/O pin has an individual slew-rate control, allowing the designer to specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges.

Open-Drain Output

MAX II devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that can be asserted by any of several devices. This output can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX II devices can be used as an additional ground pin. This programmable ground feature does not require the use of the associated LEs in the device. In the Quartus II software, unused pins can be set as programmable GND on a global default basis or they can be individually assigned. Unused pins also have the option of being set as tri-stated input pins.

3. JTAG and In-System Programmability

MII51003-1.6

Introduction

This chapter discusses how to use the IEEE Standard 1149.1 Boundary-Scan Test (BST) circuitry in MAX II devices and includes the following sections:

- "IEEE Std. 1149.1 (JTAG) Boundary-Scan Support" on page 3–1
- "In System Programmability" on page 3–4

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All MAX® II devices provide Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry that complies with the IEEE Std. 1149.1-2001 specification. JTAG boundary-scan testing can only be performed at any time after V_{CCINT} and all V_{CCIO} banks have been fully powered and a t_{CONFIG} amount of time has passed. MAX II devices can also use the JTAG port for in-system programming together with either the Quartus® II software or hardware using Programming Object Files (**.pof**), JamTM Standard Test and Programming Language (STAPL) Files (**.jam**), or Jam Byte-Code Files (**.jbc**).

The JTAG pins support 1.5-V, 1.8-V, 2.5-V, or 3.3-V I/O standards. The supported voltage level and standard are determined by the V_{CCIO} of the bank where it resides. The dedicated JTAG pins reside in Bank 1 of all MAX II devices.

MAX II devices support the JTAG instructions shown in Table 3–1.

Table 3–1. MAX II JTAG Instructions (Part 1 of 2)

JTAG Instruction	Instruction Code	Description
`SAMPLE/PRELOAD`	`00 0000 0101`	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
`EXTEST` *(1)*	`00 0000 1111`	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
`BYPASS`	`11 1111 1111`	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
`USERCODE`	`00 0000 0111`	Selects the 32-bit `USERCODE` register and places it between the `TDI` and `TDO` pins, allowing the `USERCODE` to be serially shifted out of `TDO`. This register defaults to all 1's if not specified in the Quartus II software.
`IDCODE`	`00 0000 0110`	Selects the `IDCODE` register and places it between `TDI` and `TDO`, allowing the `IDCODE` to be serially shifted out of `TDO`.
`HIGHZ` *(1)*	`00 0000 1011`	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the boundary scan test data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.

Table 3–1. MAX II JTAG Instructions (Part 2 of 2)

JTAG Instruction	Instruction Code	Description
CLAMP *(1)*	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the boundary scan test data to pass synchronously through selected devices to adjacent devices during normal device operation, while holding I/O pins to a state defined by the data in the boundary-scan register.
USER0	00 0000 1100	This instruction allows you to define the scan chain between TDI and TDO in the MAX II logic array. This instruction is also used for custom logic and JTAG interfaces.
USER1	00 0000 1110	This instruction allows you to define the scan chain between TDI and TDO in the MAX II logic array. This instruction is also used for custom logic and JTAG interfaces.
IEEE 1532 instructions	*(2)*	IEEE 1532 ISC instructions used when programming a MAX II device via the JTAG port.

Notes to Table 3–1:

(1) HIGHZ, CLAMP, and EXTEST instructions do not disable weak pull-up resistors or bus hold features.

(2) These instructions are shown in the 1532 BSDL files, which will be posted on the Altera® website at www.altera.com when they are available.

Unsupported JTAG instructions should not be issued to the MAX II device as this may put the device into an unknown state, requiring a power cycle to recover device operation.

The MAX II device instruction register length is 10 bits and the USERCODE register length is 32 bits. Table 3–2 and Table 3–3 show the boundary-scan register length and device IDCODE information for MAX II devices.

Table 3–2. MAX II Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM240	240
EPM570	480
EPM1270	636
EPM2210	816

Table 3–3. 32-Bit MAX II Device IDCODE (Part 1 of 2)

Device	Binary IDCODE (32 Bits) *(1)*				HEX IDCODE
	Version (4 Bits)	Part Number	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*	
EPM240 EPM240G	0000	0010 0000 1010 0001	000 0110 1110	1	0x020A10DD
EPM570 EPM570G	0000	0010 0000 1010 0010	000 0110 1110	1	0x020A20DD
EPM1270 EPM1270G	0000	0010 0000 1010 0011	000 0110 1110	1	0x020A30DD
EPM2210 EPM2210G	0000	0010 0000 1010 0100	000 0110 1110	1	0x020A40DD

IEEE 1532 Support

The JTAG circuitry and ISP instruction set in MAX II devices is compliant to the IEEE 1532-2002 programming specification. This provides industry-standard hardware and software for in-system programming among multiple vendor programmable logic devices (PLDs) in a JTAG chain.

The MAX II 1532 BSDL files will be released on the Altera website when available.

Jam Standard Test and Programming Language (STAPL)

The Jam STAPL JEDEC standard, JESD71, can be used to program MAX II devices with in-circuit testers, PCs, or embedded processors. The Jam byte code is also supported for MAX II devices. These software programming protocols provide a compact embedded solution for programming MAX II devices.

For more information, refer to the *Using Jam STAPL for ISP via an Embedded Processor* chapter in the *MAX II Device Handbook*.

Programming Sequence

During in-system programming, 1532 instructions, addresses, and data are shifted into the MAX II device through the `TDI` input pin. Data is shifted out through the `TDO` output pin and compared against the expected data. Programming a pattern into the device requires the following six ISP steps. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6. These steps are automatically executed by third-party programmers, the Quartus II software, or the Jam STAPL and Jam Byte-Code Players.

1. *Enter ISP*—The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode.
2. *Check ID*—Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Sector Erase*—Erasing the device in-system involves shifting in the instruction to erase the device and applying an erase pulse(s). The erase pulse is automatically generated internally by waiting in the run/test/idle state for the specified erase pulse time of 500 ms for the CFM block and 500 ms for each sector of the UFM block.
4. *Program*—Programming the device in-system involves shifting in the address, data, and program instruction and generating the program pulse to program the flash cells. The program pulse is automatically generated internally by waiting in the run/test/idle state for the specified program pulse time of 75 µs. This process is repeated for each address in the CFM and UFM blocks.
5. *Verify*—Verifying a MAX II device in-system involves shifting in addresses, applying the verify instruction to generate the read pulse, and shifting out the data for comparison. This process is repeated for each CFM and UFM address.
6. *Exit ISP*—An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode.

Real-Time ISP

For systems that require more than DC logic level control of I/O pins, the real-time ISP feature allows you to update the CFM block with a new design image while the current design continues to operate in the SRAM logic array and I/O pins. A new programming file is updated into the MAX II device without halting the original design's operation, saving down-time costs for remote or field upgrades. The updated CFM block configures the new design into the SRAM upon the next power cycle. It is also possible to execute an immediate configuration of the SRAM without a power cycle by using a specific sequence of ISP commands. The configuration of SRAM without a power cycle takes a specific amount of time (t_{CONFIG}). During this time, the I/O pins are tri-stated and weakly pulled-up to V_{CCIO}.

Design Security

All MAX II devices contain a programmable security bit that controls access to the data programmed into the CFM block. When this bit is programmed, design programming information, stored in the CFM block, cannot be copied or retrieved. This feature provides a high level of design security because programmed data within flash memory cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is erased. The SRAM is also invisible and cannot be accessed regardless of the security bit setting. The UFM block data is not protected by the security bit and is accessible through JTAG or logic array connections.

Programming with External Hardware

MAX II devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera® ByteblasterMV™, MasterBlaster™, ByteBlaster™ II, and USB-Blaster cables.

BP Microsystems, System General, and other programming hardware manufacturers provide programming support for Altera devices. Check their websites for device support information.

Referenced Documents

This chapter references the following documents:

- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *IEEE 1149.1 (JTAG) Boundary-Scan Testing for MAX II Devices* chapter in the *MAX II Device Handbook*
- *Real-Time ISP and ISP Clamp for MAX II Devices* chapter in the *MAX II Device Handbook*
- *Using Jam STAPL for ISP via an Embedded Processor* chapter in the *MAX II Device Handbook*

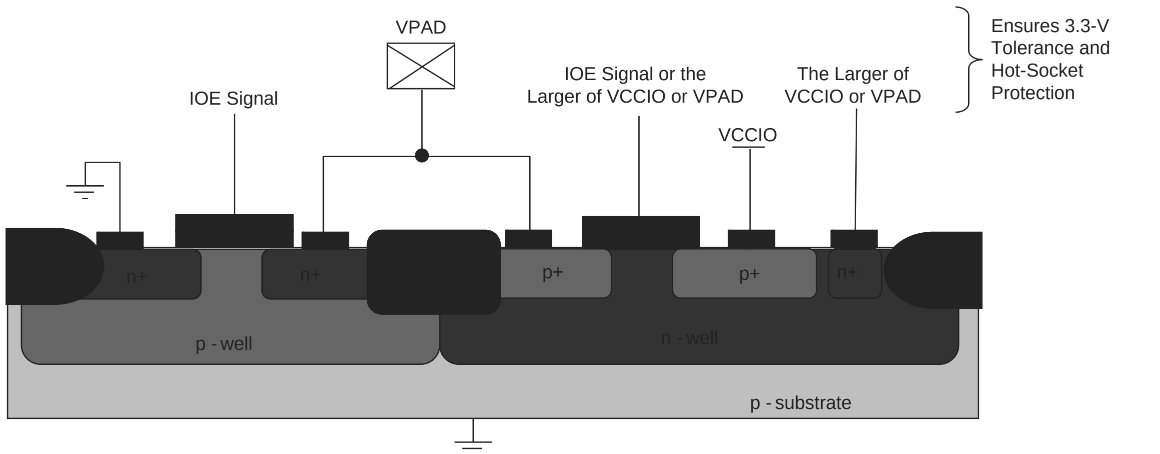
Document Revision History

Table 3–5 shows the revision history for this chapter.

Table 3–5. Document Revision History

Date and Revision	Changes Made	Summary of Changes
October 2008, version 1.6	■ Updated New Document Format.	—
December 2007, version 1.5	■ Added warning note after Table 3–1. ■ Updated Table 3–3 and Table 3–4. ■ Added "Referenced Documents" section.	—
December 2006, version 1.4	■ Added document revision history.	—
June 2005, version 1.3	■ Added text and Table 3-4.	—
June 2005, version 1.3	■ Updated text on pages 3-5 to 3-8.	—
June 2004, version 1.1	■ Corrected Figure 3-1. Added CFM acronym.	—

Figure 4–2. Transistor-Level Diagram of MAX II Device I/O Buffers



The CMOS output drivers in the I/O pins intrinsically provide electrostatic discharge (ESD) protection. There are two cases to consider for ESD voltage strikes: positive voltage zap and negative voltage zap.

A positive ESD voltage zap occurs when a positive voltage is present on an I/O pin due to an ESD charge event. This can cause the N+ (Drain)/ P-Substrate junction of the N-channel drain to break down and the N+ (Drain)/P-Substrate/N+ (Source) intrinsic bipolar transistor turn on to discharge ESD current from I/O pin to GND. The dashed line (see Figure 4–3) shows the ESD current discharge path during a positive ESD zap.

Figure 4–3. ESD Protection During Positive Voltage Zap

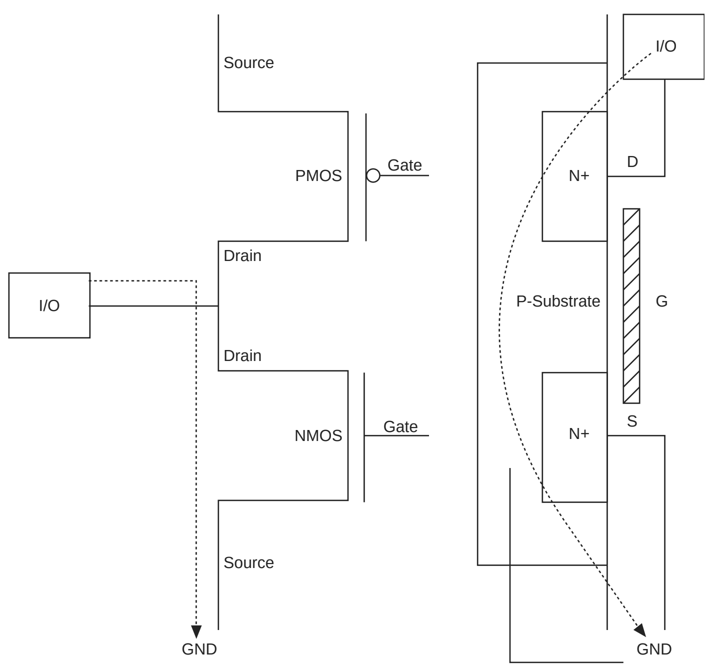
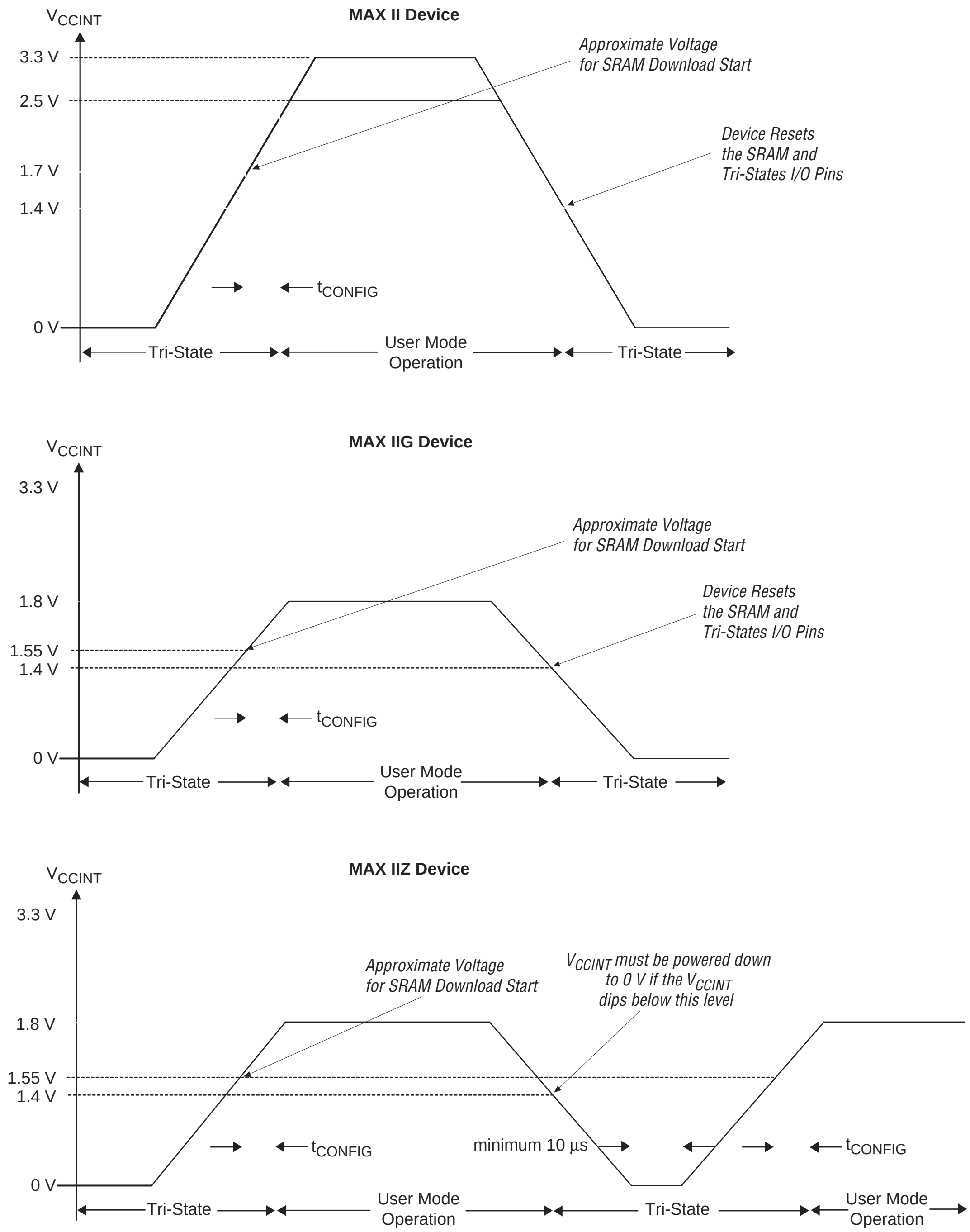


Figure 4–5. Power-Up Characteristics for MAX II, MAX IIG, and MAX IIZ Devices *(Note 1)*, *(2)*



Notes to Figure 4–5:

(1) Time scale is relative.

(2) Figure 4–5 assumes all V_{CCIO} banks power up simultaneously with the V_{CCINT} profile shown. If not, t_{CONFIG} stretches out until all V_{CCIO} banks are powered.

☞ After SRAM configuration, all registers in the device are cleared and released into user function before I/O tri-states are released. To release clears after tri-states are released, use the `DEV_CLRn` pin option. To hold the tri-states beyond the power-up configuration time, use the `DEV_OE` pin option.

Table 5–10. 3.3-V PCI Specifications *(Note 1)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	3.0	3.3	3.6	V
V_{IH}	High-level input voltage	—	0.5 × V_{CCIO}	—	V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage	—	–0.5	—	0.3 × V_{CCIO}	V
V_{OH}	High-level output voltage	IOH = –500 µA	0.9 × V_{CCIO}	—	—	V
V_{OL}	Low-level output voltage	IOL = 1.5 mA	—	—	0.1 × V_{CCIO}	V

Note to Table 5–10:

(1) 3.3-V PCI I/O standard is only supported in Bank 3 of the EPM1270 and EPM2210 devices.

Bus Hold Specifications

Table 5–11 shows the MAX II device family bus hold specifications.

Table 5–11. Bus Hold Specifications

Parameter	Conditions	V_{CCIO} Level								Unit
		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	$V_{IN} > V_{IL}$ (maximum)	20	—	30	—	50	—	70	—	µA
High sustaining current	$V_{IN} < V_{IH}$ (minimum)	–20	—	–30	—	–50	—	–70	—	µA
Low overdrive current	0 V < V_{IN} < V_{CCIO}	—	160	—	200	—	300	—	500	µA
High overdrive current	0 V < V_{IN} < V_{CCIO}	—	–160	—	–200	—	–300	—	–500	µA

Table 5–13. MAX II Device Timing Model Status (Part 2 of 2)

Device	Preliminary	Final
EPM1270	—	✓
EPM2210	—	✓

Note to Table 5–13:

(1) The MAX IIZ device timing models are only available in the Quartus II software version 8.0 and later.

Performance

Table 5–14 shows the MAX II device performance for some common designs. All performance values were obtained with the Quartus II software compilation of megafunctions. Performance values for –3, –4, and –5 speed grades are based on an EPM1270 device target, while –6, –7, and –8 speed grades are based on an EPM570Z device target.

Table 5–14. MAX II Device Performance

Resource Used	Design Size and Function	Resources Used			Performance						Unit
					MAX II / MAX IIG			MAX IIZ			
		Mode	LEs	UFM Blocks	–3 Speed Grade	–4 Speed Grade	–5 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	
LE	16-bit counter *(1)*	—	16	0	304.0	247.5	201.1	184.1	123.5	118.3	MHz
	64-bit counter *(1)*	—	64	0	201.5	154.8	125.8	83.2	83.2	80.5	MHz
	16-to-1 multiplexer	—	11	0	6.0	8.0	9.3	17.4	17.3	20.4	ns
	32-to-1 multiplexer	—	24	0	7.1	9.0	11.4	12.5	22.8	25.3	ns
	16-bit XOR function	—	5	0	5.1	6.6	8.2	9.0	15.0	16.1	ns
	16-bit decoder with single address line	—	5	0	5.2	6.6	8.2	9.2	15.0	16.1	ns
UFM	512 × 16	None	3	1	10.0	10.0	10.0	10.0	10.0	10.0	MHz
	512 × 16	SPI *(2)*	37	1	8.0	8.0	8.0	9.7	9.7	9.7	MHz
	512 × 8	Parallel *(3)*	73	1	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	MHz
	512 × 16	I²C *(3)*	142	1	100 *(5)*	100 *(5)*	100 *(5)*	100 *(5)*	100 *(5)*	100 *(5)*	kHz

Notes to Table 5–14:

(1) This design is a binary loadable up counter.
(2) This design is configured for read-only operation in Extended mode. Read and write ability increases the number of LEs used.
(3) This design is configured for read-only operation. Read and write ability increases the number of LEs used.
(4) This design is asynchronous.
(5) The I²C megafunction is verified in hardware up to 100-kHz serial clock line (SCL) rate.

Table 5–21. UFM Block Internal Timing Microparameters (Part 2 of 3)

Symbol	Parameter	MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{DDS}	Data register data in setup to data register clock	20	—	20	—	20	—	20	—	20	—	20	—	ns
t_{DDH}	Data register data in hold from data register clock	20	—	20	—	20	—	20	—	20	—	20	—	ns
t_{DP}	Program signal to data clock hold time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{PB}	Maximum delay between program rising edge to UFM busy signal rising edge	—	960	—	960	—	960	—	960	—	960	—	960	ns
t_{BP}	Minimum delay allowed from UFM busy signal going low to program signal going low	20	—	20	—	20	—	20	—	20	—	20	—	ns
t_{PPMX}	Maximum length of busy pulse during a program	—	100	—	100	—	100	—	100	—	100	—	100	µs
t_{AE}	Minimum erase signal to address clock hold time	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{EB}	Maximum delay between the erase rising edge to the UFM busy signal rising edge	—	960	—	960	—	960	—	960	—	960	—	960	ns
t_{BE}	Minimum delay allowed from the UFM busy signal going low to erase signal going low	20	—	20	—	20	—	20	—	20	—	20	—	ns
t_{EPMX}	Maximum length of busy pulse during an erase	—	500	—	500	—	500	—	500	—	500	—	500	ms
t_{DCO}	Delay from data register clock to data register output	—	5	—	5	—	5	—	5	—	5	—	5	ns

External Timing Parameters

External timing parameters are specified by device density and speed grade. All external I/O timing parameters shown are for the 3.3-V LVTTL I/O standard with the maximum drive strength and fast slew rate. For external I/O timing using standards other than LVTTL or for different drive strengths, use the I/O standard input and output delay adders in Table 5–27 through Table 5–31.

For more information about each external timing parameters symbol, refer to the *Understanding Timing in MAX II Devices* chapter in the *MAX II Device Handbook*.

Table 5–23 shows the external I/O timing parameters for EPM240 devices.

Table 5–23. EPM240 Global Clock External I/O Timing Parameters (Part 1 of 2)

			MAX II / MAX IIG						MAX IIZ						
			–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{PD1}	Worst case pin-to-pin delay through 1 look-up table (LUT)	10 pF	—	4.7	—	6.1	—	7.5	—	7.9	—	12.0	—	14.0	ns
t_{PD2}	Best case pin-to-pin delay through 1 LUT	10 pF	—	3.7	—	4.8	—	5.9	—	5.8	—	7.8	—	8.5	ns
t_{SU}	Global clock setup time	—	1.7	—	2.2	—	2.7	—	2.4	—	4.1	—	4.6	—	ns
t_{H}	Global clock hold time	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	4.3	2.0	5.6	2.0	6.9	2.0	6.6	2.0	8.1	2.0	8.6	ns
t_{CH}	Global clock high time	—	166	—	216	—	266	—	253	—	335	—	339	—	ps
t_{CL}	Global clock low time	—	166	—	216	—	266	—	253	—	335	—	339	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	3.3	—	4.0	—	5.0	—	5.4	—	8.1	—	8.4	—	ns

Table 5–23. EPM240 Global Clock External I/O Timing Parameters (Part 2 of 2)

Symbol	Parameter	Condition	MAX II / MAX IIG						MAX IIZ						Unit
			–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	304.0 *(1)*	—	247.5	—	201.1	—	184.1	—	123.5	—	118.3	MHz

Note to Table 5–23:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5–24 shows the external I/O timing parameters for EPM570 devices.

Table 5–24. EPM570 Global Clock External I/O Timing Parameters (Part 1 of 2)

Symbol	Parameter	Condition	MAX II / MAX IIG						MAX IIZ						Unit
			–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through 1 look-up table (LUT)	10 pF	—	5.4	—	7.0	—	8.7	—	9.5	—	15.1	—	17.7	ns
t_{PD2}	Best case pin-to-pin delay through 1 LUT	10 pF	—	3.7	—	4.8	—	5.9	—	5.7	—	7.7	—	8.5	ns
t_{SU}	Global clock setup time	—	1.2	—	1.5	—	1.9	—	2.2	—	3.9	—	4.4	—	ns
t_H	Global clock hold time	—	0	—	0	—	0	—	0	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	4.5	2.0	5.8	2.0	7.1	2.0	6.7	2.0	8.2	2.0	8.7	ns
t_{CH}	Global clock high time	—	166	—	216	—	266	—	253	—	335	—	339	—	ps
t_{CL}	Global clock low time	—	166	—	216	—	266	—	253	—	335	—	339	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	3.3	—	4.0	—	5.0	—	5.4	—	8.1	—	8.4	—	ns

Table 5–31. MAX II IOE Programmable Delays

Parameter	MAX II / MAX IIG						MAX IIZ						Unit
	–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input Delay from Pin to Internal Cells = 1	—	1,225	—	1,592	—	1,960	—	1,858	—	2,171	—	2,214	ps
Input Delay from Pin to Internal Cells = 0	—	89	—	115	—	142	—	569	—	609	—	616	ps

Maximum Input and Output Clock Rates

Table 5–32 and Table 5–33 show the maximum input and output clock rates for standard I/O pins in MAX II devices.

Table 5–32. MAX II Maximum Input Clock Rate for I/O

I/O Standard		MAX II / MAX IIG			MAX IIZ			Unit
		–3 Speed Grade	–4 Speed Grade	–5 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	
3.3-V LVTTL	Without Schmitt Trigger	304	304	304	304	304	304	MHz
	With Schmitt Trigger	250	250	250	250	250	250	MHz
3.3-V LVCMOS	Without Schmitt Trigger	304	304	304	304	304	304	MHz
	With Schmitt Trigger	250	250	250	250	250	250	MHz
2.5-V LVTTL	Without Schmitt Trigger	220	220	220	220	220	220	MHz
	With Schmitt Trigger	188	188	188	188	188	188	MHz
2.5-V LVCMOS	Without Schmitt Trigger	220	220	220	220	220	220	MHz
	With Schmitt Trigger	188	188	188	188	188	188	MHz
1.8-V LVTTL	Without Schmitt Trigger	200	200	200	200	200	200	MHz
1.8-V LVCMOS	Without Schmitt Trigger	200	200	200	200	200	200	MHz
1.5-V LVCMOS	Without Schmitt Trigger	150	150	150	150	150	150	MHz
3.3-V PCI	Without Schmitt Trigger	304	304	304	304	304	304	MHz