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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.4 ns
Voltage Supply - Internal	1.71V ~ 1.89V
Number of Logic Elements/Blocks	570
Number of Macrocells	440
Number of Gates	-
Number of I/O	116
Operating Temperature	0°C ~ 85°C (TJ)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epm570gt144c5

Table 1–6. Document Revision History

Date and Revision	Changes Made	Summary of Changes
June 2005, version 1.3	■ Updated timing numbers in Table 1-1.	—
December 2004, version 1.2	■ Updated timing numbers in Table 1-1.	—
June 2004, version 1.1	■ Updated timing numbers in Table 1-1.	—

Table 2–1. MAX II Device Resources

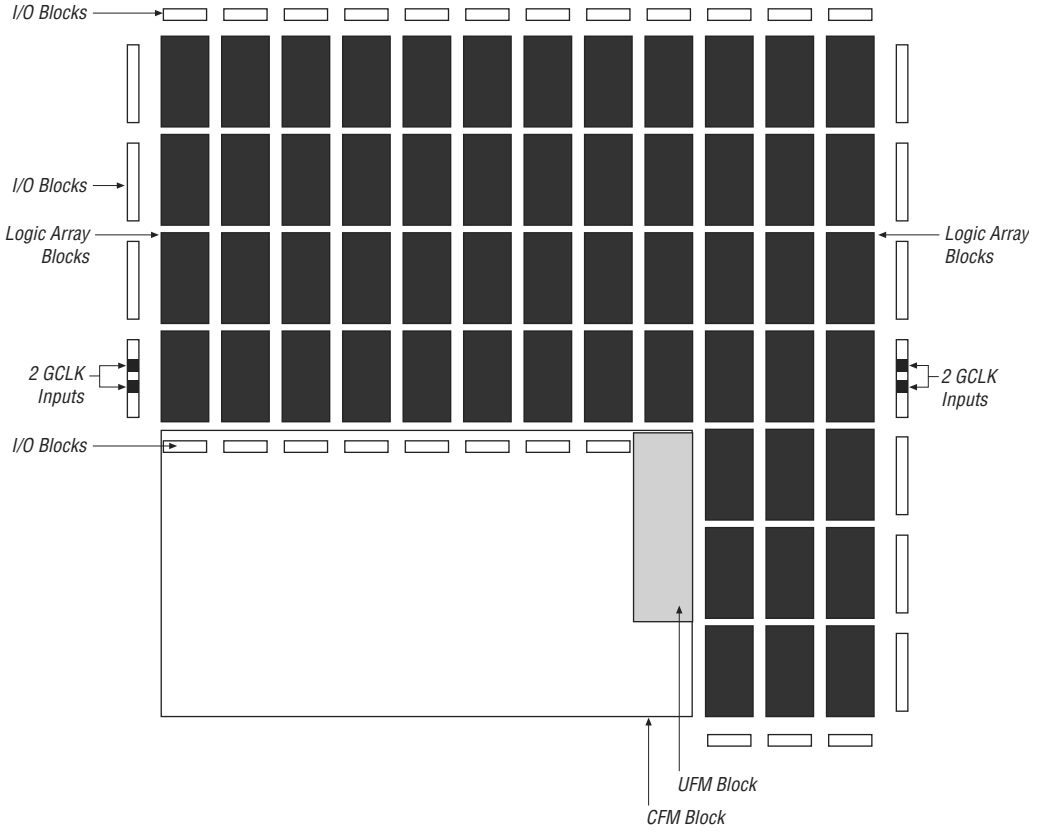
Devices	UFM Blocks	LAB Columns	LAB Rows		Total LABs
			Long LAB Rows	Short LAB Rows (Width) *(1)*	
EPM240	1	6	4	—	24
EPM570	1	12	4	3 (3)	57
EPM1270	1	16	7	3 (5)	127
EPM2210	1	20	10	3 (7)	221

Note to Table 2–1:

(1) The width is the number of LAB columns in length.

Figure 2–2 shows a floorplan of a MAX II device.

Figure 2–2. MAX II Device Floorplan *(Note 1)*



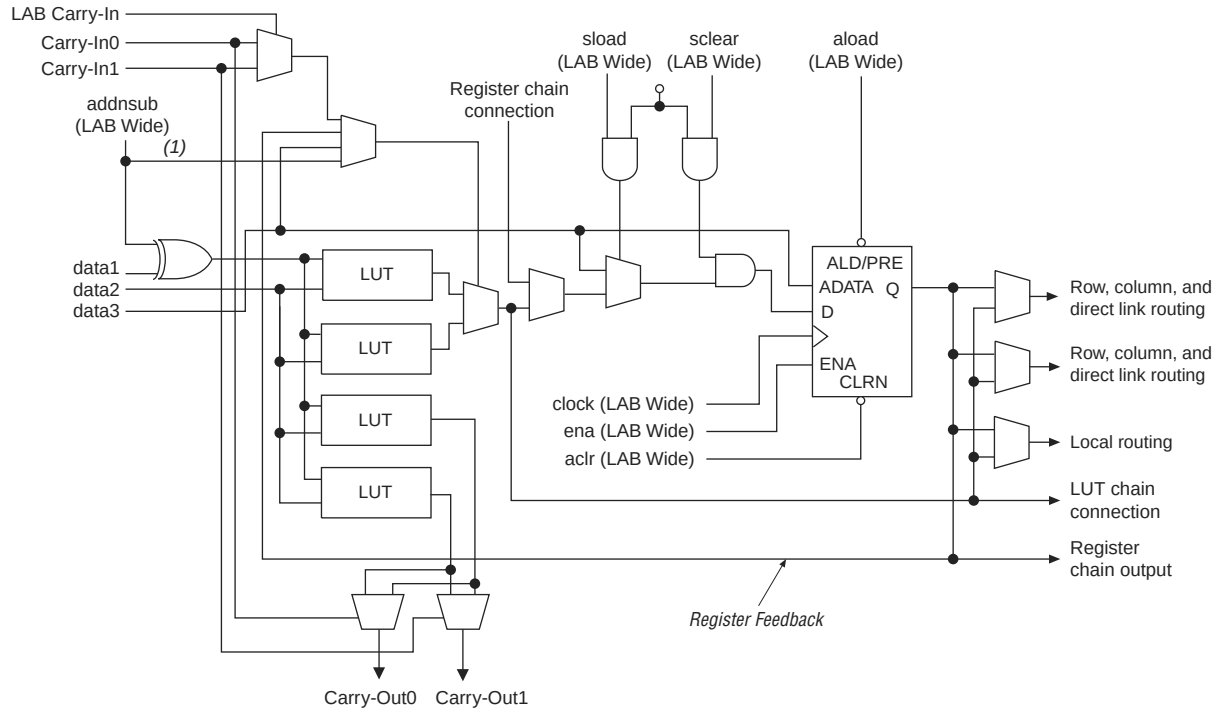
Note to Figure 2–2:

(1) The device shown is an EPM570 device. EPM1270 and EPM2210 devices have a similar floorplan with more LABs. For EPM240 devices, the CFM and UFM blocks are located on the left side of the device.

The other two LUTs use the data1 and data2 signals to generate two possible carry-out signals: one for a carry of 1 and the other for a carry of 0. The `carry-in0` signal acts as the carry-select for the `carry-out0` output and `carry-in1` acts as the carry-select for the `carry-out1` output. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The dynamic arithmetic mode also offers clock enable, counter enable, synchronous up/down control, synchronous clear, synchronous load, and dynamic adder/subtractor options. The LAB local interconnect data inputs generate the counter enable and synchronous up/down control signals. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs. The addnsub LAB-wide signal controls whether the LE acts as an adder or subtractor.

Figure 2–8. LE in Dynamic Arithmetic Mode



Note to Figure 2–8:

(1) The addnsub signal is tied to the carry input for the first LE of a carry chain only.

Carry-Select Chain

The carry-select chain provides a very fast carry-select function between LEs in dynamic arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 0 and carry-in of 1 in parallel. The `carry-in0` and `carry-in1` signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

I/O Structure

IOEs support many features, including:

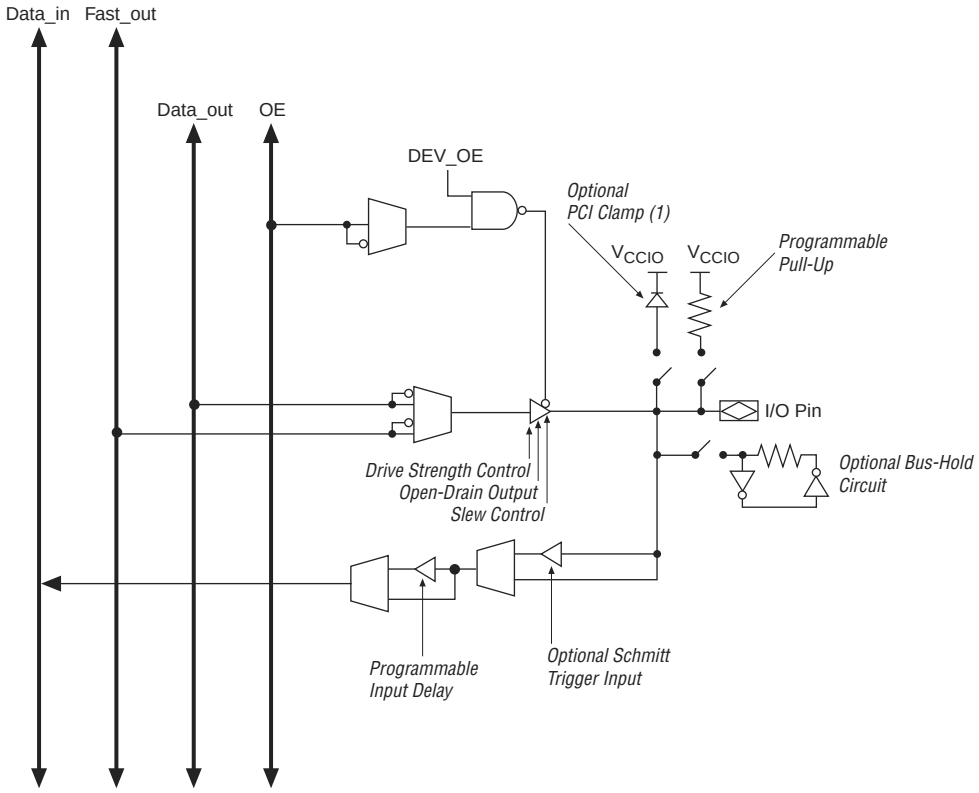
- LVTTL and LVCMOS I/O standards
- 3.3-V, 32-bit, 66-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Programmable drive strength control
- Weak pull-up resistors during power-up and in system programming
- Slew-rate control
- Tri-state buffers with individual output enable control
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Unique output enable per pin
- Open-drain outputs
- Schmitt trigger inputs
- Fast I/O connection
- Programmable input delay

MAX II device IOEs contain a bidirectional I/O buffer. Figure 2–19 shows the MAX II IOE structure. Registers from adjacent LABs can drive to or be driven from the IOE's bidirectional I/O buffers. The Quartus II software automatically attempts to place registers in the adjacent LAB with fast I/O connection to achieve the fastest possible clock-to-output and registered output enable timing. For input registers, the Quartus II software automatically routes the register to guarantee zero hold time. You can set timing assignments in the Quartus II software to achieve desired I/O timing.

Fast I/O Connection

A dedicated fast I/O connection from the adjacent LAB to the IOEs within an I/O block provides faster output delays for clock-to-output and t_{PD} propagation delays. This connection exists for data output signals, not output enable signals or input signals. Figure 2–20, Figure 2–21, and Figure 2–22 illustrate the fast I/O connection.

Figure 2–19. MAX II IOE Structure



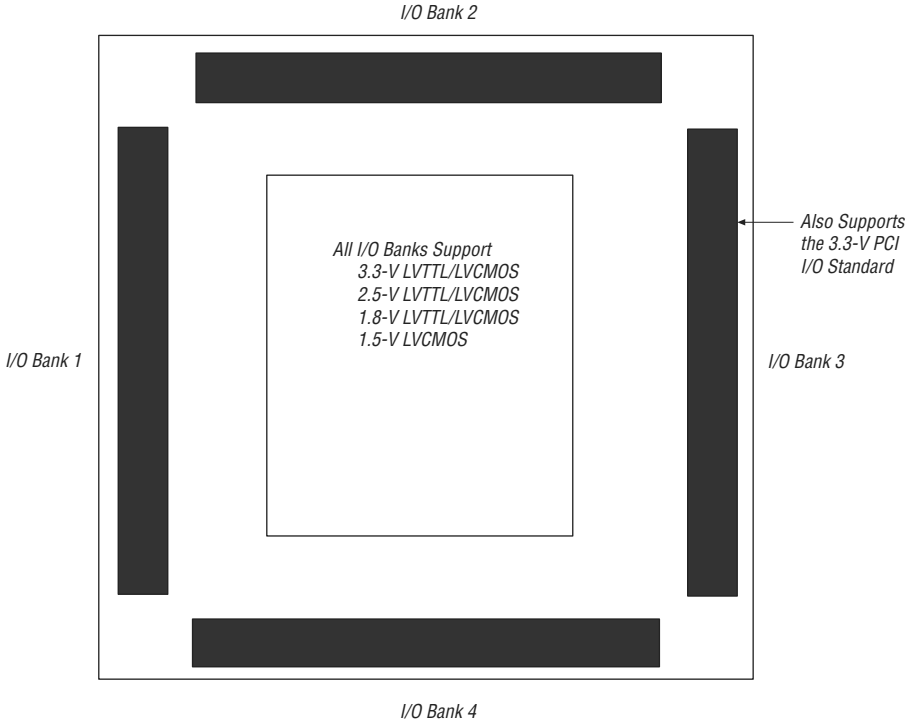
Note to Figure 2–19:

(1) Available in EPM1270 and EPM2210 devices only.

I/O Blocks

The IOEs are located in I/O blocks around the periphery of the MAX II device. There are up to seven IOEs per row I/O block (5 maximum in the EPM240 device) and up to four IOEs per column I/O block. Each column or row I/O block interfaces with its adjacent LAB and MultiTrack interconnect to distribute signals throughout the device. The row I/O blocks drive row, column, or DirectLink interconnects. The column I/O blocks drive column interconnects.

Figure 2–23. MAX II I/O Banks for EPM1270 and EPM2210 *(Note 1), (2)*



Notes to Figure 2–23:

(1) Figure 2–23 is a top view of the silicon die.

(2) Figure 2–23 is a graphical representation only. Refer to the pin list and the Quartus II software for exact pin locations.

Each I/O bank has dedicated V_{CCIO} pins that determine the voltage standard support in that bank. A single device can support 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each individual bank can support a different standard. Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3 V, Bank 3 can support LVTTL, LVCMOS, and 3.3-V PCI. V_{CCIO} powers both the input and output buffers in MAX II devices.

The JTAG pins for MAX II devices are dedicated pins that cannot be used as regular I/O pins. The pins `TMS`, `TDI`, `TDO`, and `TCK` support all the I/O standards shown in Table 2–4 on page 2–27 except for PCI. These pins reside in Bank 1 for all MAX II devices and their I/O standard support is controlled by the V_{CCIO} setting for Bank 1.

PCI Compliance

The MAX II EPM1270 and EPM2210 devices are compliant with PCI applications as well as all 3.3-V electrical specifications in the *PCI Local Bus Specification Revision 2.2*. These devices are also large enough to support PCI intellectual property (IP) cores. Table 2–5 shows the MAX II device speed grades that meet the PCI timing specifications.

Real-Time ISP

For systems that require more than DC logic level control of I/O pins, the real-time ISP feature allows you to update the CFM block with a new design image while the current design continues to operate in the SRAM logic array and I/O pins. A new programming file is updated into the MAX II device without halting the original design's operation, saving down-time costs for remote or field upgrades. The updated CFM block configures the new design into the SRAM upon the next power cycle. It is also possible to execute an immediate configuration of the SRAM without a power cycle by using a specific sequence of ISP commands. The configuration of SRAM without a power cycle takes a specific amount of time (t_{CONFIG}). During this time, the I/O pins are tri-stated and weakly pulled-up to V_{CCIO}.

Design Security

All MAX II devices contain a programmable security bit that controls access to the data programmed into the CFM block. When this bit is programmed, design programming information, stored in the CFM block, cannot be copied or retrieved. This feature provides a high level of design security because programmed data within flash memory cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is erased. The SRAM is also invisible and cannot be accessed regardless of the security bit setting. The UFM block data is not protected by the security bit and is accessible through JTAG or logic array connections.

Programming with External Hardware

MAX II devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera® ByteblasterMV™, MasterBlaster™, ByteBlaster™ II, and USB-Blaster cables.

BP Microsystems, System General, and other programming hardware manufacturers provide programming support for Altera devices. Check their websites for device support information.

Referenced Documents

This chapter references the following documents:

- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *IEEE 1149.1 (JTAG) Boundary-Scan Testing for MAX II Devices* chapter in the *MAX II Device Handbook*
- *Real-Time ISP and ISP Clamp for MAX II Devices* chapter in the *MAX II Device Handbook*
- *Using Jam STAPL for ISP via an Embedded Processor* chapter in the *MAX II Device Handbook*

Referenced Documents

This chapter refereces the following documents:

- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *Using MAX II Devices in Multi-Voltage Systems* chapter in the *MAX II Device Handbook*

Document Revision History

Table 4–1 shows the revision history for this chapter.

Table 4–1. Document Revision History

Date and Revision	Changes Made	Summary of Changes
October 2008, version2.1	■ Updated "MAX II Hot-Socketing Specifications" and "Power-On Reset Circuitry" sections. ■ Updated New Document Format.	—
December 2007, version 2.0	■ Updated "Hot Socketing Feature Implementation in MAX II Devices" section. ■ Updated "Power-On Reset Circuitry" section. ■ Updated Figure 4–5. ■ Added "Referenced Documents" section.	Updated document with MAX IIZ information.
December 2006, version 1.5	■ Added document revision history.	—
February 2006, version 1.4	■ Updated "MAX II Hot-Socketing Specifications" section. ■ Updated "AC and DC Specifications" section. ■ Updated "Power-On Reset Circuitry" section.	—
June 2005, version 1.3	■ Updated AC and DC specifications on page 4-2.	—
December 2004, version 1.2	■ Added content to Power-Up Characteristics section. ■ Updated Figure 4-5.	—
June 2004, version 1.1	■ Corrected Figure 4-2.	—

5. DC and Switching Characteristics

MII51005-2.5

Introduction

System designers must consider the recommended DC and switching conditions discussed in this chapter to maintain the highest possible performance and reliability of the MAX® II devices. This chapter contains the following sections:

Operating Conditions

Table 5–1 through Table 5–12 provide information about absolute maximum ratings, recommended operating conditions, DC electrical characteristics, and other specifications for MAX II devices.

Absolute Maximum Ratings

Table 5–1 shows the absolute maximum ratings for the MAX II device family.

Table 5–1. MAX II Device Absolute Maximum Ratings *(Note 1)*, *(2)*

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT}	Internal supply voltage *(3)*	With respect to ground	–0.5	4.6	V
V_{CCIO}	I/O supply voltage	—	–0.5	4.6	V
V_I	DC input voltage	—	–0.5	4.6	V
I_{OUT}	DC output current, per pin *(4)*	—	–25	25	mA
T_{STG}	Storage temperature	No bias	–65	150	°C
T_{AMB}	Ambient temperature	Under bias *(5)*	–65	135	°C
T_J	Junction temperature	TQFP and BGA packages under bias	—	135	°C

Notes to Table 5–1:

(1) Refer to the *Operating Requirements for Altera Devices Data Sheet*.

(2) Conditions beyond those listed in Table 5–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.

(3) Maximum V_{CCINT} for MAX II devices is 4.6 V. For MAX IIG and MAX IIZ devices, it is 2.4 V.

(4) Refer to *AN 286: Implementing LED Drivers in MAX & MAX II Devices* for more information about the maximum source and sink current for MAX II devices.

(5) Refer to Table 5–2 for information about "under bias" conditions.

Recommended Operating Conditions

Table 5–2 shows the MAX II device family recommended operating conditions.

Table 5–2. MAX II Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCINT} *(1)*	3.3-V supply voltage for internal logic and ISP	MAX II devices	3.00	3.60	V
	2.5-V supply voltage for internal logic and ISP	MAX II devices	2.375	2.625	V
	1.8-V supply voltage for internal logic and ISP	MAX IIG and MAX IIZ devices	1.71	1.89	V
V_{CCIO} *(1)*	Supply voltage for I/O buffers, 3.3-V operation	—	3.00	3.60	V
	Supply voltage for I/O buffers, 2.5-V operation	—	2.375	2.625	V
	Supply voltage for I/O buffers, 1.8-V operation	—	1.71	1.89	V
	Supply voltage for I/O buffers, 1.5-V operation	—	1.425	1.575	V
V_I	Input voltage	*(2)*, *(3)*, *(4)*	–0.5	4.0	V
V_O	Output voltage	—	0	V_{CCIO}	V
T_J	Operating junction temperature	Commercial range	0	85	°C
		Industrial range	–40	100	°C
		Extended range *(5)*	–40	125	°C

Notes to Table 5–2:

(1) MAX II device in-system programming and/or user flash memory (UFM) programming via JTAG or logic array is not guaranteed outside the recommended operating conditions (for example, if brown-out occurs in the system during a potential write/program sequence to the UFM, users are recommended to read back UFM contents and verify against the intended write data).

(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

(3) During transitions, the inputs may overshoot to the voltages shown in the following table based upon input duty cycle. The DC case is equivalent to 100% duty cycle. For more information about 5.0-V tolerance, refer to the *Using MAX II Devices in Multi-Voltage Systems* chapter in the *MAX II Device Handbook*.

V_{IN}	Max. Duty Cycle
4.0 V	100% (DC)
4.1	90%
4.2	50%
4.3	30%
4.4	17%
4.5	10%

(4) All pins, including clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(5) For the extended temperature range of 100 to 125° C, MAX II UFM programming (erase/write) is only supported via the JTAG interface. UFM programming via the logic array interface is not guaranteed in this range.

Programming/Erasure Specifications

Table 5–3 shows the MAX II device family programming/erasure specifications.

Table 5–3. MAX II Device Programming/Erasure Specifications

Parameter	Minimum	Typical	Maximum	Unit
Erase and reprogram cycles	—	—	100 *(1)*	Cycles

Note to Table 5–3:

(1) This specification applies to the UFM and configuration flash memory (CFM) blocks.

DC Electrical Characteristics

Table 5–4 shows the MAX II device family DC electrical characteristics.

Table 5–4. MAX II Device DC Electrical Characteristics *(Note 1)* (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIO}$ max to 0 V *(2)*	–10	—	10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIO}$ max to 0 V *(2)*	–10	—	10	µA
$I_{CCSTANDBY}$	V_{CCINT} supply current (standby) *(3)*	MAX II devices	—	12	—	mA
		MAX IIG devices	—	2	—	mA
		EPM240Z (Commercial grade) *(4)*	—	25	90	µA
		EPM240Z (Industrial grade) *(5)*	—	25	139	µA
		EPM570Z (Commercial grade) *(4)*	—	27	96	µA
		EPM570Z (Industrial grade) *(5)*	—	27	152	µA
$V_{SCHMITT}$ *(6)*	Hysteresis for Schmitt trigger input *(7)*	V_{CCIO} = 3.3 V	—	400	—	mV
		V_{CCIO} = 2.5 V	—	190	—	mV
$I_{CCPOWERUP}$	V_{CCINT} supply current during power-up *(8)*	MAX II devices	—	55	—	mA
		MAX IIG and MAX IIZ devices	—	40	—	mA
R_{PULLUP}	Value of I/O pin pull-up resistor during user mode and in-system programming	V_{CCIO} = 3.3 V *(9)*	5	—	25	kΩ
		V_{CCIO} = 2.5 V *(9)*	10	—	40	kΩ
		V_{CCIO} = 1.8 V *(9)*	25	—	60	kΩ
		V_{CCIO} = 1.5 V *(9)*	45	—	95	kΩ

Table 5–4. MAX II Device DC Electrical Characteristics *(Note 1)* (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{PULLUP}	I/O pin pull-up resistor current when I/O is unprogrammed	—	—	—	300	µA
C_{IO}	Input capacitance for user I/O pin	—	—	—	8	pF
C_{GCLK}	Input capacitance for dual-purpose GCLK/user I/O pin	—	—	—	8	pF

Notes to Table 5–4:

(1) Typical values are for T_A = 25°C, V_{CCINT} = 3.3 or 2.5 V, and V_{CCIO} = 1.5 V, 1.8 V, 2.5 V, or 3.3 V.

(2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).

(3) V_I = ground, no load, no toggling inputs.

(4) Commercial temperature ranges from 0°C to 85°C with maximum current at 85°C.

(5) Industrial temperature ranges from –40°C to 100°C with maximum current at 100°C.

(6) This value applies to commercial and industrial range devices. For extended temperature range devices, the $V_{SCHMITT}$ typical value is 300 mV for V_{CCIO} = 3.3 V and 120 mV for V_{CCIO} = 2.5 V.

(7) The TCK input is susceptible to high pulse glitches when the input signal fall time is greater than 200 ns for all I/O standards.

(8) This is a peak current value with a maximum duration of t_{CONFIG} time.

(9) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.

Table 5–6. 3.3-V LVCMOS Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{OH}	High-level output voltage	V_{CCIO} = 3.0, IOH = –0.1 mA *(1)*	V_{CCIO} – 0.2	—	V
V_{OL}	Low-level output voltage	V_{CCIO} = 3.0, IOL = 0.1 mA *(1)*	—	0.2	V

Table 5–7. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	2.375	2.625	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.5	0.7	V
V_{OH}	High-level output voltage	IOH = –0.1 mA *(1)*	2.1	—	V
		IOH = –1 mA *(1)*	2.0	—	V
		IOH = –2 mA *(1)*	1.7	—	V
V_{OL}	Low-level output voltage	IOL = 0.1 mA *(1)*	—	0.2	V
		IOL = 1 mA *(1)*	—	0.4	V
		IOL = 2 mA *(1)*	—	0.7	V

Table 5–8. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	1.71	1.89	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	2.25 *(2)*	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	IOH = –2 mA *(1)*	V_{CCIO} – 0.45	—	V
V_{OL}	Low-level output voltage	IOL = 2 mA *(1)*	—	0.45	V

Table 5–9. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	1.425	1.575	V
V_{IH}	High-level input voltage	—	0.65 × V_{CCIO}	V_{CCIO} + 0.3 *(2)*	V
V_{IL}	Low-level input voltage	—	–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	IOH = –2 mA *(1)*	0.75 × V_{CCIO}	—	V
V_{OL}	Low-level output voltage	IOL = 2 mA *(1)*	—	0.25 × V_{CCIO}	V

Notes to Table 5–5 through Table 5–9:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the *MAX II Architecture* chapter (*I/O Structure section*) in the *MAX II Device Handbook*.

(2) This maximum V_{IH} reflects the JEDEC specification. The MAX II input buffer can tolerate a V_{IH} maximum of 4.0, as specified by the V_I parameter in Table 5–2.

Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Table 5–15 through Table 5–22 describe the MAX II device internal timing microparameters for logic elements (LEs), input/output elements (IOEs), UFM blocks, and MultiTrack interconnects. The timing values for –3, –4, and –5 speed grades shown in Table 5–15 through Table 5–22 are based on an EPM1270 device target, while –6, –7, and –8 speed grade values are based on an EPM570Z device target.

For more explanations and descriptions about each internal timing microparameters symbol, refer to the *Understanding Timing in MAX II Devices* chapter in the *MAX II Device Handbook*.

Table 5–15. LE Internal Timing Microparameters

		MAX II / MAX IIG						MAX IIZ						
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{LUT}	LE combinational LUT delay	—	571	—	742	—	914	—	1,215	—	2,247	—	2,247	ps
t_{COMB}	Combinational path delay	—	147	—	192	—	236	—	243	—	305	—	309	ps
t_{CLR}	LE register clear delay	238	—	309	—	381	—	401	—	541	—	545	—	ps
t_{PRE}	LE register preset delay	238	—	309	—	381	—	401	—	541	—	545	—	ps
t_{SU}	LE register setup time before clock	208	—	271	—	333	—	260	—	319	—	321	—	ps
t_{H}	LE register hold time after clock	0	—	0	—	0	—	0	—	0	—	0	—	ps
t_{CO}	LE register clock-to-output delay	—	235	—	305	—	376	—	380	—	489	—	494	ps
t_{CLKHL}	Minimum clock high or low time	166	—	216	—	266	—	253	—	335	—	339	—	ps
t_{C}	Register control delay	—	857	—	1,114	—	1,372	—	1,356	—	1,722	—	1,741	ps

Table 5–17. t_{ZX} IOE Microparameter Adders for Fast Slew Rate (Part 2 of 2)

Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
1.5-V LVCMOS	4 mA	—	1,118	—	1,454	—	1,789	—	580	—	588	—	588	ps
	2 mA	—	2,410	—	3,133	—	3,856	—	915	—	923	—	923	ps
3.3-V PCI	20 mA	—	19	—	25	—	31	—	72	—	71	—	74	ps

Table 5–18. t_{ZX} IOE Microparameter Adders for Slow Slew Rate

Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	6,350	—	6,050	—	5,749	—	5,951	—	5,952	—	6,063	ps
	8 mA	—	9,383	—	9,083	—	8,782	—	6,534	—	6,533	—	6,662	ps
3.3-V LVCMOS	8 mA	—	6,350	—	6,050	—	5,749	—	5,951	—	5,952	—	6,063	ps
	4 mA	—	9,383	—	9,083	—	8,782	—	6,534	—	6,533	—	6,662	ps
2.5-V LVTTL / LVCMOS	14 mA	—	10,412	—	10,112	—	9,811	—	9,110	—	9,105	—	9,237	ps
	7 mA	—	13,613	—	13,313	—	13,012	—	9,830	—	9,835	—	9,977	ps
3.3-V PCI	20 mA	—	–75	—	–97	—	–120	—	6,534	—	6,533	—	6,662	ps

Table 5–19. t_{XZ} IOE Microparameter Adders for Fast Slew Rate

Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	8 mA	—	–56	—	–72	—	–89	—	–69	—	–69	—	–69	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	4 mA	—	–56	—	–72	—	–89	—	–69	—	–69	—	–69	ps
2.5-V LVTTL / LVCMOS	14 mA	—	–3	—	–4	—	–5	—	–7	—	–11	—	–11	ps
	7 mA	—	–47	—	–61	—	–75	—	–66	—	–70	—	–70	ps
1.8-V LVTTL / LVCMOS	6 mA	—	119	—	155	—	191	—	45	—	34	—	37	ps
	3 mA	—	207	—	269	—	331	—	34	—	22	—	25	ps
1.5-V LVCMOS	4 mA	—	606	—	788	—	970	—	166	—	154	—	155	ps
	2 mA	—	673	—	875	—	1,077	—	190	—	177	—	179	ps
3.3-V PCI	20 mA	—	71	—	93	—	114	—	–69	—	–69	—	–69	ps

Table 5–26 shows the external I/O timing parameters for EPM2210 devices.

Table 5–26. EPM2210 Global Clock External I/O Timing Parameters

Symbol	Parameter	Condition	MAX II / MAX IIG						Unit
			–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through 1 look-up table (LUT)	10 pF	—	7.0	—	9.1	—	11.2	ns
t_{PD2}	Best case pin-to-pin delay through 1 LUT	10 pF	—	3.7	—	4.8	—	5.9	ns
t_{SU}	Global clock setup time	—	1.2	—	1.5	—	1.9	—	ns
t_{H}	Global clock hold time	—	0	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	4.6	2.0	6.0	2.0	7.4	ns
t_{CH}	Global clock high time	—	166	—	216	—	266	—	ps
t_{CL}	Global clock low time	—	166	—	216	—	266	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	3.3	—	4.0	—	5.0	—	ns
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	304.0 *(1)*	—	247.5	—	201.1	MHz

Note to Table 5–26:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

External Timing I/O Delay Adders

The I/O delay timing parameters for I/O standard input and output adders, and input delays are specified by speed grade independent of device density.

Table 5–27 through Table 5–31 show the adder delays associated with I/O pins for all packages. The delay numbers for –3, –4, and –5 speed grades shown in Table 5–27 through Table 5–33 are based on an EPM1270 device target, while –6, –7, and –8 speed grade values are based on an EPM570Z device target. If an I/O standard other than 3.3-V LVTTL is selected, add the input delay adder to the external t_{SU} timing parameters shown in Table 5–23 through Table 5–26. If an I/O standard other than 3.3-V LVTTL with 16 mA drive strength and fast slew rate is selected, add the output delay adder to the external t_{CO} and t_{PD} shown in Table 5–23 through Table 5–26.

Table 5–27. External Timing Input Delay Adders (Part 1 of 2)

I/O Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	334	—	434	—	535	—	387	—	434	—	442	ps

Table 5–33. MAX II Maximum Output Clock Rate for I/O

I/O Standard		MAX II / MAX IIG			MAX IIZ		
		–3 Speed Grade	–4 Speed Grade	–5 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade
3.3-V LVTTL	304	304	304	304	304	304	MHz
3.3-V LVCMOS	304	304	304	304	304	304	MHz
2.5-V LVTTL	220	220	220	220	220	220	MHz
2.5-V LVCMOS	220	220	220	220	220	220	MHz
1.8-V LVTTL	200	200	200	200	200	200	MHz
1.8-V LVCMOS	200	200	200	200	200	200	MHz
1.5-V LVCMOS	150	150	150	150	150	150	MHz
3.3-V PCI	304	304	304	304	304	304	MHz

JTAG Timing Specifications

Figure 5–6 shows the timing waveforms for the JTAG signals.

Figure 5–6. MAX II JTAG Timing Waveforms

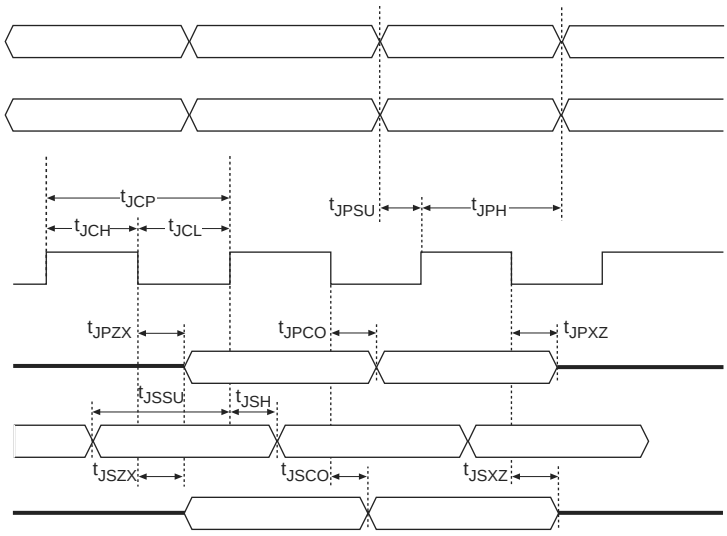


Table 5–34 shows the JTAG Timing parameters and values for MAX II devices.

Table 5–34. MAX II JTAG Timing Parameters (Part 1 of 2)

Symbol	Parameter	Min	Max	Unit
t_{JCP} *(1)*	TCK clock period for V_{CCIO1} = 3.3 V	55.5	—	ns
	TCK clock period for V_{CCIO1} = 2.5 V	62.5	—	ns
	TCK clock period for V_{CCIO1} = 1.8 V	100	—	ns
	TCK clock period for V_{CCIO1} = 1.5 V	143	—	ns
t_{JCH}	TCK clock high time	20	—	ns
t_{JCL}	TCK clock low time	20	—	ns

Table 5–34. MAX II JTAG Timing Parameters (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{JPSU}	JTAG port setup time *(2)*	8	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output *(2)*	—	15	ns
t_{JPZX}	JTAG port high impedance to valid output *(2)*	—	15	ns
t_{JPXZ}	JTAG port valid output to high impedance *(2)*	—	15	ns
t_{JSSU}	Capture register setup time	8	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Notes to Table 5–34:

(1) Minimum clock period specified for 10 pF load on the TDO pin. Larger loads on TDO will degrade the maximum TCK frequency.

(2) This specification is shown for 3.3-V LVTTL/LVCMOS and 2.5-V LVTTL/LVCMOS operation of the JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the t_{JPSU} minimum is 6 ns and t_{JPCO}, t_{JPZX}, and t_{JPXZ} are maximum values at 35 ns.

Referenced Documents

This chapter references the following documents:

- *I/O Structure* section in the *MAX II Architecture* chapter in the *MAX II Device Handbook*
- *Hot Socketing and Power-On Reset in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Operating Requirements for Altera Devices Data Sheet*
- *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*
- *Understanding and Evaluating Power in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Understanding Timing in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Using MAX II Devices in Multi-Voltage Systems* chapter in the *MAX II Device Handbook*