Intel - EPM570M100C5N Datasheet





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Understanding <u>Embedded - CPLDs (Complex</u> <u>Programmable Logic Devices)</u>

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixedfunction ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.4 ns
Voltage Supply - Internal	2.5V, 3.3V
Number of Logic Elements/Blocks	570
Number of Macrocells	440
Number of Gates	-
Number of I/O	76
Operating Temperature	0°C ~ 85°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-MBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm570m100c5n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Figure 2-4. DirectLink Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, a synchronous clear, an asynchronous preset/load, a synchronous load, and add/subtract control signals, providing a maximum of 10 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the labclk1 signal also uses labclkena1. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. Deasserting the clock enable signal turns off the LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. By default, the Quartus II software uses a NOT gate push-back technique to achieve preset. If you disable the NOT gate push-back option or assign a given register to power-up high using the Quartus II software, the preset is then achieved using the asynchronous load signal with asynchronous load data input tied high.

With the LAB-wide addnsub control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB column clocks [3..0], driven by the global clock network, and LAB local interconnect generate the LAB-wide control signals. The MultiTrack interconnect structure drives the LAB local interconnect for non-global control signal generation. The MultiTrack interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 2–5 shows the LAB control signal generation circuit.

LUT Chain and Register Chain

In addition to the three general routing outputs, the LEs within an LAB have LUT chain and register chain outputs. LUT chain connections allow LUTs within the same LAB to cascade together for wide input functions. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows an LAB to use LUTs for a single combinational function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. Refer to "MultiTrack Interconnect" on page 2–12 for more information about LUT chain and register chain connections.

addnsub Signal

The LE's dynamic adder/subtractor feature saves logic resources by using one set of LEs to implement both an adder and a subtractor. This feature is controlled by the LAB-wide control signal addnsub. The addnsub signal sets the LAB to perform either A + B or A - B. The LUT computes addition; subtraction is computed by adding the two's complement of the intended subtractor. The LAB-wide signal converts to two's complement by inverting the B bits within the LAB and setting carry-in to 1, which adds one to the least significant bit (LSB). The LSB of an adder/subtractor must be placed in the first LE of the LAB, where the LAB-wide addnsub signal automatically sets the carry-in to 1. The Quartus II Compiler automatically places and uses the adder/subtractor feature when using adder/subtractor parameterized functions.

LE Operating Modes

The MAX II LE can operate in one of the following modes:

- "Normal Mode"
- "Dynamic Arithmetic Mode"

Each mode uses LE resources differently. In each mode, eight available inputs to the LE, the four data inputs from the LAB local interconnect, carry-in0 and carry-in1 from the previous LE, the LAB carry-in from the previous carry-chain LAB, and the register chain connection are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset/load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes. The addnsub control signal is allowed in arithmetic mode.

The Quartus II software, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions.

Normal Mode

The normal mode is suitable for general logic applications and combinational functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (see Figure 2–7). The Quartus II Compiler automatically selects the carry-in or the data3 signal as one of the inputs to the LUT. Each LE can use LUT chain connections to drive its combinational output directly to the next LE in the LAB. Asynchronous load data for the register comes from the data3 input of the LE. LEs in normal mode support packed registers.





Note to Figure 2-7:

(1) This signal is only allowed in normal mode if the LE is at the end of an adder/subtractor chain.

Dynamic Arithmetic Mode

The dynamic arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An LE in dynamic arithmetic mode uses four 2-input LUTs configurable as a dynamic adder/subtractor. The first two 2-input LUTs compute two summations based on a possible carry-in of 1 or 0; the other two LUTs generate carry outputs for the two chains of the carry-select circuitry. As shown in Figure 2–8, the LAB carry-in signal selects either the carry-in0 or carry-in1 chain. The selected chain's logic level in turn determines which parallel sum is generated as a combinational or registered output. For example, when implementing an adder, the sum output is the selection of two possible calculated sums:

```
data1 + data2 + carry in0
or
data1 + data2 + carry-in1
```

The speed advantage of the carry-select chain is in the parallel precomputation of carry chains. Since the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delays between LAB carry-in generation (LE 5 and LE 10) are now part of the critical path. This feature allows the MAX II architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

Figure 2–9 shows the carry-select circuitry in an LAB for a 10-bit full adder. One portion of the LUT generates the sum of two bits using the input signals and the appropriate carry-in bit; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT generates carry-out bits. An LAB-wide carry-in bit selects which chain is used for the addition of given inputs. The carry-in signal for each chain, carry-in0 or carry-in1, selects the carry-out to carry forward to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is fed to local, row, or column interconnects.





The Quartus II software automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions. The Quartus II software creates carry chains longer than 10 LEs by linking adjacent LABs within the same row together automatically. A carry chain can extend horizontally up to one full LAB row, but does not extend between LAB rows.

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. MAX II devices support simultaneous preset/asynchronous load and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, MAX II devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals and uses its own dedicated routing resources (that is, it does not use any of the four global resources). Driving this signal low before or during power-up prevents user mode from releasing clears within the design. This allows you to control when clear is released on a device that has just been powered-up. If not set for its chip-wide reset function, the DEV_CLRn pin is a regular I/O pin.

By default, all registers in MAX II devices are set to power-up low. However, this power-up state can be set to high on individual registers during design entry using the Quartus II software.

MultiTrack Interconnect

In the MAX II architecture, connections between LEs, the UFM, and device I/O pins are provided by the MultiTrack interconnect structure. The MultiTrack interconnect consists of continuous, performance-optimized routing lines used for inter- and intradesign block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and short delays between logic levels instead of large delays associated with global or long routing lines. Dedicated row interconnects route signals to and from LABs within the same row. These row resources include:

- DirectLink interconnects between LABs
- R4 interconnects traversing four LABs to the right or left

The DirectLink interconnect allows an LAB to drive into the local interconnect of its left and right neighbors. The DirectLink interconnect provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.



Figure 2–14. Global Clock Network (Note 1)

Notes to Figure 2–14:

(1) LAB column clocks in I/O block regions provide high fan-out output enable signals.

(2) LAB column clocks drive to the UFM block.

User Flash Memory Block

MAX II devices feature a single UFM block, which can be used like a serial EEPROM for storing non-volatile information up to 8,192 bits. The UFM block connects to the logic array through the MultiTrack interconnect, allowing any LE to interface to the UFM block. Figure 2–15 shows the UFM block and interface signals. The logic array is used to create customer interface or protocol logic to interface the UFM block data outside of the device. The UFM block offers the following features:

- Non-volatile storage up to 16-bit wide and 8,192 total bits
- Two sectors for partitioned sector erase
- Built-in internal oscillator that optionally drives logic array
- Program, erase, and busy signals

- Auto-increment addressing
- Serial interface to logic array with programmable interface





UFM Storage

Each device stores up to 8,192 bits of data in the UFM block. Table 2–3 shows the data size, sector, and address sizes for the UFM block.

 Table 2–3.
 UFM Array Size

Device	Total Bits	Sectors	Address Bits	Data Width
EPM240	8,192	2	9	16
EPM570		(4,096 bits/sector)		
EPM1270				
EPM2210				

There are 512 locations with 9-bit addressing ranging from 000h to 1FFh. Sector 0 address space is 000h to 0FFh and Sector 1 address space is from 100h to 1FFh. The data width is up to 16 bits of data. The Quartus II software automatically creates logic to accommodate smaller read or program data widths. Erasure of the UFM involves individual sector erasing (that is, one erase of sector 0 and one erase of sector 1 is required to erase the entire UFM block). Since sector erase is required before a program or write, having two sectors enables a sector size of data to be left untouched while the other sector is erased and programmed with new data.

Figure 2–16. EPM240 UFM Block LAB Row Interface (Note 1)



Note to Figure 2–16:

(1) The UFM block inputs and outputs can drive to/from all types of interconnects, not only DirectLink interconnects from adjacent row LABs.





MultiVolt Core

The MAX II architecture supports the MultiVolt core feature, which allows MAX II devices to support multiple V_{CC} levels on the V_{CCINT} supply. An internal linear voltage regulator provides the necessary 1.8-V internal voltage supply to the device. The voltage regulator supports 3.3-V or 2.5-V supplies on its inputs to supply the 1.8-V internal voltage to the device, as shown in Figure 2–18. The voltage regulator is not guaranteed for voltages that are between the maximum recommended 2.5-V operating voltage and the minimum recommended 3.3-V operating voltage.

The MAX IIG and MAX IIZ devices use external 1.8-V supply. The 1.8-V V_{cc} external supply powers the device core directly.





Device	33-MHz PCI	66-MHz PCI
EPM1270	All Speed Grades	–3 Speed Grade
EPM2210	All Speed Grades	–3 Speed Grade

Table 2–5.	MAX II Devices	and Speed Grad	es that Support	3.3-V PCI Elect	rical Specifications and
Meet PCI Ti	ming				

Schmitt Trigger

The input buffer for each MAX II device I/O pin has an optional Schmitt trigger setting for the 3.3-V and 2.5-V standards. The Schmitt trigger allows input buffers to respond to slow input edge rates with a fast output edge rate. Most importantly, Schmitt triggers provide hysteresis on the input buffer, preventing slow-rising noisy input signals from ringing or oscillating on the input signal driven into the logic array. This provides system noise tolerance on MAX II inputs, but adds a small, nominal input delay.

The JTAG input pins (TMS, TCK, and TDI) have Schmitt trigger buffers that are always enabled.

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The TCK input is susceptible to high pulse glitches when the input signal fall time is greater than 200 ns for all I/O standards.

Output Enable Signals

Each MAX II IOE output buffer supports output enable signals for tri-state control. The output enable signal can originate from the GCLK[3..0] global signals or from the MultiTrack interconnect. The MultiTrack interconnect routes output enable signals and allows for a unique output enable for each output or bidirectional pin.

MAX II devices also provide a chip-wide output enable pin (DEV_OE) to control the output enable for every output pin in the design. An option set before compilation in the Quartus II software controls this pin. This chip-wide output enable uses its own routing resources and does not use any of the four global resources. If this option is turned on, all outputs on the chip operate normally when DEV_OE is asserted. When the pin is deasserted, all outputs are tri-stated. If this option is turned off, the DEV_OE pin is disabled when the device operates in user mode and is available as a user I/O pin.

Programmable Drive Strength

The output buffer for each MAX II device I/O pin has two levels of programmable drive strength control for each of the LVTTL and LVCMOS I/O standards. Programmable drive strength provides system noise reduction control for high performance I/O designs. Although a separate slew-rate control feature exists, using the lower drive strength setting provides signal slew-rate control to reduce system noise and signal overshoot without the large delay adder associated with the slew-rate control feature. Table 2–6 shows the possible settings for the I/O standards with drive strength control. The Quartus II software uses the maximum current strength as the default setting. The PCI I/O standard is always set at 20 mA with no alternate setting.

		Binary IDCODE (32 Bits) <i>(1)</i>											
Device	Version (4 Bits)	Part Number	Manufacturer Identity (11 Bits)	LSB (1 Bit) <i>(2)</i>	HEX IDCODE								
EPM240Z	0000	0010 0000 1010 0101	000 0110 1110	1	0x020A50DD								
EPM570Z	0000	0010 0000 1010 0110	000 0110 1110	1	0x020A60DD								

Table 3-3. 32-Bit MAX II Device IDCODE (Part 2 of 2)

Notes to Table 3-2:

(1) The most significant bit (MSB) is on the left.

(2) The IDCODE's least significant bit (LSB) is always 1.

JTAG Block

The MAX II JTAG block feature allows you to access the JTAG TAP and state signals when either the USER0 or USER1 instruction is issued to the JTAG TAP. The USER0 and USER1 instructions bring the JTAG boundary-scan chain (TDI) through the user logic instead of the MAX II device's boundary-scan cells. Each USER instruction allows for one unique user-defined JTAG chain into the logic array.

Parallel Flash Loader

The JTAG block ability to interface JTAG to non-JTAG devices is ideal for generalpurpose flash memory devices (such as Intel- or Fujitsu-based devices) that require programming during in-circuit test. The flash memory devices can be used for FPGA configuration or be part of system memory. In many cases, the MAX II device is already connected to these devices as the configuration control logic between the FPGA and the flash device. Unlike ISP-capable CPLD devices, bulk flash devices do not have JTAG TAP pins or connections. For small flash devices, it is common to use the serial JTAG scan chain of a connected device to program the non-JTAG flash device. This is slow and inefficient in most cases and impractical for large parallel flash devices. Using the MAX II device's JTAG block as a parallel flash loader, with the Quartus II software, to program and verify flash contents provides a fast and costeffective means of in-circuit programming during test. Figure 3–1 shows MAX II being used as a parallel flash loader.

[•] For JTAG AC characteristics, refer to the *DC* and *Switching Characteristics* chapter in the *MAX II Device Handbook*.

For more information about JTAG BST, refer to the *IEEE 1149.1 (JTAG) Boundary-Scan Testing for MAX II Devices* chapter in the *MAX II Device Handbook*.

Figure 3–1. MAX II Parallel Flash Loader



Notes to Figure 3-1:

(1) This block is implemented in LEs.

(2) This function is supported in the Quartus II software.

In System Programmability

MAX II devices can be programmed in-system via the industry standard 4-pin IEEE Std. 1149.1 (JTAG) interface. In-system programmability (ISP) offers quick, efficient iterations during design development and debugging cycles. The logic, circuitry, and interconnects in the MAX II architecture are configured with flash-based SRAM configuration elements. These SRAM elements require configuration data to be loaded each time the device is powered. The process of loading the SRAM data is called configuration. The on-chip configuration flash memory (CFM) block stores the SRAM element's configuration data. The CFM block stores the design's configuration pattern in a reprogrammable flash array. During ISP, the MAX II JTAG and ISP circuitry programs the design pattern into the CFM block's non-volatile flash array.

The MAX II JTAG and ISP controller internally generate the high programming voltages required to program the CFM cells, allowing in-system programming with any of the recommended operating external voltage supplies (that is, 3.3 V/2.5 V or 1.8 V for the MAX IIG and MAX IIZ devices). ISP can be performed anytime after V_{CCINT} and all V_{CCIO} banks have been fully powered and the device has completed the configuration power-up time. By default, during in-system programming, the I/O pins are tri-stated and weakly pulled-up to V_{CCIO} to eliminate board conflicts. The insystem programming clamp and real-time ISP feature allow user control of I/O state or behavior during ISP.

For more information, refer to "In-System Programming Clamp" on page 3–6 and "Real-Time ISP" on page 3–7.

These devices also offer an ISP_DONE bit that provides safe operation when insystem programming is interrupted. This ISP_DONE bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

Real-Time ISP

For systems that require more than DC logic level control of I/O pins, the real-time ISP feature allows you to update the CFM block with a new design image while the current design continues to operate in the SRAM logic array and I/O pins. A new programming file is updated into the MAX II device without halting the original design's operation, saving down-time costs for remote or field upgrades. The updated CFM block configures the new design into the SRAM upon the next power cycle. It is also possible to execute an immediate configuration of the SRAM without a power cycle by using a specific sequence of ISP commands. The configuration of SRAM without a power cycle takes a specific amount of time (t_{CONFIG}). During this time, the I/O pins are tri-stated and weakly pulled-up to V_{CCID} .

Design Security

All MAX II devices contain a programmable security bit that controls access to the data programmed into the CFM block. When this bit is programmed, design programming information, stored in the CFM block, cannot be copied or retrieved. This feature provides a high level of design security because programmed data within flash memory cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is erased. The SRAM is also invisible and cannot be accessed regardless of the security bit setting. The UFM block data is not protected by the security bit and is accessible through JTAG or logic array connections.

Programming with External Hardware

MAX II devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera® ByteblasterMVTM, MasterBlasterTM, ByteBlasterTM II, and USB-Blaster cables.

BP Microsystems, System General, and other programming hardware manufacturers provide programming support for Altera devices. Check their websites for device support information.

Referenced Documents

This chapter references the following documents:

- DC and Switching Characteristics chapter in the MAX II Device Handbook
- IEEE 1149.1 (JTAG) Boundary-Scan Testing for MAX II Devices chapter in the MAX II Device Handbook
- Real-Time ISP and ISP Clamp for MAX II Devices chapter in the MAX II Device Handbook
- Using Jam STAPL for ISP via an Embedded Processor chapter in the MAX II Device Handbook

4. Hot Socketing and Power-On Reset in MAX II Devices

MII51004-2.1

Introduction

MAX[®] II devices offer hot socketing, also known as hot plug-in or hot swap, and power sequencing support. Designers can insert or remove a MAX II board in a system during operation without undesirable effects to the system bus. The hot socketing feature removes some of the difficulties designers face when using components on printed circuit boards (PCBs) that contain a mixture of 3.3-, 2.5-, 1.8-, and 1.5-V devices.

The MAX II device hot socketing feature provides:

- Board or device insertion and removal
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter contains the following sections:

- "MAX II Hot-Socketing Specifications" on page 4–1
- "Power-On Reset Circuitry" on page 4–5

MAX II Hot-Socketing Specifications

MAX II devices offer all three of the features required for the hot-socketing capability listed above without any external components or special design requirements. The following are hot-socketing specifications:

- The device can be driven before and during power-up or power-down without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.
- Signal pins do not drive the V_{CCIO} or V_{CCINT} power supplies. External input signals to device I/O pins do not power the device V_{CCIO} or V_{CCINT} power supplies via internal paths. This is true if the V_{CCINT} and the V_{CCIO} supplies are held at GND.

Devices Can Be Driven before Power-Up

Signals can be driven into the MAX II device I/O pins and GCLK[3..0] pins before or during power-up or power-down without damaging the device. MAX II devices support any power-up or power-down sequence (V_{CCIO1} , V_{CCIO2} , V_{CCIO3} , V_{CCIO4} , V_{CCINT}), simplifying the system-level design.

Make sure that the V_{CCNT} is within the recommended operating range even though SRAM download has completed.

Each I/O and clock pin has the circuitry shown in Figure 4–1.

Figure 4–1. Hot Socketing Circuit Block Diagram for MAX II Devices



The POR circuit monitors V_{CCINT} and V_{CCIO} voltage levels and keeps I/O pins tri-stated until the device has completed its flash memory configuration of the SRAM logic. The weak pull-up resistor (R) from the I/O pin to V_{CCIO} is enabled during download to keep the I/O pins from floating. The 3.3-V tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO} and/or V_{CCINT} are powered, and it prevents the I/O pins from driving out when the device is not fully powered or operational. The hot socket circuit prevents I/O pins from internally powering V_{CCIO} and V_{CCINT} when driven by external signals before the device is powered.

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For information about 5.0-V tolerance, refer to the *Using MAX II Devices in Multi-Voltage Systems* chapter in the *MAX II Device Handbook*.

Figure 4–2 shows a transistor-level cross section of the MAX II device I/O buffers. This design ensures that the output buffers do not drive when V_{CCIO} is powered before V_{CCINT} or if the I/O pad voltage is higher than V_{CCIO} . This also applies for sudden voltage spikes during hot insertion. The V_{PAD} leakage current charges the 3.3-V tolerant circuit capacitance.

When the I/O pin receives a negative ESD zap at the pin that is less than -0.7 V (0.7 V is the voltage drop across a diode), the intrinsic

P-Substrate/N+ drain diode is forward biased. Therefore, the discharge ESD current path is from GND to the I/O pin, as shown in Figure 4–4.





Power-On Reset Circuitry

MAX II devices have POR circuits to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up. The POR circuit monitors these voltages, triggering download from the non-volatile configuration flash memory (CFM) block to the SRAM logic, maintaining tri-state of the I/O pins (with weak pull-up resistors enabled) before and during this process. When the MAX II device enters user mode, the POR circuit releases the I/O pins to user functionality. The POR circuit of the MAX II (except MAX IIZ) device continues to monitor the V_{CCINT} voltage level to detect a brown-out condition. The POR circuit of the MAX IIZ device does not monitor the V_{CCINT} voltage level after the device enters into user mode. More details are provided in the following sub-sections.

Referenced Documents

This chapter refereces the following documents:

- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- Using MAX II Devices in Multi-Voltage Systems chapter in the MAX II Device Handbook

Document Revision History

Table 4–1 shows the revision history for this chapter.

Table 4–1.	Document Revision History
	Boournent novioren motory

Date and Revision	Changes Made	Summary of Changes
October 2008, version2.1	 Updated "MAX II Hot-Socketing Specifications" and "Power-On Reset Circuitry" sections. 	_
	 Updated New Document Format. 	
December 2007, version 2.0	 Updated "Hot Socketing Feature Implementation in MAX II Devices" section. 	Updated document with MAX IIZ information.
	 Updated "Power-On Reset Circuitry" section. 	
	■ Updated Figure 4–5.	
	 Added "Referenced Documents" section. 	
December 2006, version 1.5	 Added document revision history. 	_
February 2006,	 Updated "MAX II Hot-Socketing Specifications" section. 	_
version 1.4	 Updated "AC and DC Specifications" section. 	
	 Updated "Power-On Reset Circuitry" section. 	
June 2005, version 1.3	 Updated AC and DC specifications on page 4-2. 	_
December 2004,	 Added content to Power-Up Characteristics section. 	—
version 1.2	■ Updated Figure 4-5.	
June 2004, version 1.1	Corrected Figure 4-2.	_

			MAX II / MAX IIG							MAX IIZ						
			-3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade			
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	
f _{cnt}	Maximum global clock frequency for 16-bit counter	—		304.0 <i>(1)</i>		247.5		201.1		184.1		123.5		118.3	MHz	

Table 5–24. EPM570 Global Clock External I/O Timing Parameters (Part 2 of 2)

Note to Table 5-24:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5–25 shows the external I/O timing parameters for EPM1270 devices.

Table 5-25. EPM1270 Global Clock External I/O Timing Parameters

			MAX II / MAX IIG								
			–3 Speed Grade –4 Speed Grade			–5 Spee					
Symbol	Parameter	Condition	Min	Max	Min	Max	Min	Max	Unit		
t _{PD1}	Worst case pin-to-pin delay through 1 look-up table (LUT)	10 pF		6.2		8.1	_	10.0	ns		
t _{PD2}	Best case pin-to-pin delay through 1 LUT	10 pF	_	3.7	_	4.8	—	5.9	ns		
t _{su}	Global clock setup time	—	1.2	—	1.5		1.9	—	ns		
t _H	Global clock hold time	—	0	—	0		0	—	ns		
t _{co}	Global clock to output delay	10 pF	2.0	4.6	2.0	5.9	2.0	7.3	ns		
t _{ch}	Global clock high time	—	166	—	216		266	—	ps		
t _{cL}	Global clock low time	—	166	—	216	—	266	—	ps		
t _{cnt}	Minimum global clock period for 16-bit counter	_	3.3	_	4.0		5.0	_	ns		
f _{cnt}	Maximum global clock frequency for 16-bit counter	_		304.0 (1)	_	247.5	_	201.1	MHz		

Note to Table 5-25:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

			Μ	AX II /	MAX IIG	i								
		–3 Speed Grade		-4 S Gr	–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		peed ade	–8 Speed Grade		
I/O Standa	rd	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
3.3-V LVTTL	16 mA	—	0	—	0	_	0		0	_	0	_	0	ps
	8 mA	—	65	—	84	—	104	_	-6	—	-2	—	-3	ps
3.3-V LVCMOS	8 mA	—	0	_	0	—	0	_	0	_	0	—	0	ps
	4 mA	_	65	_	84	—	104	_	-6		-2		-3	ps
2.5-V LVTTL /	14 mA	—	122	—	158	—	195	_	-63	—	-71	—	-88	ps
LVCMOS	7 mA	—	193	_	251	_	309	_	10	_	-1	_	1	ps
1.8-V LVTTL /	6 mA	—	568	—	738	—	909	_	128	_	118	_	118	ps
LVCMOS	3 mA	—	654	—	850	—	1,046	_	352	—	327	—	332	ps
1.5-V LVCMOS	4 mA	—	1,059	_	1,376	_	1,694	_	421	_	400	_	400	ps
	2 mA	—	1,167	—	1,517	—	1,867	—	757	_	743	—	743	ps
3.3-V PCI	20 mA	—	3	—	4	—	5		-6	—	-2		-3	ps

Table 5–29. External Timing Output Delay and $t_{\mbox{\tiny OD}}$ Adders for Fast Slew Rate

	Γ	II XAN	/ MAX IIO)		MAX IIZ								
			–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		Speed rade	–8 Speed Grade		
I/O Standa	rd	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
3.3-V LVTTL	16 mA	—	7,064		6,745	—	6,426	_	5,966	—	5,992	—	6,118	ps
	8 mA	_	7,946		7,627		7,308	_	6,541	—	6,570	_	6,720	ps
3.3-V LVCMOS	8 mA	—	7,064		6,745		6,426	_	5,966	—	5,992	—	6,118	ps
	4 mA	—	7,946		7,627		7,308	_	6,541	—	6,570	—	6,720	ps
2.5-V LVTTL /	14 mA	—	10,434		10,115		9,796	_	9,141	—	9,154	—	9,297	ps
LVCMOS	7 mA	—	11,548		11,229		10,910	_	9,861	—	9,874	—	10,037	ps
1.8-V LVTTL /	6 mA	—	22,927		22,608		22,289	_	21,811	—	21,854	—	21,857	ps
LVCMOS	3 mA	—	24,731		24,412		24,093	_	23,081	—	23,034	—	23,107	ps
1.5-V LVCMOS	4 mA	—	38,723		38,404		38,085	_	39,121	—	39,124	—	39,124	ps
	2 mA	—	41,330		41,011		40,692	_	40,631	—	40,634	—	40,634	ps
3.3-V PCI	20 mA	—	261		339	_	418	_	6,644	—	6,627	—	6,914	ps

Symbol	Parameter	Min	Max	Unit
t _{JPSU}	JTAG port setup time (2)	8	_	ns
t _{jph}	JTAG port hold time	10	_	ns
t _{JPC0}	JTAG port clock to output (2)		15	ns
t _{JPZX}	JTAG port high impedance to valid output (2)	_	15	ns
t _{JPXZ}	JTAG port valid output to high impedance (2)	_	15	ns
t _{ussu}	Capture register setup time	8	_	ns
t _{JSH}	Capture register hold time	10	_	ns
t _{usco}	Update register clock to output		25	ns
t _{JSZX}	Update register high impedance to valid output	_	25	ns
t _{JSXZ}	Update register valid output to high impedance		25	ns

Table 5–34. MAX II JTAG Timing Parameters (Part 2 of 2)

Notes to Table 5-34:

(1) Minimum clock period specified for 10 pF load on the TDO pin. Larger loads on TDO will degrade the maximum TCK frequency.

(2) This specification is shown for 3.3-V LVTTL/LVCMOS and 2.5-V LVTTL/LVCMOS operation of the JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the t_{JPSU} minimum is 6 ns and t_{JPC0}, t_{JPZX}, and t_{JPXZ} are maximum values at 35 ns.

Referenced Documents

This chapter references the following documents:

- *I/O Structure* section in the *MAX II Architecture* chapter in the *MAX II Device Handbook*
- Hot Socketing and Power-On Reset in MAX II Devices chapter in the MAX II Device Handbook
- Operating Requirements for Altera Devices Data Sheet
- PowerPlay Power Analysis chapter in volume 3 of the Quartus II Handbook
- Understanding and Evaluating Power in MAX II Devices chapter in the MAX II Device Handbook
- Understanding Timing in MAX II Devices chapter in the MAX II Device Handbook
- Using MAX II Devices in Multi-Voltage Systems chapter in the MAX II Device Handbook