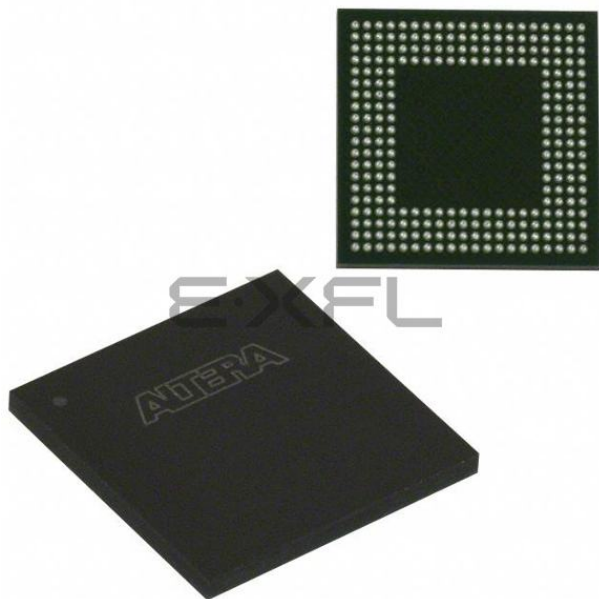




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Understanding [Embedded - CPLDs \(Complex Programmable Logic Devices\)](#)

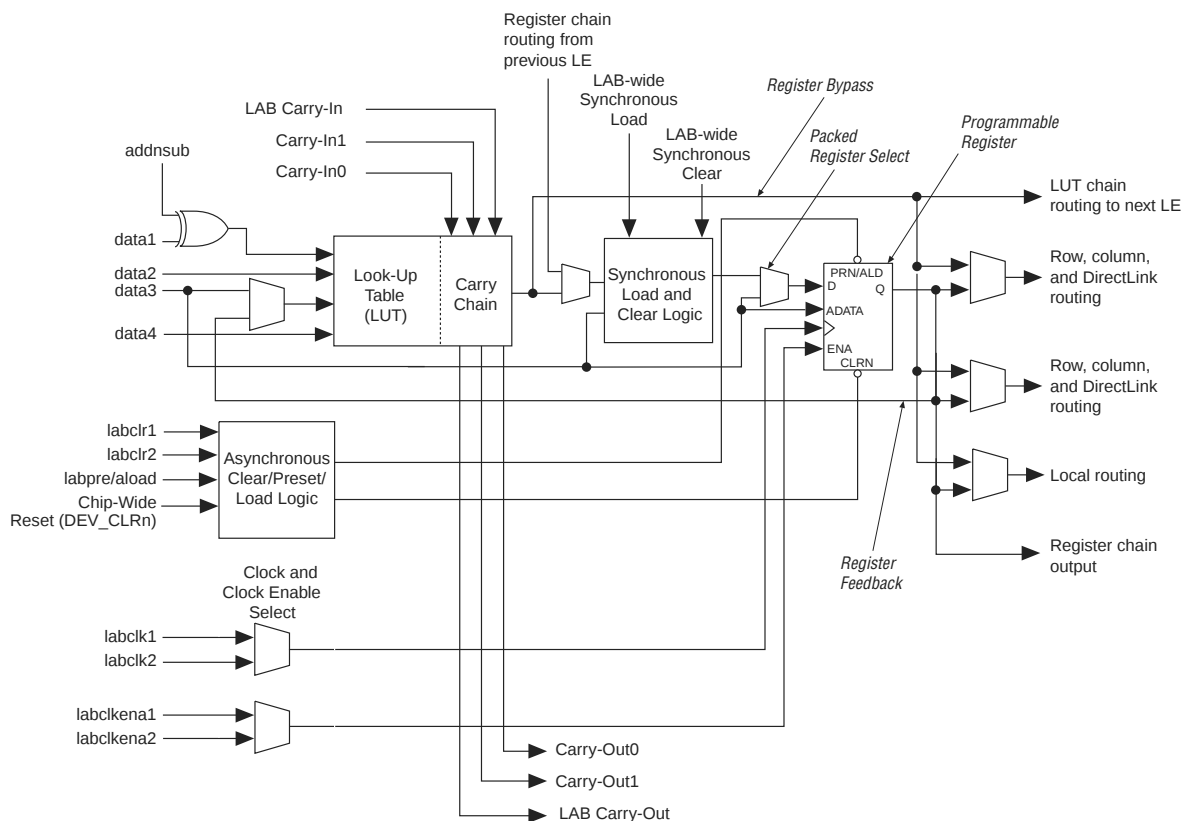
Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.4 ns
Voltage Supply - Internal	2.5V, 3.3V
Number of Logic Elements/Blocks	570
Number of Macrocells	440
Number of Gates	-
Number of I/O	160
Operating Temperature	0°C ~ 85°C (TJ)
Mounting Type	Surface Mount
Package / Case	256-TFBGA
Supplier Device Package	256-MBGA (11x11)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm570m256c4n

Figure 2-6. MAX II LE



Each LE's programmable register can be configured for D, T, JK, or SR operation. Each register has data, true asynchronous load data, clock, clock enable, clear, and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any LE can drive the register's clock and clear control signals. Either general-purpose I/O pins or LEs can drive the clock enable, preset, asynchronous load, and asynchronous data. The asynchronous load data input comes from the data3 input of the LE. For combinational functions, the LUT output bypasses the register and drives directly to the LE outputs.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and DirectLink routing connections and one drives local interconnect resources. This allows the LUT to drive one output while the register drives another output. This register packing feature improves device utilization because the device can use the register and the LUT for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same LE so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

LUT Chain and Register Chain

In addition to the three general routing outputs, the LEs within an LAB have LUT chain and register chain outputs. LUT chain connections allow LUTs within the same LAB to cascade together for wide input functions. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows an LAB to use LUTs for a single combinational function and the registers to be used for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. Refer to “MultiTrack Interconnect” on page 2-12 for more information about LUT chain and register chain connections.

addnsub Signal

The LE's dynamic adder/subtractor feature saves logic resources by using one set of LEs to implement both an adder and a subtractor. This feature is controlled by the LAB-wide control signal `addnsub`. The `addnsub` signal sets the LAB to perform either $A + B$ or $A - B$. The LUT computes addition; subtraction is computed by adding the two's complement of the intended subtractor. The LAB-wide signal converts to two's complement by inverting the B bits within the LAB and setting carry-in to 1, which adds one to the least significant bit (LSB). The LSB of an adder/subtractor must be placed in the first LE of the LAB, where the LAB-wide `addnsub` signal automatically sets the carry-in to 1. The Quartus II Compiler automatically places and uses the adder/subtractor feature when using adder/subtractor parameterized functions.

LE Operating Modes

The MAX II LE can operate in one of the following modes:

- “Normal Mode”
- “Dynamic Arithmetic Mode”

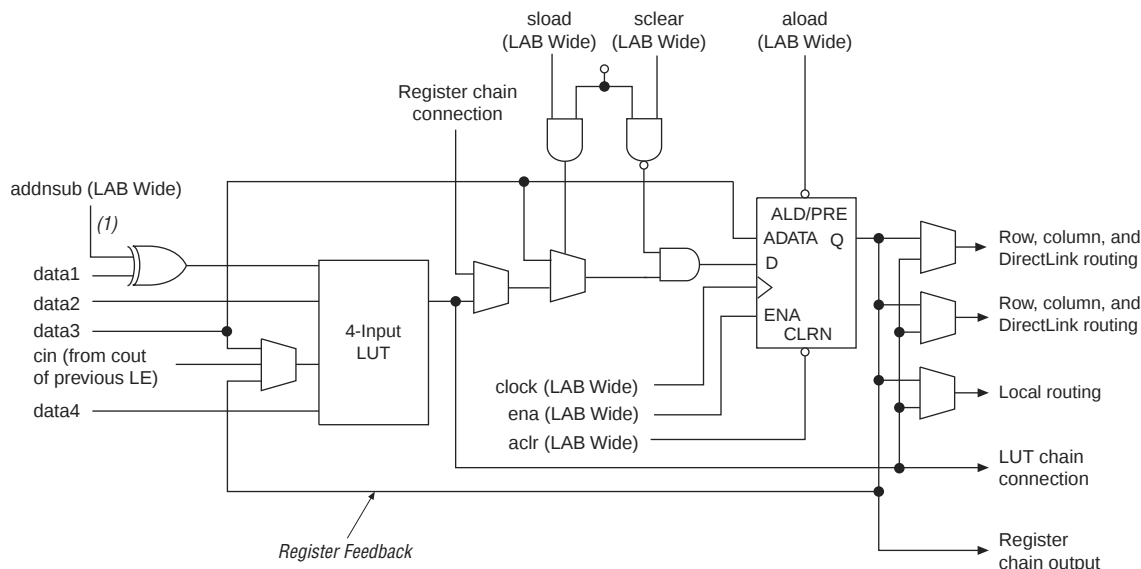
Each mode uses LE resources differently. In each mode, eight available inputs to the LE, the four data inputs from the LAB local interconnect, `carry-in0` and `carry-in1` from the previous LE, the LAB carry-in from the previous carry-chain LAB, and the register chain connection are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset/load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes. The `addnsub` control signal is allowed in arithmetic mode.

The Quartus II software, in conjunction with parameterized functions such as library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions.

Normal Mode

The normal mode is suitable for general logic applications and combinational functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (see Figure 2-7). The Quartus II Compiler automatically selects the carry-in or the data3 signal as one of the inputs to the LUT. Each LE can use LUT chain connections to drive its combinational output directly to the next LE in the LAB. Asynchronous load data for the register comes from the data3 input of the LE. LEs in normal mode support packed registers.

Figure 2-7. LE in Normal Mode



Note to Figure 2-7:

(1) This signal is only allowed in normal mode if the LE is at the end of an adder/subtractor chain.

Dynamic Arithmetic Mode

The dynamic arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An LE in dynamic arithmetic mode uses four 2-input LUTs configurable as a dynamic adder/subtractor. The first two 2-input LUTs compute two summations based on a possible carry-in of 1 or 0; the other two LUTs generate carry outputs for the two chains of the carry-select circuitry. As shown in Figure 2-8, the LAB carry-in signal selects either the carry-in0 or carry-in1 chain. The selected chain's logic level in turn determines which parallel sum is generated as a combinational or registered output. For example, when implementing an adder, the sum output is the selection of two possible calculated sums:

$$\text{data1} + \text{data2} + \text{carry in0}$$

or

$$\text{data1} + \text{data2} + \text{carry-in1}$$

The speed advantage of the carry-select chain is in the parallel precomputation of carry chains. Since the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delays between LAB carry-in generation (LE 5 and LE 10) are now part of the critical path. This feature allows the MAX II architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

Figure 2-9 shows the carry-select circuitry in an LAB for a 10-bit full adder. One portion of the LUT generates the sum of two bits using the input signals and the appropriate carry-in bit; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT generates carry-out bits. An LAB-wide carry-in bit selects which chain is used for the addition of given inputs. The carry-in signal for each chain, carry-in0 or carry-in1, selects the carry-out to carry forward to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is fed to local, row, or column interconnects.

Figure 2-9. Carry-Select Chain

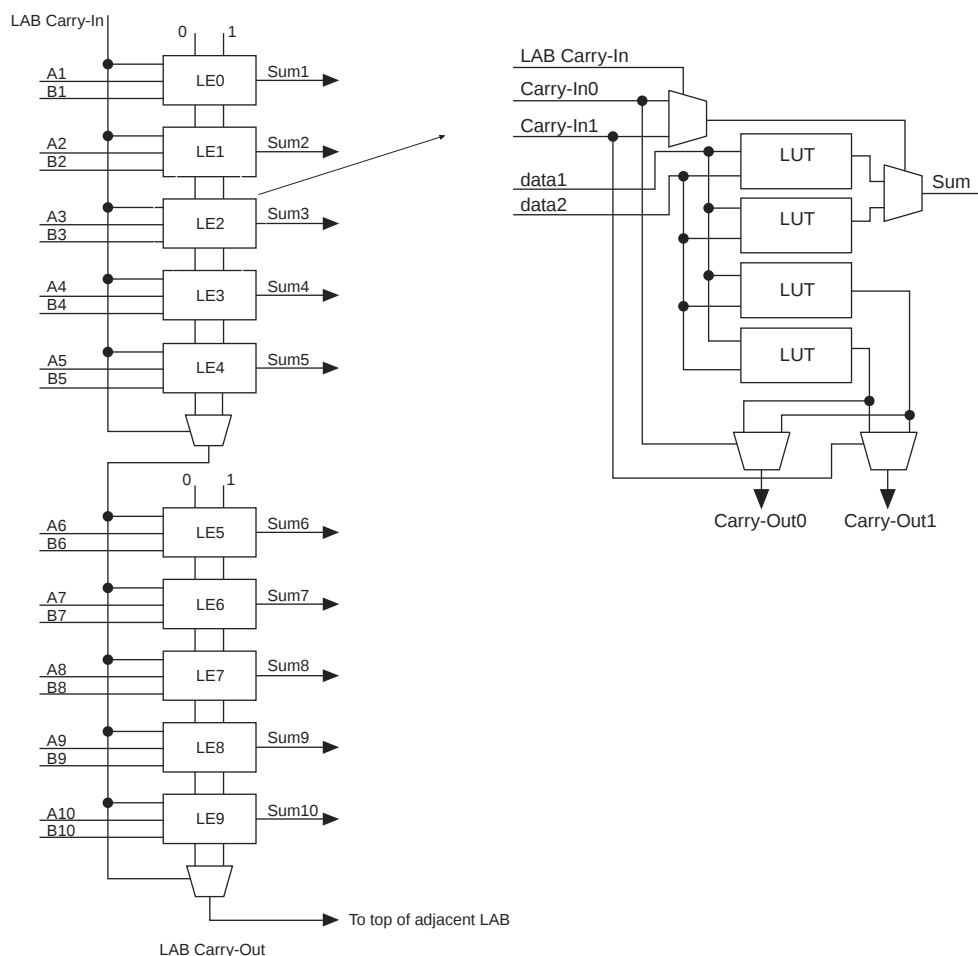
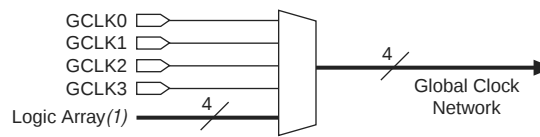


Figure 2-13. Global Clock Generation

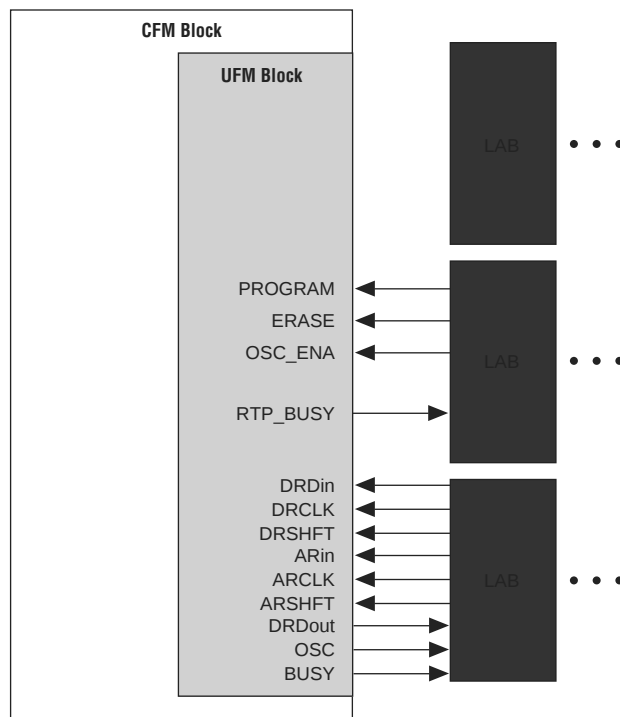


Note to Figure 2-13:

(1) Any I/O pin can use a MultiTrack interconnect to route as a logic array-generated global clock signal.

The global clock network drives to individual LAB column signals, LAB column clocks [3..0], that span an entire LAB column from the top to the bottom of the device. Unused global clocks or control signals in a LAB column are turned off at the LAB column clock buffers shown in Figure 2-14. The LAB column clocks [3..0] are multiplexed down to two LAB clock signals and one LAB clear signal. Other control signal types route from the global clock network into the LAB local interconnect. See “LAB Control Signals” on page 2-5 for more information.

Figure 2-16. EPM240 UFM Block LAB Row Interface *(Note 1)*



Note to Figure 2-16:

- (1) The UFM block inputs and outputs can drive to/from all types of interconnects, not only DirectLink interconnects from adjacent row LABs.

I/O Structure

IOEs support many features, including:

- LVTTTL and LVCMOS I/O standards
- 3.3-V, 32-bit, 66-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Programmable drive strength control
- Weak pull-up resistors during power-up and in system programming
- Slew-rate control
- Tri-state buffers with individual output enable control
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Unique output enable per pin
- Open-drain outputs
- Schmitt trigger inputs
- Fast I/O connection
- Programmable input delay

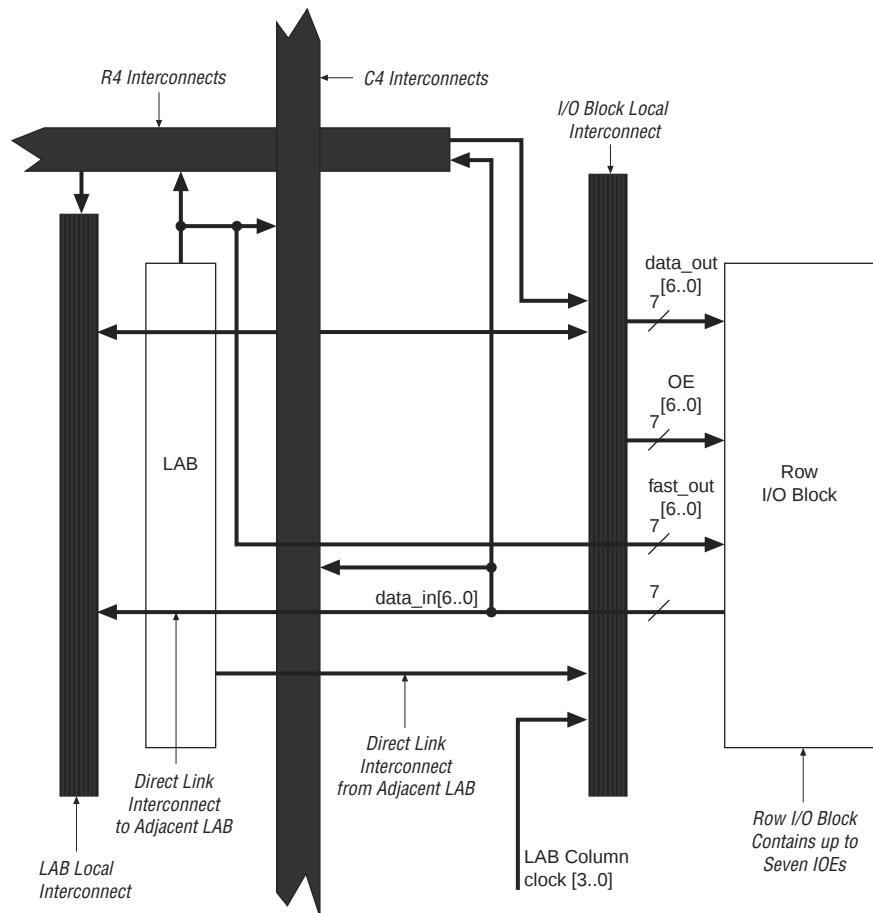
MAX II device IOEs contain a bidirectional I/O buffer. Figure 2–19 shows the MAX II IOE structure. Registers from adjacent LABs can drive to or be driven from the IOE's bidirectional I/O buffers. The Quartus II software automatically attempts to place registers in the adjacent LAB with fast I/O connection to achieve the fastest possible clock-to-output and registered output enable timing. For input registers, the Quartus II software automatically routes the register to guarantee zero hold time. You can set timing assignments in the Quartus II software to achieve desired I/O timing.

Fast I/O Connection

A dedicated fast I/O connection from the adjacent LAB to the IOEs within an I/O block provides faster output delays for clock-to-output and t_{PD} propagation delays. This connection exists for data output signals, not output enable signals or input signals. Figure 2–20, Figure 2–21, and Figure 2–22 illustrate the fast I/O connection.

Figure 2-20 shows how a row I/O block connects to the logic array.

Figure 2-20. Row I/O Block Connection to the Interconnect (Note 1)

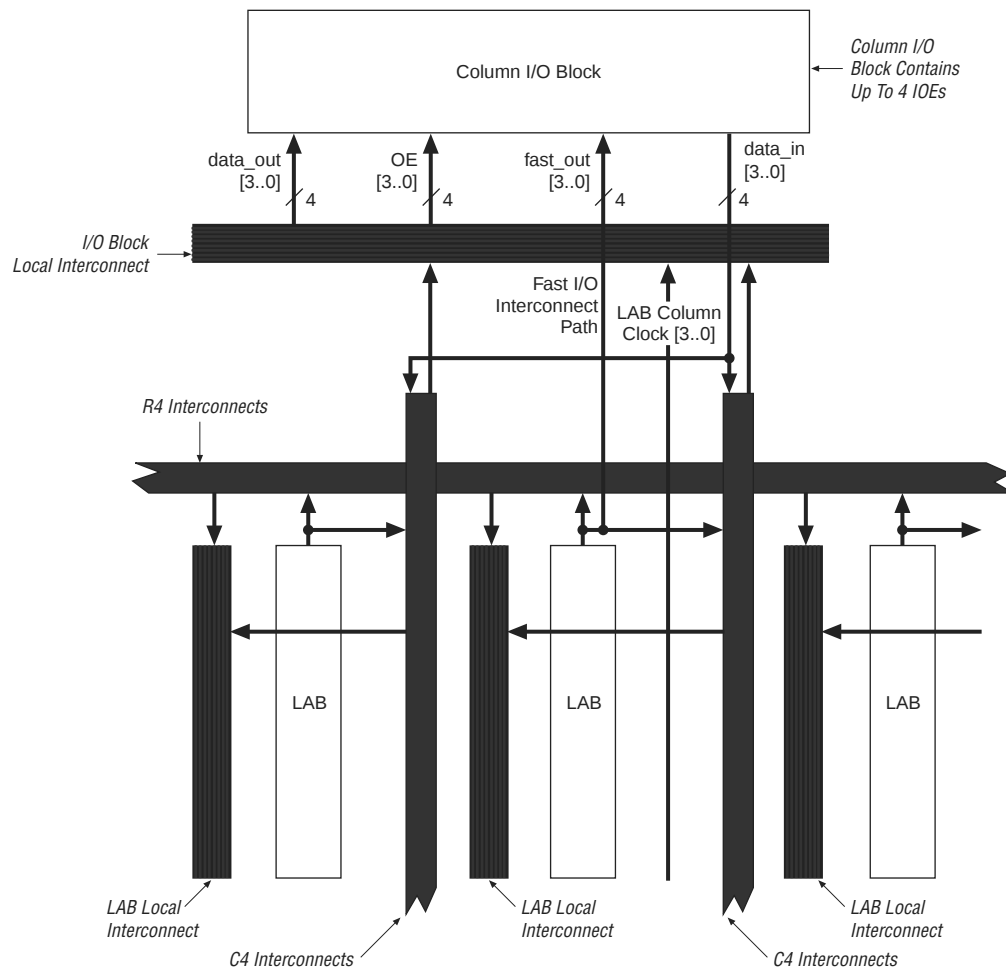


Note to Figure 2-20:

- (1) Each of the seven IOEs in the row I/O block can have one data_out or fast_out output, one OE output, and one data_in input.

Figure 2–21 shows how a column I/O block connects to the logic array.

Figure 2–21. Column I/O Block Connection to the Interconnect (*Note 1*)



Note to Figure 2–21:

(1) Each of the four IOEs in the column I/O block can have one data_out or fast_out output, one OE output, and one data_in input.

I/O Standards and Banks

MAX II device IOEs support the following I/O standards:

- 3.3-V LVTTTL/LVCMOS
- 2.5-V LVTTTL/LVCMOS
- 1.8-V LVTTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI

Table 2-6. Programmable Drive Strength (*Note 1*)

I/O Standard	IOH/IOL Current Strength Setting (mA)
3.3-V LVTTTL	16
	8
3.3-V LVCMOS	8
	4
2.5-V LVTTTL/LVCMOS	14
	7
1.8-V LVTTTL/LVCMOS	6
	3
1.5-V LVCMOS	4
	2

Note to Table 2-6:

- (1) The I_{OH} current strength numbers shown are for a condition of a $V_{OUT} = V_{OH}$ minimum, where the V_{OH} minimum is specified by the I/O standard. The I_{OL} current strength numbers shown are for a condition of a $V_{OUT} = V_{OL}$ maximum, where the V_{OL} maximum is specified by the I/O standard. For 2.5-V LVTTTL/LVCMOS, the I_{OH} condition is $V_{OUT} = 1.7$ V and the I_{OL} condition is $V_{OUT} = 0.7$ V.

Slew-Rate Control

The output buffer for each MAX II device I/O pin has a programmable output slew-rate control that can be configured for low noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal output delay to rising and falling edges. The lower the voltage standard (for example, 1.8-V LVTTTL) the larger the output delay when slow slew is enabled. Each I/O pin has an individual slew-rate control, allowing the designer to specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges.

Open-Drain Output

MAX II devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that can be asserted by any of several devices. This output can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX II devices can be used as an additional ground pin. This programmable ground feature does not require the use of the associated LEs in the device. In the Quartus II software, unused pins can be set as programmable GND on a global default basis or they can be individually assigned. Unused pins also have the option of being set as tri-stated input pins.

Connect VCCIO pins to either a 1.5-V, 1.8 V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (that is, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems. Table 2-7 summarizes MAX II MultiVolt I/O support.

Table 2-7. MAX II MultiVolt I/O Support (Note 1)

VCCIO (V)	Input Signal					Output Signal				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓	✓	—	✓	—	—	—	—
1.8	✓	✓	✓	✓	—	✓ (2)	✓	—	—	—
2.5	—	—	✓	✓	—	✓ (3)	✓ (3)	✓	—	—
3.3	—	—	✓ (4)	✓	✓ (5)	✓ (6)	✓ (6)	✓ (6)	✓	✓ (7)

Notes to Table 2-7:

- (1) To drive inputs higher than V_{CCIO} but less than 4.0 V including the overshoot, disable the I/O clamp diode. However, to drive 5.0-V inputs to the device, enable the I/O clamp diode to prevent V_i from rising above 4.0 V.
- (2) When $V_{CCIO} = 1.8$ V, a MAX II device can drive a 1.5-V device with 1.8-V tolerant inputs.
- (3) When $V_{CCIO} = 2.5$ V, a MAX II device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.
- (4) When $V_{CCIO} = 3.3$ V and a 2.5-V input signal feeds an input pin, the VCCIO supply current will be slightly larger than expected.
- (5) MAX II devices can be 5.0-V tolerant with the use of an external resistor and the internal I/O clamp diode on the EPM1270 and EPM2210 devices.
- (6) When $V_{CCIO} = 3.3$ V, a MAX II device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.
- (7) When $V_{CCIO} = 3.3$ V, a MAX II device can drive a device with 5.0-V TTL inputs but not 5.0-V CMOS inputs. In the case of 5.0-V CMOS, open-drain setting with internal I/O clamp diode (available only on EPM1270 and EPM2210 devices) and external resistor is required.



For information about output pin source and sink current guidelines, refer to the AN 428: MAX II CPLD Design Guidelines.

Referenced Documents

This chapter referenced the following documents:

- AN 428: MAX II CPLD Design Guidelines
- DC and Switching Characteristics chapter in the MAX II Device Handbook
- Hot Socketing and Power-On Reset in MAX II Devices chapter in the MAX II Device Handbook
- Using User Flash Memory in MAX II Devices chapter in the MAX II Device Handbook

Real-Time ISP

For systems that require more than DC logic level control of I/O pins, the real-time ISP feature allows you to update the CFM block with a new design image while the current design continues to operate in the SRAM logic array and I/O pins. A new programming file is updated into the MAX II device without halting the original design's operation, saving down-time costs for remote or field upgrades. The updated CFM block configures the new design into the SRAM upon the next power cycle. It is also possible to execute an immediate configuration of the SRAM without a power cycle by using a specific sequence of ISP commands. The configuration of SRAM without a power cycle takes a specific amount of time (t_{CONFIG}). During this time, the I/O pins are tri-stated and weakly pulled-up to V_{CCIO} .

Design Security

All MAX II devices contain a programmable security bit that controls access to the data programmed into the CFM block. When this bit is programmed, design programming information, stored in the CFM block, cannot be copied or retrieved. This feature provides a high level of design security because programmed data within flash memory cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is erased. The SRAM is also invisible and cannot be accessed regardless of the security bit setting. The UFM block data is not protected by the security bit and is accessible through JTAG or logic array connections.

Programming with External Hardware

MAX II devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera® ByteblasterMV™, MasterBlaster™, ByteBlaster™ II, and USB-Blaster cables.

BP Microsystems, System General, and other programming hardware manufacturers provide programming support for Altera devices. Check their websites for device support information.

Referenced Documents

This chapter references the following documents:

- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *IEEE 1149.1 (JTAG) Boundary-Scan Testing for MAX II Devices* chapter in the *MAX II Device Handbook*
- *Real-Time ISP and ISP Clamp for MAX II Devices* chapter in the *MAX II Device Handbook*
- *Using Jam STAPL for ISP via an Embedded Processor* chapter in the *MAX II Device Handbook*

I/O Pins Remain Tri-Stated during Power-Up

A device that does not support hot-socketing may interrupt system operation or cause contention by driving out before or during power-up. In a hot socketing situation, the MAX II device's output buffers are turned off during system power-up. MAX II devices do not drive out until the device attains proper operating conditions and is fully configured. Refer to "Power-On Reset Circuitry" on page 4-5 for information about turn-on voltages.

Signal Pins Do Not Drive the V_{CCIO} or V_{CCINT} Power Supplies

MAX II devices do not have a current path from I/O pins or GCLK[3..0] pins to the V_{CCIO} or V_{CCINT} pins before or during power-up. A MAX II device may be inserted into (or removed from) a system board that was powered up without damaging or interfering with system-board operation. When hot socketing, MAX II devices may have a minimal effect on the signal integrity of the backplane.

AC and DC Specifications

You can power up or power down the V_{CCIO} and V_{CCINT} pins in any sequence. During hot socketing, the I/O pin capacitance is less than 8 pF. MAX II devices meet the following hot socketing specifications:

- The hot socketing DC specification is: $|I_{IOPIN}| < 300 \mu A$.
- The hot socketing AC specification is: $|I_{IOPIN}| < 8 \text{ mA}$ for 10 ns or less.



MAX II devices are immune to latch-up when hot socketing. If the TCK JTAG input pin is driven high during hot socketing, the current on that pin might exceed the specifications above.

I_{IOPIN} is the current at any user I/O pin on the device. The AC specification applies when the device is being powered up or powered down. This specification takes into account the pin capacitance but not board trace and external loading capacitance. Additional capacitance for trace, connector, and loading must be taken into consideration separately. The peak current duration due to power-up transients is 10 ns or less.

The DC specification applies when all V_{CC} supplies to the device are stable in the powered-up or powered-down conditions.

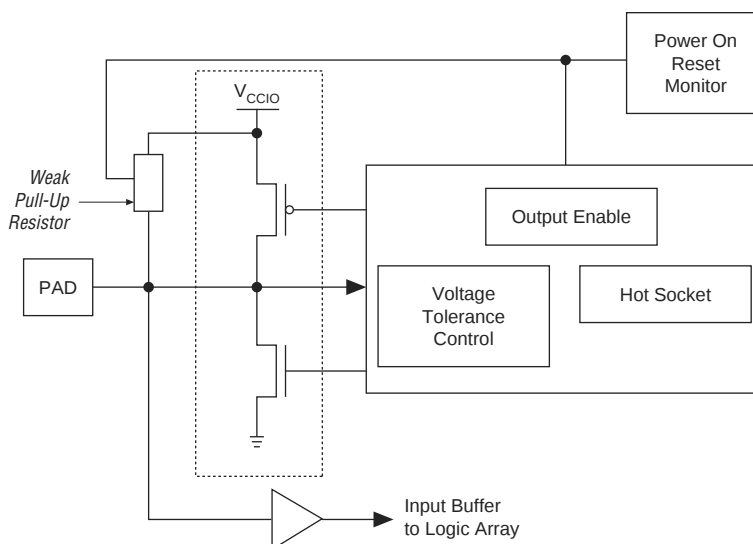
Hot Socketing Feature Implementation in MAX II Devices

The hot socketing feature turns off (tri-states) the output buffer during the power-up event (either V_{CCINT} or V_{CCIO} supplies) or power-down event. The hot-socket circuit generates an internal HOTSKT signal when either V_{CCINT} or V_{CCIO} is below the threshold voltage during power-up or power-down. The HOTSKT signal cuts off the output buffer to make sure that no DC current (except for weak pull-up leaking) leaks through the pin. When V_{CC} ramps up very slowly during power-up, V_{CC} may still be relatively low even after the power-on reset (POR) signal is released and device configuration is complete.

 Make sure that the V_{CCINT} is within the recommended operating range even though SRAM download has completed.

Each I/O and clock pin has the circuitry shown in Figure 4-1.

Figure 4-1. Hot Socketing Circuit Block Diagram for MAX II Devices



The POR circuit monitors V_{CCINT} and V_{CCIO} voltage levels and keeps I/O pins tri-stated until the device has completed its flash memory configuration of the SRAM logic. The weak pull-up resistor (R) from the I/O pin to V_{CCIO} is enabled during download to keep the I/O pins from floating. The 3.3-V tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO} and/or V_{CCINT} are powered, and it prevents the I/O pins from driving out when the device is not fully powered or operational. The hot socket circuit prevents I/O pins from internally powering V_{CCIO} and V_{CCINT} when driven by external signals before the device is powered.

 For information about 5.0-V tolerance, refer to the *Using MAX II Devices in Multi-Voltage Systems* chapter in the *MAX II Device Handbook*.

Figure 4-2 shows a transistor-level cross section of the MAX II device I/O buffers. This design ensures that the output buffers do not drive when V_{CCIO} is powered before V_{CCINT} or if the I/O pad voltage is higher than V_{CCIO} . This also applies for sudden voltage spikes during hot insertion. The V_{PAD} leakage current charges the 3.3-V tolerant circuit capacitance.

5. DC and Switching Characteristics

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Introduction

System designers must consider the recommended DC and switching conditions discussed in this chapter to maintain the highest possible performance and reliability of the MAX[®] II devices. This chapter contains the following sections:

- “Operating Conditions” on page 5–1
- “Power Consumption” on page 5–8
- “Timing Model and Specifications” on page 5–8

Operating Conditions

Table 5–1 through Table 5–12 provide information about absolute maximum ratings, recommended operating conditions, DC electrical characteristics, and other specifications for MAX II devices.

Absolute Maximum Ratings

Table 5–1 shows the absolute maximum ratings for the MAX II device family.

Table 5–1. MAX II Device Absolute Maximum Ratings (*Note 1*), (*2*)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{CCINT}	Internal supply voltage (<i>3</i>)	With respect to ground	–0.5	4.6	V
V _{CCIO}	I/O supply voltage	—	–0.5	4.6	V
V _I	DC input voltage	—	–0.5	4.6	V
I _{OUT}	DC output current, per pin (<i>4</i>)	—	–25	25	mA
T _{STG}	Storage temperature	No bias	–65	150	°C
T _{AMB}	Ambient temperature	Under bias (<i>5</i>)	–65	135	°C
T _J	Junction temperature	TQFP and BGA packages under bias	—	135	°C

Notes to Table 5–1:

- (1) Refer to the *Operating Requirements for Altera Devices Data Sheet*.
- (2) Conditions beyond those listed in Table 5–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.
- (3) Maximum V_{CCINT} for MAX II devices is 4.6 V. For MAX IIG and MAX IIZ devices, it is 2.4 V.
- (4) Refer to *AN 286: Implementing LED Drivers in MAX & MAX II Devices* for more information about the maximum source and sink current for MAX II devices.
- (5) Refer to Table 5–2 for information about “under bias” conditions.

Table 5-17. t_{ZX} IOE Microparameter Adders for Fast Slew Rate (Part 2 of 2)

Standard		MAX II / MAX IIG						MAX IIZ						Unit
		−3 Speed Grade		−4 Speed Grade		−5 Speed Grade		−6 Speed Grade		−7 Speed Grade		−8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
1.5-V LVCMOS	4 mA	—	1,118	—	1,454	—	1,789	—	580	—	588	—	588	ps
	2 mA	—	2,410	—	3,133	—	3,856	—	915	—	923	—	923	ps
3.3-V PCI	20 mA	—	19	—	25	—	31	—	72	—	71	—	74	ps

Table 5-18. t_{ZX} IOE Microparameter Adders for Slow Slew Rate

Standard		MAX II / MAX IIG						MAX IIZ						Unit
		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	16 mA	—	6,350	—	6,050	—	5,749	—	5,951	—	5,952	—	6,063	ps
	8 mA	—	9,383	—	9,083	—	8,782	—	6,534	—	6,533	—	6,662	ps
3.3-V LVCMOS	8 mA	—	6,350	—	6,050	—	5,749	—	5,951	—	5,952	—	6,063	ps
	4 mA	—	9,383	—	9,083	—	8,782	—	6,534	—	6,533	—	6,662	ps
2.5-V LVTTTL / LVCMOS	14 mA	—	10,412	—	10,112	—	9,811	—	9,110	—	9,105	—	9,237	ps
	7 mA	—	13,613	—	13,313	—	13,012	—	9,830	—	9,835	—	9,977	ps
3.3-V PCI	20 mA	—	-75	—	-97	—	-120	—	6,534	—	6,533	—	6,662	ps

Table 5-19. t_{XZ} IOE Microparameter Adders for Fast Slew Rate

Standard		MAX II / MAX IIG						MAX IIZ						Unit
		-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTTL	16 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	8 mA	—	-56	—	-72	—	-89	—	-69	—	-69	—	-69	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	4 mA	—	-56	—	-72	—	-89	—	-69	—	-69	—	-69	ps
2.5-V LVTTTL / LVCMOS	14 mA	—	-3	—	-4	—	-5	—	-7	—	-11	—	-11	ps
	7 mA	—	-47	—	-61	—	-75	—	-66	—	-70	—	-70	ps
1.8-V LVTTTL / LVCMOS	6 mA	—	119	—	155	—	191	—	45	—	34	—	37	ps
	3 mA	—	207	—	269	—	331	—	34	—	22	—	25	ps
1.5-V LVCMOS	4 mA	—	606	—	788	—	970	—	166	—	154	—	155	ps
	2 mA	—	673	—	875	—	1,077	—	190	—	177	—	179	ps
3.3-V PCI	20 mA	—	71	—	93	—	114	—	-69	—	-69	—	-69	ps

Figure 5-4. UFM Program Waveforms

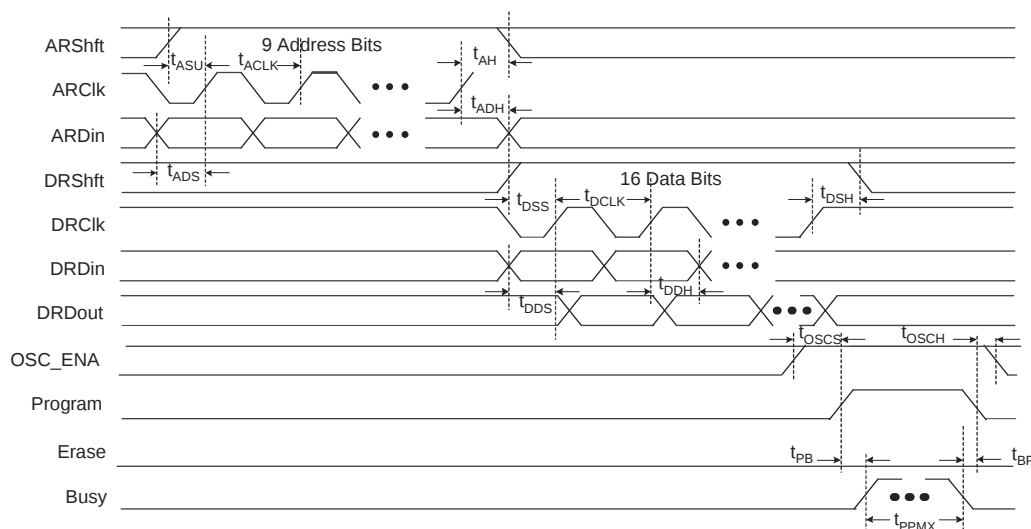


Figure 5-5. UFM Erase Waveform

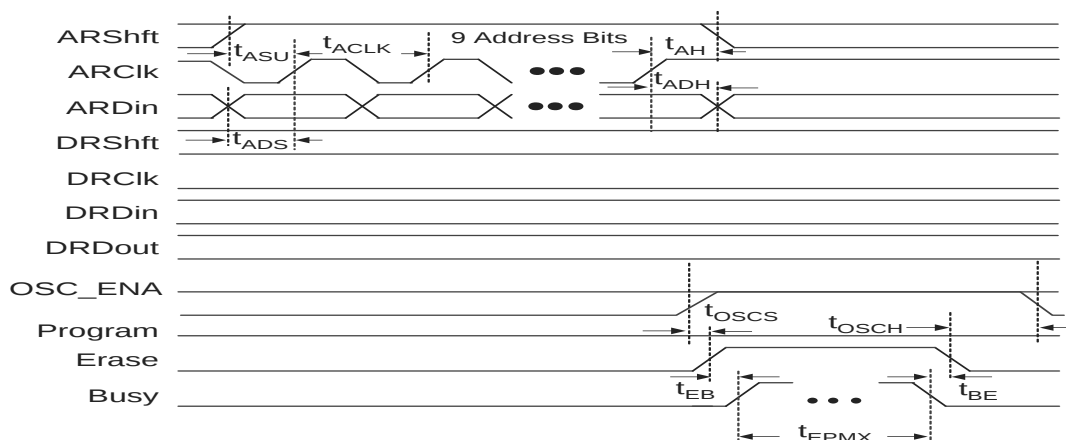


Table 5-22. Routing Delay Internal Timing Microparameters

Routing	MAX II / MAX IIG						MAX IIZ						Unit
	-3 Speed Grade		-4 Speed Grade		-5 Speed Grade		-6 Speed Grade		-7 Speed Grade		-8 Speed Grade		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{C4}	—	429	—	556	—	687	—	(1)	—	(1)	—	(1)	ps
t _{R4}	—	326	—	423	—	521	—	(1)	—	(1)	—	(1)	ps
t _{LOCAL}	—	330	—	429	—	529	—	(1)	—	(1)	—	(1)	ps

Note to Table 5-22:

(1) The numbers will only be available in a later revision.

Table 5-24. EPM570 Global Clock External I/O Timing Parameters (Part 2 of 2)

Symbol	Parameter	Condition	MAX II / MAX IIG						MAX IIZ						Unit
			−3 Speed Grade		−4 Speed Grade		−5 Speed Grade		−6 Speed Grade		−7 Speed Grade		−8 Speed Grade		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f _{CNT}	Maximum global clock frequency for 16-bit counter	—	—	304.0 (1)	—	247.5	—	201.1	—	184.1	—	123.5	—	118.3	MHz

Note to Table 5-24:

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5-25 shows the external I/O timing parameters for EPM1270 devices.

Table 5-25. EPM1270 Global Clock External I/O Timing Parameters

Symbol	Parameter	Condition	MAX II / MAX IIG						Unit
			–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		
			Min	Max	Min	Max	Min	Max	
t _{PD1}	Worst case pin-to-pin delay through 1 look-up table (LUT)	10 pF	—	6.2	—	8.1	—	10.0	ns
t _{PD2}	Best case pin-to-pin delay through 1 LUT	10 pF	—	3.7	—	4.8	—	5.9	ns
t _{SU}	Global clock setup time	—	1.2	—	1.5	—	1.9	—	ns
t _H	Global clock hold time	—	0	—	0	—	0	—	ns
t _{CO}	Global clock to output delay	10 pF	2.0	4.6	2.0	5.9	2.0	7.3	ns
t _{CH}	Global clock high time	—	166	—	216	—	266	—	ps
t _{CL}	Global clock low time	—	166	—	216	—	266	—	ps
t _{CNT}	Minimum global clock period for 16-bit counter	—	3.3	—	4.0	—	5.0	—	ns
f _{CNT}	Maximum global clock frequency for 16-bit counter	—	—	304.0 (1)	—	247.5	—	201.1	MHz

Note to Table 5-25:

- (1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5-34. MAX II JTAG Timing Parameters (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{JPSU}	JTAG port setup time (2)	8	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output (2)	—	15	ns
t_{JPZX}	JTAG port high impedance to valid output (2)	—	15	ns
t_{JPXZ}	JTAG port valid output to high impedance (2)	—	15	ns
t_{JSU}	Capture register setup time	8	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Notes to Table 5-34:

- (1) Minimum clock period specified for 10 pF load on the TDO pin. Larger loads on TDO will degrade the maximum TCK frequency.
- (2) This specification is shown for 3.3-V LVTTTL/LVCMOS and 2.5-V LVTTTL/LVCMOS operation of the JTAG pins. For 1.8-V LVTTTL/LVCMOS and 1.5-V LVCMOS, the t_{JPSU} minimum is 6 ns and t_{JPCO} , t_{JPZX} , and t_{JPXZ} are maximum values at 35 ns.

Referenced Documents

This chapter references the following documents:

- *I/O Structure* section in the *MAX II Architecture* chapter in the *MAX II Device Handbook*
- *Hot Socketing and Power-On Reset in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Operating Requirements for Altera Devices Data Sheet*
- *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*
- *Understanding and Evaluating Power in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Understanding Timing in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Using MAX II Devices in Multi-Voltage Systems* chapter in the *MAX II Device Handbook*