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Understanding <u>Embedded - CPLDs (Complex</u> <u>Programmable Logic Devices)</u>

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixedfunction ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.4 ns
Voltage Supply - Internal	2.5V, 3.3V
Number of Logic Elements/Blocks	570
Number of Macrocells	440
Number of Gates	-
Number of I/O	76
Operating Temperature	0°C ~ 85°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm570t100c5n

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Table 1–1 shows the MAX II family features.

Feature	EPM240 EPM240G	EPM570 EPM570G	EPM1270 EPM1270G	EPM2210 EPM2210G	EPM240Z	EPM570Z
LEs	240	570	1,270	2,210	240	570
Typical Equivalent Macrocells	192	440	980	1,700	192	440
Equivalent Macrocell Range	128 to 240	240 to 570	570 to 1,270	1,270 to 2,210	128 to 240	240 to 570
UFM Size (bits)	8,192	8,192	8,192	8,192	8,192	8,192
Maximum User I/O pins	80	160	212	272	80	160
t _{PD1} (ns) (1)	4.7	5.4	6.2	7.0	7.5	9.0
f _{cnt} (MHz) <i>(2)</i>	304	304	304	304	152	152
t _{su} (ns)	1.7	1.2	1.2	1.2	2.3	2.2
t _{co} (ns)	4.3	4.5	4.6	4.6	6.5	6.7

Table 1–1. MAX II Family Features

Notes to Table 1-1:

(1) t_{PD1} represents a pin-to-pin delay for the worst case I/O placement with a full diagonal path across the device and combinational logic implemented in a single LUT and LAB that is adjacent to the output pin.

(2) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay will run faster than this number.

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For more information about equivalent macrocells, refer to the *MAX II Logic Element to Macrocell Conversion Methodology* white paper.

MAX II and MAX IIG devices are available in three speed grades: -3, -4, and -5, with -3 being the fastest. Similarly, MAX IIZ devices are available in three speed grades: -6, -7, and -8, with -6 being the fastest. These speed grades represent the overall relative performance, not any specific timing parameter. For propagation delay timing numbers within each speed grade and density, refer to the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*.

Table 1–2 shows MAX II device speed-grade offerings.

	Speed Grade						
Device	-3	-4	-5	-6	-7	-8	
EPM240	\checkmark	\checkmark	\checkmark		—	—	
EPM240G							
EPM570	\checkmark	\checkmark	~	_	_	—	
EPM570G							
EPM1270	\checkmark	\checkmark	~	_	_	_	
EPM1270G							
EPM2210	\checkmark	\checkmark	~	_	_	—	
EPM2210G							
EPM240Z	_	—	—	\checkmark	\checkmark	\checkmark	
EPM570Z			_	\checkmark	\checkmark	\checkmark	

 Table 1–2.
 MAX II Speed Grades

Table 1–6. Document Revision History

Date and Revision	Changes Made	Summary of Changes
June 2005, version 1.3	Updated timing numbers in Table 1-1.	_
December 2004, version 1.2	Updated timing numbers in Table 1-1.	_
June 2004, version 1.1	Updated timing numbers in Table 1-1.	_

Figure 2-4. DirectLink Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, a synchronous clear, an asynchronous preset/load, a synchronous load, and add/subtract control signals, providing a maximum of 10 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the labclk1 signal also uses labclkena1. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. Deasserting the clock enable signal turns off the LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. By default, the Quartus II software uses a NOT gate push-back technique to achieve preset. If you disable the NOT gate push-back option or assign a given register to power-up high using the Quartus II software, the preset is then achieved using the asynchronous load signal with asynchronous load data input tied high.

With the LAB-wide addnsub control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB column clocks [3..0], driven by the global clock network, and LAB local interconnect generate the LAB-wide control signals. The MultiTrack interconnect structure drives the LAB local interconnect for non-global control signal generation. The MultiTrack interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 2–5 shows the LAB control signal generation circuit.



Figure 2–5. LAB-Wide Control Signals

Logic Elements

The smallest unit of logic in the MAX II architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry-select capability. A single LE also supports dynamic single-bit addition or subtraction mode selectable by an LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and DirectLink interconnects. See Figure 2–6.

Normal Mode

The normal mode is suitable for general logic applications and combinational functions. In normal mode, four data inputs from the LAB local interconnect are inputs to a four-input LUT (see Figure 2–7). The Quartus II Compiler automatically selects the carry-in or the data3 signal as one of the inputs to the LUT. Each LE can use LUT chain connections to drive its combinational output directly to the next LE in the LAB. Asynchronous load data for the register comes from the data3 input of the LE. LEs in normal mode support packed registers.





Note to Figure 2-7:

(1) This signal is only allowed in normal mode if the LE is at the end of an adder/subtractor chain.

Dynamic Arithmetic Mode

The dynamic arithmetic mode is ideal for implementing adders, counters, accumulators, wide parity functions, and comparators. An LE in dynamic arithmetic mode uses four 2-input LUTs configurable as a dynamic adder/subtractor. The first two 2-input LUTs compute two summations based on a possible carry-in of 1 or 0; the other two LUTs generate carry outputs for the two chains of the carry-select circuitry. As shown in Figure 2–8, the LAB carry-in signal selects either the carry-in0 or carry-in1 chain. The selected chain's logic level in turn determines which parallel sum is generated as a combinational or registered output. For example, when implementing an adder, the sum output is the selection of two possible calculated sums:

```
data1 + data2 + carry in0
or
data1 + data2 + carry-in1
```

The speed advantage of the carry-select chain is in the parallel precomputation of carry chains. Since the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delays between LAB carry-in generation (LE 5 and LE 10) are now part of the critical path. This feature allows the MAX II architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

Figure 2–9 shows the carry-select circuitry in an LAB for a 10-bit full adder. One portion of the LUT generates the sum of two bits using the input signals and the appropriate carry-in bit; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT generates carry-out bits. An LAB-wide carry-in bit selects which chain is used for the addition of given inputs. The carry-in signal for each chain, carry-in0 or carry-in1, selects the carry-out to carry forward to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is fed to local, row, or column interconnects.





functions from LE 1 to LE 10 in the same LAB. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–11 shows the LUT chain and register chain interconnects.





The C4 interconnects span four LABs up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–12 shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by column and row IOEs. For LAB interconnection, a primary LAB or its vertical LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column to-column connections.

Figure 2–12. C4 Interconnect Connections (Note 1)



(1) Each C4 interconnect can drive either up or down four rows.





Note to Figure 2-13:

(1) Any I/O pin can use a MultiTrack interconnect to route as a logic array-generated global clock signal.

The global clock network drives to individual LAB column signals, LAB column clocks [3..0], that span an entire LAB column from the top to the bottom of the device. Unused global clocks or control signals in a LAB column are turned off at the LAB column clock buffers shown in Figure 2–14. The LAB column clocks [3..0] are multiplexed down to two LAB clock signals and one LAB clear signal. Other control signal types route from the global clock network into the LAB local interconnect. See "LAB Control Signals" on page 2–5 for more information.

Internal Oscillator

As shown in Figure 2–15, the dedicated circuitry within the UFM block contains an oscillator. The dedicated circuitry uses this internally for its read and program operations. This oscillator's divide by 4 output can drive out of the UFM block as a logic interface clock source or for general-purpose logic clocking. The typical OSC output signal frequency ranges from 3.3 to 5.5 MHz, and its exact frequency of operation is not programmable.

Program, Erase, and Busy Signals

The UFM block's dedicated circuitry automatically generates the necessary internal program and erase algorithm once the PROGRAM or ERASE input signals have been asserted. The PROGRAM or ERASE signal must be asserted until the busy signal deasserts, indicating the UFM internal program or erase operation has completed. The UFM block also supports JTAG as the interface for programming and/or reading.



For more information about programming and erasing the UFM block, refer to the *Using User Flash Memory in MAX II Devices* chapter in the *MAX II Device Handbook*.

Auto-Increment Addressing

The UFM block supports standard read or stream read operations. The stream read is supported with an auto-increment address feature. Deasserting the ARSHIFT signal while clocking the ARCLK signal increments the address register value to read consecutive locations from the UFM array.

Serial Interface

The UFM block supports a serial interface with serial address and data signals. The internal shift registers within the UFM block for address and data are 9 bits and 16 bits wide, respectively. The Quartus II software automatically generates interface logic in LEs for a parallel address and data interface to the UFM block. Other standard protocol interfaces such as SPI are also automatically generated in LE logic by the Quartus II software.

• For more information about the UFM interface signals and the Quartus II LE-based alternate interfaces, refer to the *Using User Flash Memory in MAX II Devices* chapter in the *MAX II Device Handbook*.

UFM Block to Logic Array Interface

The UFM block is a small partition of the flash memory that contains the CFM block, as shown in Figure 2–1 and Figure 2–2. The UFM block for the EPM240 device is located on the left side of the device adjacent to the left most LAB column. The UFM block for the EPM570, EPM1270, and EPM2210 devices is located at the bottom left of the device. The UFM input and output signals interface to all types of interconnects (R4 interconnect, C4 interconnect, and DirectLink interconnect to/from adjacent LAB rows). The UFM signals can also be driven from global clocks, GCLK[3..0]. The interface region for the EPM240 device is shown in Figure 2–16. The interface regions for EPM570, EPM1270, and EPM2210 devices are shown in Figure 2–17.

Device	33-MHz PCI	66-MHz PCI
EPM1270	All Speed Grades	–3 Speed Grade
EPM2210	All Speed Grades	–3 Speed Grade

Table 2–5. MAX II Devices and Speed Grades that Support 3.3-V PCI Electrical Specifications and

 Meet PCI Timing

Schmitt Trigger

The input buffer for each MAX II device I/O pin has an optional Schmitt trigger setting for the 3.3-V and 2.5-V standards. The Schmitt trigger allows input buffers to respond to slow input edge rates with a fast output edge rate. Most importantly, Schmitt triggers provide hysteresis on the input buffer, preventing slow-rising noisy input signals from ringing or oscillating on the input signal driven into the logic array. This provides system noise tolerance on MAX II inputs, but adds a small, nominal input delay.

The JTAG input pins (TMS, TCK, and TDI) have Schmitt trigger buffers that are always enabled.

The TCK input is susceptible to high pulse glitches when the input signal fall time is greater than 200 ns for all I/O standards.

Output Enable Signals

Each MAX II IOE output buffer supports output enable signals for tri-state control. The output enable signal can originate from the GCLK[3..0] global signals or from the MultiTrack interconnect. The MultiTrack interconnect routes output enable signals and allows for a unique output enable for each output or bidirectional pin.

MAX II devices also provide a chip-wide output enable pin (DEV_OE) to control the output enable for every output pin in the design. An option set before compilation in the Quartus II software controls this pin. This chip-wide output enable uses its own routing resources and does not use any of the four global resources. If this option is turned on, all outputs on the chip operate normally when DEV_OE is asserted. When the pin is deasserted, all outputs are tri-stated. If this option is turned off, the DEV_OE pin is disabled when the device operates in user mode and is available as a user I/O pin.

Programmable Drive Strength

The output buffer for each MAX II device I/O pin has two levels of programmable drive strength control for each of the LVTTL and LVCMOS I/O standards. Programmable drive strength provides system noise reduction control for high performance I/O designs. Although a separate slew-rate control feature exists, using the lower drive strength setting provides signal slew-rate control to reduce system noise and signal overshoot without the large delay adder associated with the slew-rate control feature. Table 2–6 shows the possible settings for the I/O standards with drive strength control. The Quartus II software uses the maximum current strength as the default setting. The PCI I/O standard is always set at 20 mA with no alternate setting.

|--|

JTAG Instruction	Instruction Code	Description
Clamp (1)	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the boundary scan test data to pass synchronously through selected devices to adjacent devices during normal device operation, while holding I/O pins to a state defined by the data in the boundary-scan register.
USER0	00 0000 1100	This instruction allows you to define the scan chain between TDI and TDO in the MAX II logic array. This instruction is also used for custom logic and JTAG interfaces.
USER1	00 0000 1110	This instruction allows you to define the scan chain between TDI and TDO in the MAX II logic array. This instruction is also used for custom logic and JTAG interfaces.
IEEE 1532 instructions	(2)	IEEE 1532 ISC instructions used when programming a MAX II device via the JTAG port.

Notes to Table 3-1:

(1) HIGHZ, CLAMP, and EXTEST instructions do not disable weak pull-up resistors or bus hold features.

(2) These instructions are shown in the 1532 BSDL files, which will be posted on the Altera® website at www.altera.com when they are available.



Unsupported JTAG instructions should not be issued to the MAX II device as this may put the device into an unknown state, requiring a power cycle to recover device operation.

The MAX II device instruction register length is 10 bits and the USERCODE register length is 32 bits. Table 3–2 and Table 3–3 show the boundary-scan register length and device IDCODE information for MAX II devices.

Table 3–2. MAX II Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM240	240
EPM570	480
EPM1270	636
EPM2210	816

Table 3-3. 32-Bit MAX II Device IDCODE (Part 1 of 2)

Device	Version (4 Bits)	Part Number	Manufacturer Identity (11 Bits)	LSB (1 Bit) <i>(2)</i>	HEX IDCODE
EPM240	0000	0010 0000 1010 0001	000 0110 1110	1	0x020A10DD
EPM240G					
EPM570	0000	0010 0000 1010 0010	000 0110 1110	1	0x020A20DD
EPM570G					
EPM1270	0000	0010 0000 1010 0011	000 0110 1110	1	0x020A30DD
EPM1270G					
EPM2210	0000	0010 0000 1010 0100	000 0110 1110	1	0x020A40DD
EPM2210G					

Table 3–4 shows the programming times for MAX II devices using in-circuit testers to execute the algorithm vectors in hardware. Software-based programming tools used with download cables are slightly slower because of data processing and transfer limitations.

Description	EPM240 EPM240G EPM240Z	EPM570 EPM570G EPM570Z	EPM1270 EPM1270G	EPM2210 EPM2210G	Unit
Erase + Program (1 MHz)	1.72	2.16	2.90	3.92	sec
Erase + Program (10 MHz)	1.65	1.99	2.58	3.40	sec
Verify (1 MHz)	0.09	0.17	0.30	0.49	sec
Verify (10 MHz)	0.01	0.02	0.03	0.05	sec
Complete Program Cycle (1 MHz)	1.81	2.33	3.20	4.41	sec
Complete Program Cycle (10 MHz)	1.66	2.01	2.61	3.45	sec

Table 3-4. MAX II Device Family Programming Times

UFM Programming

The Quartus II software, with the use of POF, Jam, or JBC files, supports programming of the user flash memory (UFM) block independent of the logic array design pattern stored in the CFM block. This allows updating or reading UFM contents through ISP without altering the current logic array design, or vice versa. By default, these programming files and methods will program the entire flash memory contents, which includes the CFM block and UFM contents. The stand-alone embedded Jam STAPL player and Jam Byte-Code Player provides action commands for programming or reading the entire flash memory (UFM and CFM together) or each independently.



For more information, refer to the *Using Jam STAPL for ISP via an Embedded Processor* chapter in the *MAX II Device Handbook*.

In-System Programming Clamp

By default, the IEEE 1532 instruction used for entering ISP automatically tri-states all I/O pins with weak pull-up resistors for the duration of the ISP sequence. However, some systems may require certain pins on MAX II devices to maintain a specific DC logic level during an in-field update. For these systems, an optional in-system programming clamp instruction exists in MAX II circuitry to control I/O behavior during the ISP sequence. The in-system programming clamp instruction enables the device to sample and sustain the value on an output pin (an input pin would remain tri-stated if sampled) or to explicitly set a logic high, logic low, or tri-state value on any pin. Setting these options is controlled on an individual pin basis using the Quartus II software.

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• For more information, refer to the *Real-Time ISP and ISP Clamp for MAX II Devices* chapter in the *MAX II Device Handbook*.

Real-Time ISP

For systems that require more than DC logic level control of I/O pins, the real-time ISP feature allows you to update the CFM block with a new design image while the current design continues to operate in the SRAM logic array and I/O pins. A new programming file is updated into the MAX II device without halting the original design's operation, saving down-time costs for remote or field upgrades. The updated CFM block configures the new design into the SRAM upon the next power cycle. It is also possible to execute an immediate configuration of the SRAM without a power cycle by using a specific sequence of ISP commands. The configuration of SRAM without a power cycle takes a specific amount of time (t_{CONFIG}). During this time, the I/O pins are tri-stated and weakly pulled-up to V_{CCID} .

Design Security

All MAX II devices contain a programmable security bit that controls access to the data programmed into the CFM block. When this bit is programmed, design programming information, stored in the CFM block, cannot be copied or retrieved. This feature provides a high level of design security because programmed data within flash memory cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is erased. The SRAM is also invisible and cannot be accessed regardless of the security bit setting. The UFM block data is not protected by the security bit and is accessible through JTAG or logic array connections.

Programming with External Hardware

MAX II devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera® ByteblasterMVTM, MasterBlasterTM, ByteBlasterTM II, and USB-Blaster cables.

BP Microsystems, System General, and other programming hardware manufacturers provide programming support for Altera devices. Check their websites for device support information.

Referenced Documents

This chapter references the following documents:

- DC and Switching Characteristics chapter in the MAX II Device Handbook
- IEEE 1149.1 (JTAG) Boundary-Scan Testing for MAX II Devices chapter in the MAX II Device Handbook
- Real-Time ISP and ISP Clamp for MAX II Devices chapter in the MAX II Device Handbook
- Using Jam STAPL for ISP via an Embedded Processor chapter in the MAX II Device Handbook

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I _{PULLUP}	I/O pin pull-up resistor current when I/O is unprogrammed	_	_	_	300	μA
C ₁₀	Input capacitance for user I/O pin	_			8	pF
C _{GCLK}	Input capacitance for dual-purpose GCLK/user I/O pin	_			8	pF

 Table 5-4.
 MAX II Device DC Electrical Characteristics (Note 1) (Part 2 of 2)

Notes to Table 5-4:

- (1) Typical values are for $T_A = 25^{\circ}$ C, $V_{CCINT} = 3.3$ or 2.5 V, and $V_{CCIO} = 1.5$ V, 1.8 V, 2.5 V, or 3.3 V.
- (2) This value is specified for normal device operation. The value may vary during power-up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).
- (3) V_1 = ground, no load, no toggling inputs.
- (4) Commercial temperature ranges from 0°C to 85°C with maximum current at 85°C.
- (5) Industrial temperature ranges from -40°C to 100°C with maximum current at 100°C.
- (6) This value applies to commercial and industrial range devices. For extended temperature range devices, the V_{SCHMITT} typical value is 300 mV for V_{CCI0} = 3.3 V and 120 mV for V_{CCI0} = 2.5 V.
- (7) The TCK input is susceptible to high pulse glitches when the input signal fall time is greater than 200 ns for all I/O standards.
- (8) This is a peak current value with a maximum duration of t_{CONFIG} time.
- (9) Pin pull-up resistance values will lower if an external source drives the pin higher than V_{CCIO}.

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{OH}	High-level output voltage	$V_{ccio} = 3.0,$ IOH = -0.1 mA (1)	$V_{\text{ccio}} - 0.2$	—	V
V _{OL}	Low-level output voltage	V _{ccio} = 3.0, IOL = 0.1 mA <i>(1)</i>	_	0.2	V

Table 5-6. 3.3-V LVCMOS Specifications (Part 2 of 2)

Table 5-7. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{CCIO}	I/O supply voltage	—	2.375	2.625	V
VIH	High-level input voltage	—	1.7	4.0	V
VIL	Low-level input voltage		-0.5	0.7	V
V _{OH}	High-level output voltage	IOH = -0.1 mA (1)	2.1		V
		IOH = -1 mA (1)	2.0		V
		IOH = -2 mA (1)	1.7		V
V _{ol}	Low-level output voltage	IOL = 0.1 mA (1)		0.2	V
		IOL = 1 mA (1)		0.4	V
		IOL = 2 mA (1)	_	0.7	V

Table 5-8. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
Vccio	I/O supply voltage	—	1.71	1.89	V
V _{IH}	High-level input voltage		$0.65 \times V_{\text{CCIO}}$	2.25 <i>(2)</i>	V
VIL	Low-level input voltage		-0.3	$0.35 \times V_{ccio}$	V
V _{OH}	High-level output voltage	IOH = -2 mA (1)	$V_{\text{ccio}} - 0.45$		V
V _{OL}	Low-level output voltage	IOL = 2 mA (1)		0.45	V

Table 5-9. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{ccio}	I/O supply voltage	_	1.425	1.575	V
VIH	High-level input voltage	_	$0.65 \times V_{ccio}$	V _{ccio} + 0.3 <i>(2)</i>	V
VIL	Low-level input voltage	—	-0.3	$0.35 \times V_{ccio}$	V
V _{OH}	High-level output voltage	IOH = -2 mA (1)	$0.75 \times V_{ccio}$		V
Vol	Low-level output voltage	IOL = 2 mA (1)		$0.25 \times V_{ccio}$	V

Notes to Table 5–5 through Table 5–9:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the MAX II Architecture chapter (I/O Structure section) in the MAX II Device Handbook.

(2) This maximum V_{IH} reflects the JEDEC specification. The MAX II input buffer can tolerate a V_{IH} maximum of 4.0, as specified by the V_{I} parameter in Table 5–2.

Power-Up Timing

Table 5–12 shows the power-up timing characteristics for MAX II devices.

Table 5-12. MAX II Power-Up Timing

Symbol	Parameter	Device	Min	Тур	Max	Unit
t _{config} (1)	The amount of time from when	EPM240	_	_	200	μs
	the device enters user mode (2)	EPM570	_	_	300	μs
		EPM1270	_	_	300	μs
		EPM2210			450	μs

Notes to Table 5-12:

(1) Table 5–12 values apply to commercial and industrial range devices. For extended temperature range devices, the t_{CONFIG} maximum values are as follows:
 Device Maximum

Device	Maximu
EPM240	300 µs
EPM570	400 µs
EPM1270	400 µs
EPM2210	500 us

(2) For more information about POR trigger voltage, refer to the *Hot Socketing and Power-On Reset in MAX II Devices* chapter in the *MAX II Device Handbook*.

Power Consumption

Designers can use the Altera[®] PowerPlay Early Power Estimator and PowerPlay Power Analyzer to estimate the device power.



Timing Model and Specifications

MAX II devices timing can be analyzed with the Altera Quartus[®] II software, a variety of popular industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 5–2.

MAX II devices have predictable internal delays that enable the designer to determine the worst-case timing of any design. The software provides timing simulation, point-to-point delay prediction, and detailed timing analysis for device-wide performance evaluation.

Device	Preliminary	Final
EPM1270	—	\checkmark
EPM2210		\checkmark

Table 5–13.	MAX II Device	Timing Model Status	(Part 2 of 2))
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Note to Table 5-13:

(1) The MAX IIZ device timing models are only available in the Quartus II software version 8.0 and later.

Performance

Table 5–14 shows the MAX II device performance for some common designs. All performance values were obtained with the Quartus II software compilation of megafunctions. Performance values for –3, –4, and –5 speed grades are based on an EPM1270 device target, while –6, –7, and –8 speed grades are based on an EPM570Z device target.

Table 5–14. MAX II Device Performance

		Performance									
		Resources Used		MAX II / MAX IIG			MAX IIZ				
Resource Used	Design Size and Function	Mode	LEs	UFM Blocks	–3 Speed Grade	–4 Speed Grade	–5 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	Unit
LE	16-bit counter (1)		16	0	304.0	247.5	201.1	184.1	123.5	118.3	MHz
	64-bit counter (1)		64	0	201.5	154.8	125.8	83.2	83.2	80.5	MHz
	16-to-1 multiplexer	—	11	0	6.0	8.0	9.3	17.4	17.3	20.4	ns
	32-to-1 multiplexer	_	24	0	7.1	9.0	11.4	12.5	22.8	25.3	ns
	16-bit XOR function	—	5	0	5.1	6.6	8.2	9.0	15.0	16.1	ns
	16-bit decoder with single address line		5	0	5.2	6.6	8.2	9.2	15.0	16.1	ns
UFM	512 × 16	None	3	1	10.0	10.0	10.0	10.0	10.0	10.0	MHz
	512 × 16	SPI (2)	37	1	8.0	8.0	8.0	9.7	9.7	9.7	MHz
	512 × 8	Parallel (3)	73	1	(4)	(4)	(4)	(4)	(4)	(4)	MHz
	512 × 16	I ² C <i>(3)</i>	142	1	100 <i>(5)</i>	100 <i>(5)</i>	100 <i>(5)</i>	100 <i>(5)</i>	100 <i>(5)</i>	100 <i>(5)</i>	kHz

Notes to Table 5-14:

(1) This design is a binary loadable up counter.

(2) This design is configured for read-only operation in Extended mode. Read and write ability increases the number of LEs used.

(3) This design is configured for read-only operation. Read and write ability increases the number of LEs used.

(4) This design is asynchronous.

(5) The I²C megafunction is verified in hardware up to 100-kHz serial clock line (SCL) rate.

Referenced Documents

This chapter references the following document:

Package Information chapter in the MAX II Device Handbook

Document Revision History

Table 6–1 shows the revision history for this chapter.

Table 6–1.	Document Revision History
	Document nevision mistory

Date and Revision	Changes Made	Summary of Changes
August 2009, version 1.6	Updated Figure 6–1.	Added information for speed grade –8
October 2008, version 1.5	 Updated New Document Format. 	_
December 2007, version 1.4	 Added "Referenced Documents" section. Updated Figure 6–1. 	Updated document with MAX IIZ information.
December 2006, version 1.3	 Added document revision history. 	_
October 2006, version 1.2	 Updated Figure 6-1. 	_
June 2005, version 1.1	 Removed Dual Marking section. 	_