Intel - EPM570T144C3N Datasheet





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Understanding <u>Embedded - CPLDs (Complex</u> <u>Programmable Logic Devices)</u>

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixedfunction ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details

Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	5.4 ns
Voltage Supply - Internal	2.5V, 3.3V
Number of Logic Elements/Blocks	570
Number of Macrocells	440
Number of Gates	-
Number of I/O	116
Operating Temperature	0°C ~ 85°C (TJ)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm570t144c3n

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

MAX II devices are available in space-saving FineLine BGA, Micro FineLine BGA, and thin quad flat pack (TQFP) packages (refer to Table 1–3 and Table 1–4). MAX II devices support vertical migration within the same package (for example, you can migrate between the EPM570, EPM1270, and EPM2210 devices in the 256-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins and JTAG pins are the same and power pins are subsets or supersets for a given package across device densities. The largest density in any package has the highest number of power pins; you must lay out for the largest planned density in a package to provide the necessary power pins for migration. For I/O pin migration across densities, cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins can be migrated. The Quartus® II software can automatically cross-reference and place all pins for you when given a device migration list.

 Table 1–3.
 MAX II Packages and User I/O Pins

Device	68-Pin Micro FineLine BGA <i>(1)</i>	100-Pin Micro FineLine BGA <i>(1)</i>	100-Pin FineLine BGA	100-Pin TQFP	144-Pin TQFP	144-Pin Micro FineLine BGA <i>(1)</i>	256-Pin Micro FineLine BGA <i>(1)</i>	256-Pin FineLine BGA	324-Pin FineLine BGA
EPM240	—	80	80	80	—	_	_	—	_
EPM240G									
EPM570	—	76	76	76	116	_	160	160	
EPM570G									
EPM1270	—	_	—	—	116	_	212	212	_
EPM1270G									
EPM2210	—	—	—	—	—	—	—	204	272
EPM2210G									
EPM240Z	54	80	_	_	—	_	_	—	
EPM570Z	—	76	—	_	—	116	160	_	_

Note to Table 1-3:

(1) Packages available in lead-free versions only.

Table 1-4. MAX II TQFP, FineLine BGA, and Micro FineLine BGA Package Sizes

Package	68-Pin Micro FineLine BGA	100-Pin Micro FineLine BGA	100-Pin FineLine BGA	100-Pin TQFP	144-Pin TQFP	144-Pin Micro FineLine BGA	256-Pin Micro FineLine BGA	256-Pin FineLine BGA	324-Pin FineLine BGA
Pitch (mm)	0.5	0.5	1	0.5	0.5	0.5	0.5	1	1
Area (mm2)	25	36	121	256	484	49	121	289	361
Length × width (mm × mm)	5 × 5	6 × 6	11 × 11	16 × 16	22 × 22	7×7	11 × 11	17 × 17	19 × 19

Figure 2-4. DirectLink Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, a synchronous clear, an asynchronous preset/load, a synchronous load, and add/subtract control signals, providing a maximum of 10 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the labclk1 signal also uses labclkena1. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. Deasserting the clock enable signal turns off the LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. By default, the Quartus II software uses a NOT gate push-back technique to achieve preset. If you disable the NOT gate push-back option or assign a given register to power-up high using the Quartus II software, the preset is then achieved using the asynchronous load signal with asynchronous load data input tied high.

With the LAB-wide addnsub control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB column clocks [3..0], driven by the global clock network, and LAB local interconnect generate the LAB-wide control signals. The MultiTrack interconnect structure drives the LAB local interconnect for non-global control signal generation. The MultiTrack interconnect's inherent low skew allows clock and control signal distribution in addition to data. Figure 2–5 shows the LAB control signal generation circuit.

Figure 2-6. MAX II LE



Each LE's programmable register can be configured for D, T, JK, or SR operation. Each register has data, true asynchronous load data, clock, clock enable, clear, and asynchronous load/preset inputs. Global signals, general-purpose I/O pins, or any LE can drive the register's clock and clear control signals. Either general-purpose I/O pins or LEs can drive the clock enable, preset, asynchronous load, and asynchronous data. The asynchronous load data input comes from the data3 input of the LE. For combinational functions, the LUT output bypasses the register and drives directly to the LE outputs.

Each LE has three outputs that drive the local, row, and column routing resources. The LUT or register output can drive these three outputs independently. Two LE outputs drive column or row and DirectLink routing connections and one drives local interconnect resources. This allows the LUT to drive one output while the register drives another output. This register packing feature improves device utilization because the device can use the register and the LUT for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same LE so that the register is packed with its own fan-out LUT. This provides another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

The speed advantage of the carry-select chain is in the parallel precomputation of carry chains. Since the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delays between LAB carry-in generation (LE 5 and LE 10) are now part of the critical path. This feature allows the MAX II architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

Figure 2–9 shows the carry-select circuitry in an LAB for a 10-bit full adder. One portion of the LUT generates the sum of two bits using the input signals and the appropriate carry-in bit; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT generates carry-out bits. An LAB-wide carry-in bit selects which chain is used for the addition of given inputs. The carry-in signal for each chain, carry-in0 or carry-in1, selects the carry-out to carry forward to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is fed to local, row, or column interconnects.





The Quartus II software automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions. The Quartus II software creates carry chains longer than 10 LEs by linking adjacent LABs within the same row together automatically. A carry chain can extend horizontally up to one full LAB row, but does not extend between LAB rows.

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. MAX II devices support simultaneous preset/asynchronous load and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, MAX II devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals and uses its own dedicated routing resources (that is, it does not use any of the four global resources). Driving this signal low before or during power-up prevents user mode from releasing clears within the design. This allows you to control when clear is released on a device that has just been powered-up. If not set for its chip-wide reset function, the DEV_CLRn pin is a regular I/O pin.

By default, all registers in MAX II devices are set to power-up low. However, this power-up state can be set to high on individual registers during design entry using the Quartus II software.

MultiTrack Interconnect

In the MAX II architecture, connections between LEs, the UFM, and device I/O pins are provided by the MultiTrack interconnect structure. The MultiTrack interconnect consists of continuous, performance-optimized routing lines used for inter- and intradesign block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and short delays between logic levels instead of large delays associated with global or long routing lines. Dedicated row interconnects route signals to and from LABs within the same row. These row resources include:

- DirectLink interconnects between LABs
- R4 interconnects traversing four LABs to the right or left

The DirectLink interconnect allows an LAB to drive into the local interconnect of its left and right neighbors. The DirectLink interconnect provides fast communication between adjacent LABs and/or blocks without using row interconnect resources.

The UFM block communicates with the logic array similar to LAB-to-LAB interfaces. The UFM block connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. This block also has DirectLink interconnects for fast connections to and from a neighboring LAB. For more information about the UFM interface to the logic array, see "User Flash Memory Block" on page 2–18.

Table 2–2 shows the MAX II device routing scheme.

Table 2–2. MAX II Device Routing Scheme

		Destination									
Source	LUT Chain	Register Chain	Local (1)	DirectLink <i>(1)</i>	R4 <i>(1)</i>	C4 (1)	LE	UFM Block	Column IOE	Row IOE	Fast I/0 <i>(1)</i>
LUT Chain	-		-	—			~			—	
Register Chain	_	—	_	—			\checkmark	—		_	_
Local Interconnect	-		-	_		—	\checkmark	~	~	~	_
DirectLink Interconnect	_		\checkmark	_				_		_	_
R4 Interconnect	_	—	\checkmark	—	~	~	_	—		—	—
C4 Interconnect	-	—	\checkmark	—	\checkmark	~		—	_	—	—
LE	\checkmark	\checkmark	\checkmark	\checkmark	~	~		_	~	\checkmark	\checkmark
UFM Block	_	—	\checkmark	\checkmark	\checkmark	~		—	—	—	—
Column IOE	_	—	_	—	—	\checkmark	—	—	—	—	—
Row IOE	-	—	-	\checkmark	\checkmark	\checkmark	—	—	_	—	—

Note to Table 2-2:

(1) These categories are interconnects.

Global Signals

Each MAX II device has four dual-purpose dedicated clock pins (GCLK[3..0], two pins on the left side and two pins on the right side) that drive the global clock network for clocking, as shown in Figure 2–13. These four pins can also be used as general-purpose I/O if they are not used to drive the global clock network.

The four global clock lines in the global clock network drive throughout the entire device. The global clock network can provide clocks for all resources within the device including LEs, LAB local interconnect, IOEs, and the UFM block. The global clock lines can also be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, or protocol control signals such as TRDY and IRDY for PCI. Internal logic can drive the global clock network for internally-generated global clocks and control signals. Figure 2–13 shows the various sources that drive the global clock network.

Figure 2–19. MAX II IOE Structure



(1) Available in EPM1270 and EPM2210 devices only.

I/O Blocks

The IOEs are located in I/O blocks around the periphery of the MAX II device. There are up to seven IOEs per row I/O block (5 maximum in the EPM240 device) and up to four IOEs per column I/O block. Each column or row I/O block interfaces with its adjacent LAB and MultiTrack interconnect to distribute signals throughout the device. The row I/O blocks drive row, column, or DirectLink interconnects. The column I/O blocks drive column interconnects.

Table 2–4 describes the I/O standards supported by MAX II devices.

Table 2-4.	MAX II I/O	Standards
------------	------------	-----------

I/O Standard	Туре	Output Supply Voltage (VCCIO) (V)
3.3-V LVTTL/LVCMOS	Single-ended	3.3
2.5-V LVTTL/LVCMOS	Single-ended	2.5
1.8-V LVTTL/LVCMOS	Single-ended	1.8
1.5-V LVCMOS	Single-ended	1.5
3.3-V PCI (1)	Single-ended	3.3

Note to Table 2-4:

(1) The 3.3-V PCI compliant I/O is supported in Bank 3 of the EPM1270 and EPM2210 devices.

The EPM240 and EPM570 devices support two I/O banks, as shown in Figure 2–22. Each of these banks support all the LVTTL and LVCMOS standards shown in Table 2–4. PCI compliant I/O is not supported in these devices and banks.





Notes to Figure 2–22:

(1) Figure 2-22 is a top view of the silicon die.

(2) Figure 2-22 is a graphical representation only. Refer to the pin list and the Quartus II software for exact pin locations.

The EPM1270 and EPM2210 devices support four I/O banks, as shown in Figure 2–23. Each of these banks support all of the LVTTL and LVCMOS standards shown in Table 2–4. PCI compliant I/O is supported in Bank 3. Bank 3 supports the PCI clamping diode on inputs and PCI drive compliance on outputs. You must use Bank 3 for designs requiring PCI compliant I/O pins. The Quartus II software automatically places I/O pins in this bank if assigned with the PCI I/O standard.

Connect VCCIO pins to either a 1.5-V, 1.8 V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (that is, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems. Table 2–7 summarizes MAX II MultiVolt I/O support.

Table 2–7. MAX II MultiVolt I/O Support (Note 1)

			Input Signa	I		0	utput Sign	al		
VCCIO (V)	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	\checkmark	\checkmark	\checkmark	\checkmark	_	\checkmark	_	_	_	_
1.8	\checkmark	\checkmark	\checkmark	\checkmark	_	✓ (2)	\checkmark	_	_	_
2.5	_	_	\checkmark	\checkmark	_	✓ (3)	✓ (3)	\checkmark	_	_
3.3	—	_	✓ (4)	\checkmark	✓ (5)	✓ (6)	✓ (6)	√ (6)	\checkmark	✓ (7)

Notes to Table 2-7:

(1) To drive inputs higher than V_{CGIO} but less than 4.0 V including the overshoot, disable the I/O clamp diode. However, to drive 5.0-V inputs to the device, enable the I/O clamp diode to prevent V₁ from rising above 4.0 V.

- (2) When $V_{CCIO} = 1.8$ V, a MAX II device can drive a 1.5-V device with 1.8-V tolerant inputs.
- (3) When $V_{CCIO} = 2.5$ V, a MAX II device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.
- (4) When V_{CCI0} = 3.3 V and a 2.5-V input signal feeds an input pin, the VCCI0 supply current will be slightly larger than expected.
- (5) MAX II devices can be 5.0-V tolerant with the use of an external resistor and the internal I/O clamp diode on the EPM1270 and EPM2210 devices.
- (6) When $V_{CCIO} = 3.3$ V, a MAX II device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.
- (7) When V_{CCI0} = 3.3 V, a MAX II device can drive a device with 5.0-V TTL inputs but not 5.0-V CMOS inputs. In the case of 5.0-V CMOS, opendrain setting with internal I/O clamp diode (available only on EPM1270 and EPM2210 devices) and external resistor is required.



• For information about output pin source and sink current guidelines, refer to the *AN* 428: *MAX II CPLD Design Guidelines*.

Referenced Documents

This chapter referenced the following documents:

- AN 428: MAX II CPLD Design Guidelines
- DC and Switching Characteristics chapter in the MAX II Device Handbook
- *Hot Socketing and Power-On Reset in MAX II Devices* chapter in the *MAX II Device Handbook*
- Using User Flash Memory in MAX II Devices chapter in the MAX II Device Handbook

3. JTAG and In-System Programmability

Introduction

This chapter discusses how to use the IEEE Standard 1149.1 Boundary-Scan Test (BST) circuitry in MAX II devices and includes the following sections:

- "IEEE Std. 1149.1 (JTAG) Boundary-Scan Support" on page 3–1
- "In System Programmability" on page 3–4

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All MAX[®] II devices provide Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry that complies with the IEEE Std. 1149.1-2001 specification. JTAG boundary-scan testing can only be performed at any time after V_{CCINT} and all V_{CCIO} banks have been fully powered and a t_{CONFIG} amount of time has passed. MAX II devices can also use the JTAG port for in-system programming together with either the Quartus[®] II software or hardware using Programming Object Files (**.pof**), JamTM Standard Test and Programming Language (STAPL) Files (**.jam**), or Jam Byte-Code Files (**.jbc**).

The JTAG pins support 1.5-V, 1.8-V, 2.5-V, or 3.3-V I/O standards. The supported voltage level and standard are determined by the V_{cCIO} of the bank where it resides. The dedicated JTAG pins reside in Bank 1 of all MAX II devices.

MAX II devices support the JTAG instructions shown in Table 3–1.

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
extest (1)	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO. This register defaults to all 1's if not specified in the Quartus II software.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ (1)	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the boundary scan test data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.

Table 3–1. MAX II JTAG Instructions (Part 1 of 2)

Table 3–4 shows the programming times for MAX II devices using in-circuit testers to execute the algorithm vectors in hardware. Software-based programming tools used with download cables are slightly slower because of data processing and transfer limitations.

Description	EPM240 EPM240G EPM240Z	EPM570 EPM570G EPM570Z	EPM1270 EPM1270G	EPM2210 EPM2210G	Unit
Erase + Program (1 MHz)	1.72	2.16	2.90	3.92	sec
Erase + Program (10 MHz)	1.65	1.99	2.58	3.40	sec
Verify (1 MHz)	0.09	0.17	0.30	0.49	sec
Verify (10 MHz)	0.01	0.02	0.03	0.05	sec
Complete Program Cycle (1 MHz)	1.81	2.33	3.20	4.41	sec
Complete Program Cycle (10 MHz)	1.66	2.01	2.61	3.45	sec

Table 3-4. MAX II Device Family Programming Times

UFM Programming

The Quartus II software, with the use of POF, Jam, or JBC files, supports programming of the user flash memory (UFM) block independent of the logic array design pattern stored in the CFM block. This allows updating or reading UFM contents through ISP without altering the current logic array design, or vice versa. By default, these programming files and methods will program the entire flash memory contents, which includes the CFM block and UFM contents. The stand-alone embedded Jam STAPL player and Jam Byte-Code Player provides action commands for programming or reading the entire flash memory (UFM and CFM together) or each independently.

• For more information, refer to the Using Jam STAPL for ISP via an Embedded Processor chapter in the MAX II Device Handbook.

In-System Programming Clamp

By default, the IEEE 1532 instruction used for entering ISP automatically tri-states all I/O pins with weak pull-up resistors for the duration of the ISP sequence. However, some systems may require certain pins on MAX II devices to maintain a specific DC logic level during an in-field update. For these systems, an optional in-system programming clamp instruction exists in MAX II circuitry to control I/O behavior during the ISP sequence. The in-system programming clamp instruction enables the device to sample and sustain the value on an output pin (an input pin would remain tri-stated if sampled) or to explicitly set a logic high, logic low, or tri-state value on any pin. Setting these options is controlled on an individual pin basis using the Quartus II software.

For more information, refer to the *Real-Time ISP and ISP Clamp for MAX II Devices* chapter in the *MAX II Device Handbook*.

Real-Time ISP

For systems that require more than DC logic level control of I/O pins, the real-time ISP feature allows you to update the CFM block with a new design image while the current design continues to operate in the SRAM logic array and I/O pins. A new programming file is updated into the MAX II device without halting the original design's operation, saving down-time costs for remote or field upgrades. The updated CFM block configures the new design into the SRAM upon the next power cycle. It is also possible to execute an immediate configuration of the SRAM without a power cycle by using a specific sequence of ISP commands. The configuration of SRAM without a power cycle takes a specific amount of time (t_{CONFIG}). During this time, the I/O pins are tri-stated and weakly pulled-up to V_{CCID} .

Design Security

All MAX II devices contain a programmable security bit that controls access to the data programmed into the CFM block. When this bit is programmed, design programming information, stored in the CFM block, cannot be copied or retrieved. This feature provides a high level of design security because programmed data within flash memory cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is erased. The SRAM is also invisible and cannot be accessed regardless of the security bit setting. The UFM block data is not protected by the security bit and is accessible through JTAG or logic array connections.

Programming with External Hardware

MAX II devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera® ByteblasterMVTM, MasterBlasterTM, ByteBlasterTM II, and USB-Blaster cables.

BP Microsystems, System General, and other programming hardware manufacturers provide programming support for Altera devices. Check their websites for device support information.

Referenced Documents

This chapter references the following documents:

- DC and Switching Characteristics chapter in the MAX II Device Handbook
- IEEE 1149.1 (JTAG) Boundary-Scan Testing for MAX II Devices chapter in the MAX II Device Handbook
- Real-Time ISP and ISP Clamp for MAX II Devices chapter in the MAX II Device Handbook
- Using Jam STAPL for ISP via an Embedded Processor chapter in the MAX II Device Handbook

4. Hot Socketing and Power-On Reset in MAX II Devices

MII51004-2.1

Introduction

MAX[®] II devices offer hot socketing, also known as hot plug-in or hot swap, and power sequencing support. Designers can insert or remove a MAX II board in a system during operation without undesirable effects to the system bus. The hot socketing feature removes some of the difficulties designers face when using components on printed circuit boards (PCBs) that contain a mixture of 3.3-, 2.5-, 1.8-, and 1.5-V devices.

The MAX II device hot socketing feature provides:

- Board or device insertion and removal
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter contains the following sections:

- "MAX II Hot-Socketing Specifications" on page 4–1
- "Power-On Reset Circuitry" on page 4–5

MAX II Hot-Socketing Specifications

MAX II devices offer all three of the features required for the hot-socketing capability listed above without any external components or special design requirements. The following are hot-socketing specifications:

- The device can be driven before and during power-up or power-down without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.
- Signal pins do not drive the V_{CCIO} or V_{CCINT} power supplies. External input signals to device I/O pins do not power the device V_{CCIO} or V_{CCINT} power supplies via internal paths. This is true if the V_{CCINT} and the V_{CCIO} supplies are held at GND.

Devices Can Be Driven before Power-Up

Signals can be driven into the MAX II device I/O pins and GCLK[3..0] pins before or during power-up or power-down without damaging the device. MAX II devices support any power-up or power-down sequence (V_{CCIO1} , V_{CCIO2} , V_{CCIO3} , V_{CCIO4} , V_{CCINT}), simplifying the system-level design.





Notes to Figure 4–5:

(1) Time scale is relative.

(2) Figure 4–5 assumes all V_{CCIO} banks power up simultaneously with the V_{CCINT} profile shown. If not, t_{CONFIG} stretches out until all V_{CCIO} banks are powered.

After SRAM configuration, all registers in the device are cleared and released into user function before I/O tri-states are released. To release clears after tri-states are released, use the DEV_CLRn pin option. To hold the tri-states beyond the power-up configuration time, use the DEV_OE pin option.

Recommended Operating Conditions

Table 5–2 shows the MAX II device family recommended operating conditions.

Table 5-2. MAX II Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{CCINT} (1)	3.3-V supply voltage for internal logic and ISP	MAX II devices	3.00	3.60	V
	2.5-V supply voltage for internal logic and ISP	MAX II devices	2.375	2.625	V
	1.8-V supply voltage for internal logic and ISP	MAX IIG and MAX IIZ devices	1.71	1.89	V
V _{ccio} (1)	Supply voltage for I/O buffers, 3.3-V operation	_	3.00	3.60	V
	Supply voltage for I/O buffers, 2.5-V operation	_	2.375	2.625	V
	Supply voltage for I/O buffers, 1.8-V operation	_	1.71	1.89	V
	Supply voltage for I/O buffers, 1.5-V operation	_	1.425	1.575	V
V	Input voltage	(2), (3), (4)	-0.5	4.0	V
Vo	Output voltage	_	0	Vccio	V
TJ	Operating junction temperature	Commercial range	0	85	°C
		Industrial range	-40	100	°C
		Extended range (5)	-40	125	°C

Notes to Table 5-2:

(1) MAX II device in-system programming and/or user flash memory (UFM) programming via JTAG or logic array is not guaranteed outside the recommended operating conditions (for example, if brown-out occurs in the system during a potential write/program sequence to the UFM, users are recommended to read back UFM contents and verify against the intended write data).

(2) Minimum DC input is -0.5 V. During transitions, the inputs may undershoot to -2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

(3) During transitions, the inputs may overshoot to the voltages shown in the following table based upon input duty cycle. The DC case is equivalent to 100% duty cycle. For more information about 5.0-V tolerance, refer to the Using MAX II Devices in Multi-Voltage Systems chapter in the MAX II Device Handbook.

- V_ℕ 4.0 V Max. Duty Cycle
- 100% (DC)
- 4.1 90%
- 4.2 50%
- 4.3 30%
- 17% 4.4
- 4.5 10%

(4) All pins, including clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.

(5) For the extended temperature range of 100 to 125° C, MAX II UFM programming (erase/write) is only supported via the JTAG interface. UFM programming via the logic array interface is not guaranteed in this range.

5–6	

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{OH}	High-level output voltage	$V_{ccio} = 3.0,$ IOH = -0.1 mA (1)	$V_{\text{ccio}} - 0.2$	—	V
V _{OL}	Low-level output voltage	$V_{ccio} = 3.0,$ IOL = 0.1 mA (1)	_	0.2	V

Table 5-6. 3.3-V LVCMOS Specifications (Part 2 of 2)

Table 5-7. 2.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{CCIO}	I/O supply voltage	—	2.375	2.625	V
VIH	High-level input voltage	_	1.7	4.0	V
VIL	Low-level input voltage		-0.5	0.7	V
V _{OH}	High-level output voltage	IOH = -0.1 mA (1)	2.1		V
		IOH = -1 mA (1)	2.0	_	V
		IOH = -2 mA (1)	1.7	—	V
Vol	Low-level output voltage	IOL = 0.1 mA (1)		0.2	V
		IOL = 1 mA (1)		0.4	V
		IOL = 2 mA (1)		0.7	V

Table 5-8. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{ccio}	I/O supply voltage	—	1.71	1.89	V
V _{IH}	High-level input voltage		$0.65 \times V_{cc10}$	2.25 <i>(2)</i>	V
VIL	Low-level input voltage		-0.3	$0.35 \times V_{ccio}$	V
V _{OH}	High-level output voltage	IOH = -2 mA (1)	$V_{\text{ccio}} - 0.45$		V
VOL	Low-level output voltage	IOL = 2 mA (1)		0.45	V

Table 5-9. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V _{ccio}	I/O supply voltage	—	1.425	1.575	V
VIH	High-level input voltage		$0.65 \times V_{ccio}$	V _{CCI0} + 0.3 (2)	V
VIL	Low-level input voltage		-0.3	$0.35 \times V_{ccio}$	V
V _{OH}	High-level output voltage	IOH = -2 mA (1)	$0.75 \times V_{ccio}$		V
VOL	Low-level output voltage	IOL = 2 mA <i>(1)</i>	—	$0.25 \times V_{ccio}$	V

Notes to Table 5–5 through Table 5–9:

(1) This specification is supported across all the programmable drive strength settings available for this I/O standard, as shown in the MAX II Architecture chapter (I/O Structure section) in the MAX II Device Handbook.

(2) This maximum V_{IH} reflects the JEDEC specification. The MAX II input buffer can tolerate a V_{IH} maximum of 4.0, as specified by the V_{I} parameter in Table 5–2.

Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Table 5–15 through Table 5–22 describe the MAX II device internal timing microparameters for logic elements (LEs), input/output elements (IOEs), UFM blocks, and MultiTrack interconnects. The timing values for –3, –4, and –5 speed grades shown in Table 5–15 through Table 5–22 are based on an EPM1270 device target, while –6, –7, and –8 speed grade values are based on an EPM570Z device target.

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• For more explanations and descriptions about each internal timing microparameters symbol, refer to the *Understanding Timing in MAX II Devices* chapter in the *MAX II Device Handbook*.

Table 5–15. LE Internal Timing Microparameters

				MAX II	/ MAX I	IG		MAX IIZ						
		–3 S Gra	–3 Speed –4 S Grade G		peed –5 Sp ade Gra		Speed –6 Speed ade Grade		Speed rade	–7 \$ Gi	Speed rade	-8 S Gi	Speed ade	
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
t _{lut}	LE combinational LUT delay	_	571	-	742	_	914	-	1,215		2,247	_	2,247	ps
t _{сомв}	Combinational path delay	-	147	-	192	_	236	-	243	—	305	—	309	ps
t _{clr}	LE register clear delay	238	_	309	—	381	_	401	—	541	—	545		ps
t _{PRE}	LE register preset delay	238	_	309	—	381	_	401	—	541	—	545		ps
t _{su}	LE register setup time before clock	208	_	271	—	333	_	260	—	319	—	321		ps
t _H	LE register hold time after clock	0	-	0	_	0	_	0	_	0	_	0		ps
t _{co}	LE register clock- to-output delay	-	235	-	305	_	376	-	380	—	489	_	494	ps
t _{clkhl}	Minimum clock high or low time	166	-	216	—	266	_	253	—	335	-	339	_	ps
t _c	Register control delay	—	857	—	1,114	_	1,372	—	1,356		1,722	_	1,741	ps





Figure 5–5. UFM Erase Waveform



MAX II / MAX IIG								MAX IIZ							
	–3 S Gr	Speed rade	-4 S Gr	Speed 'ade	–5 S Gi	Speed –6 Speed rade Grade		–7 Speed Grade		–8 Speed Grade					
Routing	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit		
t _{c4}	—	429	—	556	—	687	—	(1)	—	(1)	—	(1)	ps		
t _{R4}	_	326	—	423	_	521	—	(1)	_	(1)	_	(1)	ps		
t _{local}	—	330	—	429	_	529	—	(1)	—	(1)		(1)	ps		

Table 5-22.	Routing	Delay	Internal	Timing	Microparameters
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Note to Table 5-22:

(1) The numbers will only be available in a later revision.

			MAX II / MAX IIG							MA	X IIZ			
		–3 Speed Grade		–4 S Gr	-4 Speed Grade		Speed rade	–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
I/O St	andard	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
3.3-V LVCMOS	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	_	0	ps
	With Schmitt Trigger	_	334	—	434	-	535	-	387	_	434	_	442	ps
2.5-V LVTTL / LVCMOS	Without Schmitt Trigger	—	23	—	30	-	37	-	42	—	43	-	43	ps
	With Schmitt Trigger	_	339	_	441	-	543	-	429	_	476	_	483	ps
1.8-V LVTTL / LVCMOS	Without Schmitt Trigger	_	291	—	378	-	466	—	378	_	373	_	373	ps
1.5-V LVCMOS	Without Schmitt Trigger	-	681	-	885	-	1,090	-	681	-	622	_	658	ps
3.3-V PCI	Without Schmitt Trigger	-	0	-	0	-	0	-	0	-	0	-	0	ps

Table 5–27. External Timing Input Delay Adders (Part 2 of 2)

Table 5-28. Ex	xternal Timing	Input Delay tours	Adders for	GCLK Pins
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		MAX II / MAX IIG			MAX IIZ									
		–3 Speed Grade		-4 S Gi	–4 Speed Grade		Speed rade	–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
I/0 St	andard	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
3.3-V LVTTL	Without Schmitt Trigger	—	0	—	0		0	—	0	—	0	—	0	ps
	With Schmitt Trigger	_	308	_	400	_	493	-	387	_	434	_	442	ps
3.3-V LVCMOS	Without Schmitt Trigger	_	0	_	0	_	0	-	0	_	0	_	0	ps
	With Schmitt Trigger	_	308	_	400	_	493	-	387	_	434	_	442	ps
2.5-V LVTTL / LVCMOS	Without Schmitt Trigger	_	21	_	27	_	33	-	42	_	43	_	43	ps
	With Schmitt Trigger	_	423	_	550		677	-	429	_	476	_	483	ps
1.8-V LVTTL / LVCMOS	Without Schmitt Trigger	-	353	—	459		565	-	378	_	373	_	373	ps
1.5-V LVCMOS	Without Schmitt Trigger	-	855	-	1,111		1,368	-	681	—	622	—	658	ps
3.3-V PCI	Without Schmitt Trigger	-	6	—	7		9	-	0	—	0	—	0	ps

Referenced Documents

This chapter references the following document:

■ *Package Information* chapter in the MAX II Device Handbook

Document Revision History

Table 6–1 shows the revision history for this chapter.

Date and Revision	Changes Made	Summary of Changes
August 2009, version 1.6	■ Updated Figure 6–1.	Added information for speed grade –8
October 2008, version 1.5	 Updated New Document Format. 	_
December 2007,	 Added "Referenced Documents" section. 	Updated document with
version 1.4	■ Updated Figure 6–1.	MAX IIZ information.
December 2006, version 1.3	 Added document revision history. 	_
October 2006, version 1.2	■ Updated Figure 6-1.	_
June 2005, version 1.1	 Removed Dual Marking section. 	

 Table 6–1.
 Document Revision History