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## Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

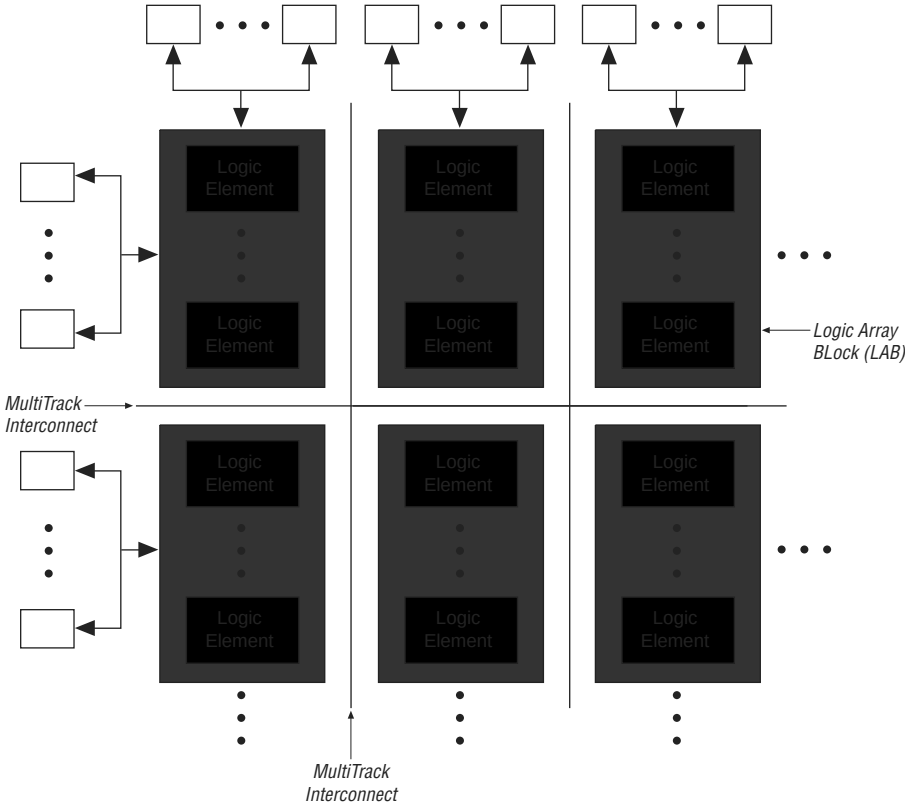
Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

## Applications of Embedded - CPLDs

| Details | |
|---|---|
| Product Status | Active |
| Programmable Type | In System Programmable |
| Delay Time tpd(1) Max | 5.4 ns |
| Voltage Supply - Internal | 2.5V, 3.3V |
| Number of Logic Elements/Blocks | 570 |
| Number of Macrocells | 440 |
| Number of Gates | - |
| Number of I/O | 116 |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/epm570t144i5n |

Figure 2–1 shows a functional block diagram of the MAX II device.

**Figure 2–1.** MAX II Device Block Diagram




Each MAX II device contains a flash memory block within its floorplan. On the EPM240 device, this block is located on the left side of the device. On the EPM570, EPM1270, and EPM2210 devices, the flash memory block is located on the bottom-left area of the device. The majority of this flash memory storage is partitioned as the dedicated configuration flash memory (CFM) block. The CFM block provides the non-volatile storage for all of the SRAM configuration information. The CFM automatically downloads and configures the logic and I/O at power-up, providing instant-on operation.

For more information about configuration upon power-up, refer to the *Hot Socketing and Power-On Reset in MAX II Devices* chapter in the *MAX II Device Handbook*.

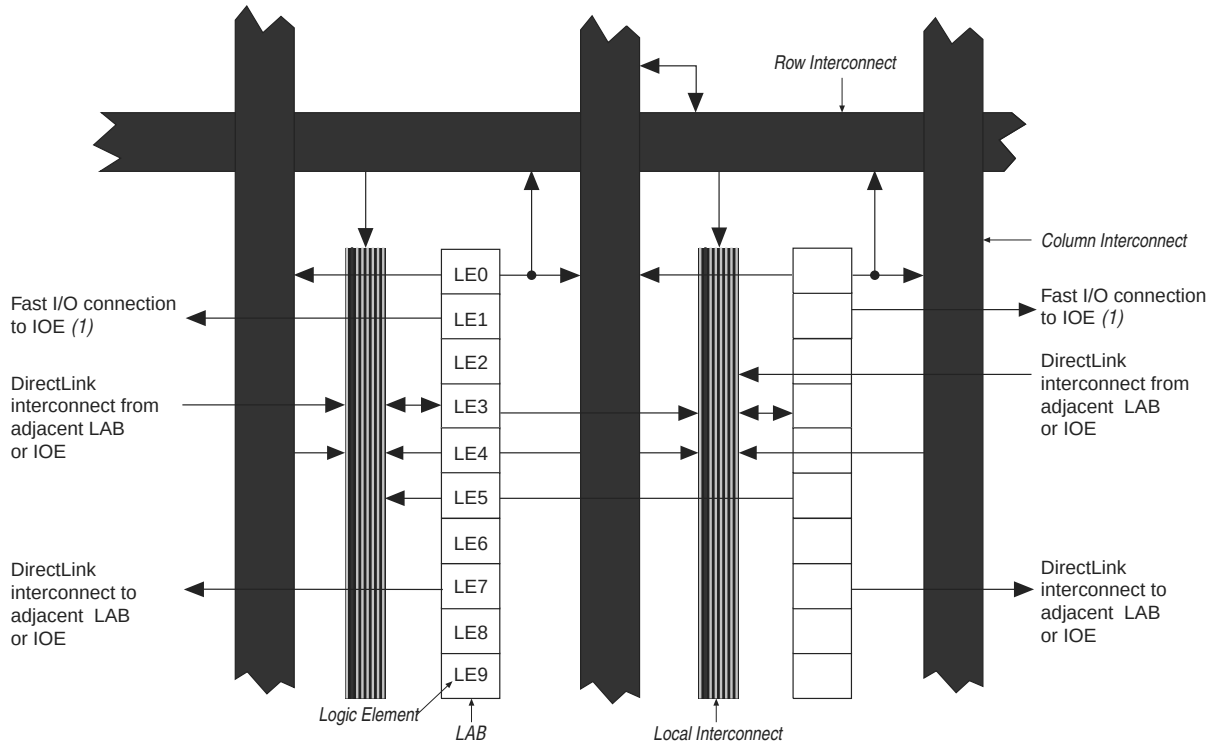
A portion of the flash memory within the MAX II device is partitioned into a small block for user data. This user flash memory (UFM) block provides 8,192 bits of general-purpose user storage. The UFM provides programmable port connections to the logic array for reading and writing. There are three LAB rows adjacent to this block, with column numbers varying by device.

Table 2–1 shows the number of LAB rows and columns in each device, as well as the number of LAB rows and columns adjacent to the flash memory area in the EPM570, EPM1270, and EPM2210 devices. The long LAB rows are full LAB rows that extend from one side of row I/O blocks to the other. The short LAB rows are adjacent to the UFM block; their length is shown as width in LAB columns.

# Logic Array Blocks

Each LAB consists of 10 LEs, LE carry chains, LAB control signals, a local interconnect, a look-up table (LUT) chain, and register chain connection lines. There are 26 possible unique inputs into an LAB, with an additional 10 local feedback input lines fed by LE outputs in the same LAB. The local interconnect transfers signals between LEs in the same LAB. LUT chain connections transfer the output of one LE's LUT to the adjacent LE for fast sequential LUT connections within the same LAB. Register chain connections transfer the output of one LE's register to the adjacent LE's register within an LAB. The Quartus® II software places associated logic within an LAB or adjacent LABs, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency. Figure 2–3 shows the MAX II LAB.

**Figure 2–3.** MAX II LAB Structure



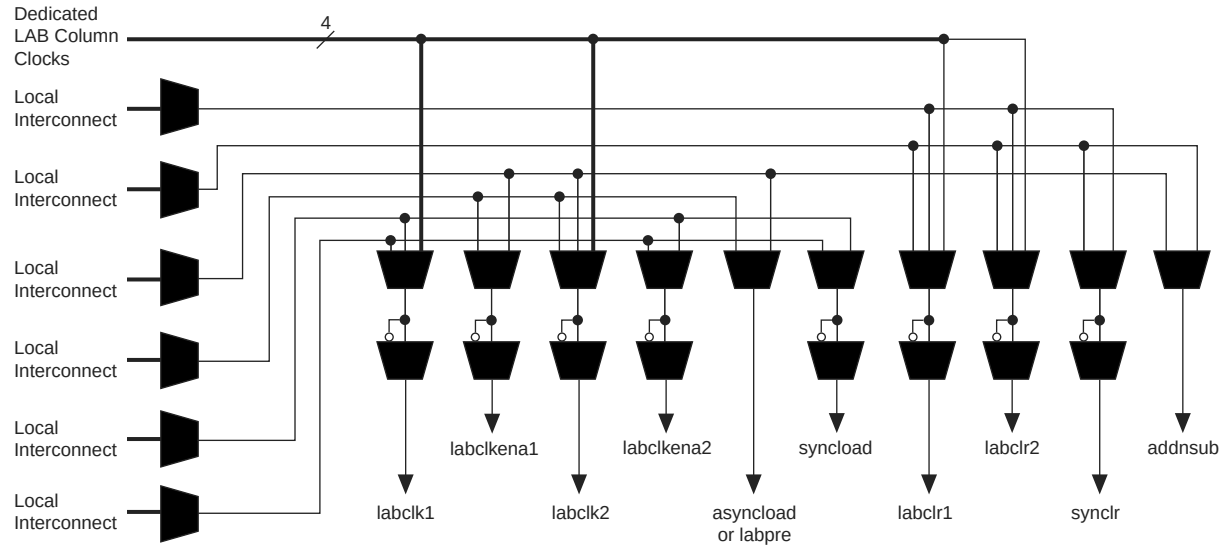

**Note to Figure 2–3:**

(1) Only from LABs adjacent to IOEs.

## LAB Interconnects

The LAB local interconnect can drive LEs within the same LAB. The LAB local interconnect is driven by column and row interconnects and LE outputs within the same LAB. Neighboring LABs, from the left and right, can also drive an LAB's local interconnect through the DirectLink connection. The DirectLink connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive 30 other LEs through fast local and DirectLink interconnects. Figure 2–4 shows the DirectLink connection.

**Figure 2–5.** LAB-Wide Control Signals

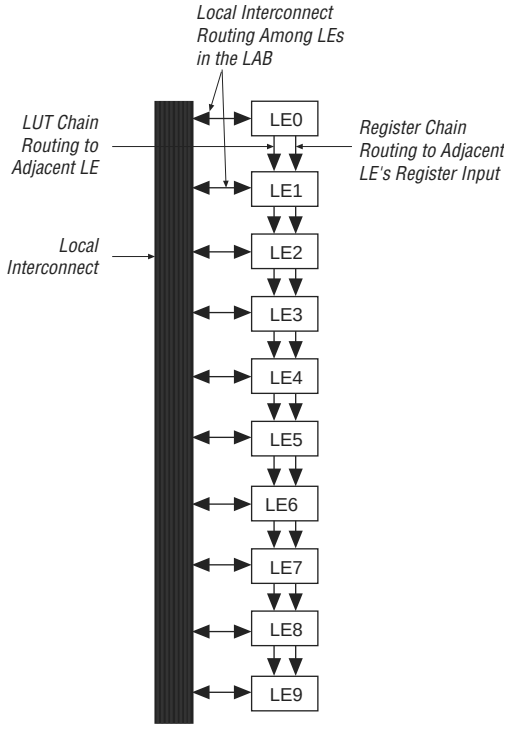



# Logic Elements

The smallest unit of logic in the MAX II architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry-select capability. A single LE also supports dynamic single-bit addition or subtraction mode selectable by an LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and DirectLink interconnects. See Figure 2–6.

functions from LE 1 to LE 10 in the same LAB. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2–11 shows the LUT chain and register chain interconnects.

**Figure 2–11.** LUT Chain and Register Chain Interconnects




The C4 interconnects span four LABs up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. Figure 2–12 shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by column and row IOEs. For LAB interconnection, a primary LAB or its vertical LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

The UFM block communicates with the logic array similar to LAB-to-LAB interfaces. The UFM block connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. This block also has DirectLink interconnects for fast connections to and from a neighboring LAB. For more information about the UFM interface to the logic array, see "User Flash Memory Block" on page 2–18.

Table 2–2 shows the MAX II device routing scheme.

**Table 2–2.** MAX II Device Routing Scheme

| Source | Destination | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | **LUT Chain** | **Register Chain** | **Local *(1)*** | **DirectLink *(1)*** | **R4 *(1)*** | **C4 *(1)*** | **LE** | **UFM Block** | **Column IOE** | **Row IOE** | **Fast I/O *(1)*** |
| LUT Chain | — | — | — | — | — | — | ✓ | — | — | — | — |
| Register Chain | — | — | — | — | — | — | ✓ | — | — | — | — |
| Local Interconnect | — | — | — | — | — | — | ✓ | ✓ | ✓ | ✓ | — |
| DirectLink Interconnect | — | — | ✓ | — | — | — | — | — | — | — | — |
| R4 Interconnect | — | — | ✓ | — | ✓ | ✓ | — | — | — | — | — |
| C4 Interconnect | — | — | ✓ | — | ✓ | ✓ | — | — | — | — | — |
| LE | ✓ | ✓ | ✓ | ✓ | ✓ | ✓ | — | — | ✓ | ✓ | ✓ |
| UFM Block | — | — | ✓ | ✓ | ✓ | ✓ | — | — | — | — | — |
| Column IOE | — | — | — | — | — | ✓ | — | — | — | — | — |
| Row IOE | — | — | — | ✓ | ✓ | ✓ | — | — | — | — | — |

**Note to Table 2–2:**

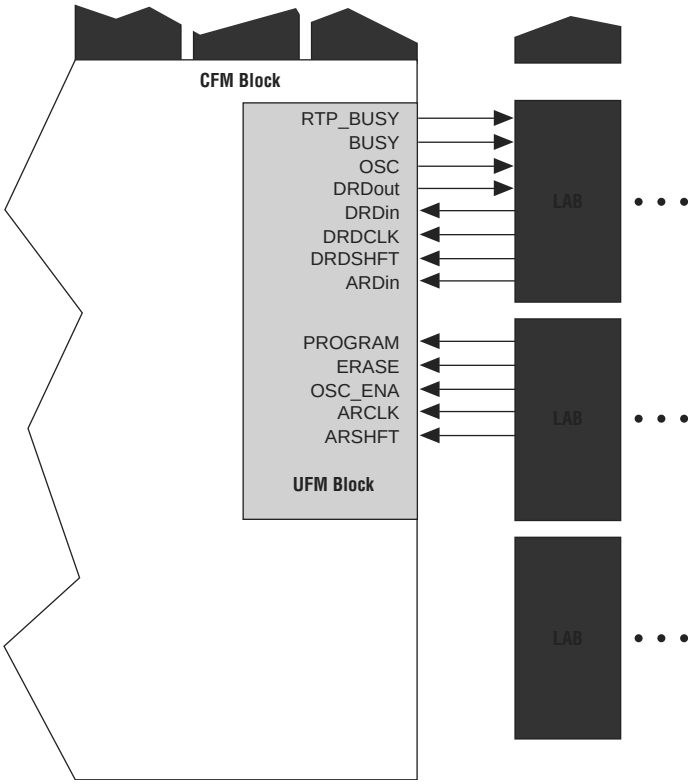
(1) These categories are interconnects.

# Global Signals

Each MAX II device has four dual-purpose dedicated clock pins (`GCLK[3..0]`, two pins on the left side and two pins on the right side) that drive the global clock network for clocking, as shown in Figure 2–13. These four pins can also be used as general-purpose I/O if they are not used to drive the global clock network.

The four global clock lines in the global clock network drive throughout the entire device. The global clock network can provide clocks for all resources within the device including LEs, LAB local interconnect, IOEs, and the UFM block. The global clock lines can also be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, or protocol control signals such as `TRDY` and `IRDY` for PCI. Internal logic can drive the global clock network for internally-generated global clocks and control signals. Figure 2–13 shows the various sources that drive the global clock network.

**Figure 2–17.** EPM570, EPM1270, and EPM2210 UFM Block LAB Row Interface




# MultiVolt Core

The MAX II architecture supports the MultiVolt core feature, which allows MAX II devices to support multiple $V_{CC}$ levels on the $V_{CCINT}$ supply. An internal linear voltage regulator provides the necessary 1.8-V internal voltage supply to the device. The voltage regulator supports 3.3-V or 2.5-V supplies on its inputs to supply the 1.8-V internal voltage to the device, as shown in Figure 2–18. The voltage regulator is not guaranteed for voltages that are between the maximum recommended 2.5-V operating voltage and the minimum recommended 3.3-V operating voltage.

The MAX IIG and MAX IIZ devices use external 1.8-V supply. The 1.8-V $V_{CC}$ external supply powers the device core directly.

**Figure 2–18.** MultiVolt Core Feature in MAX II Devices

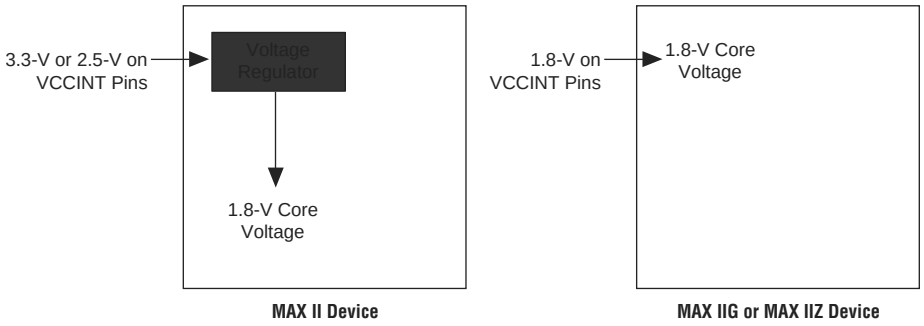
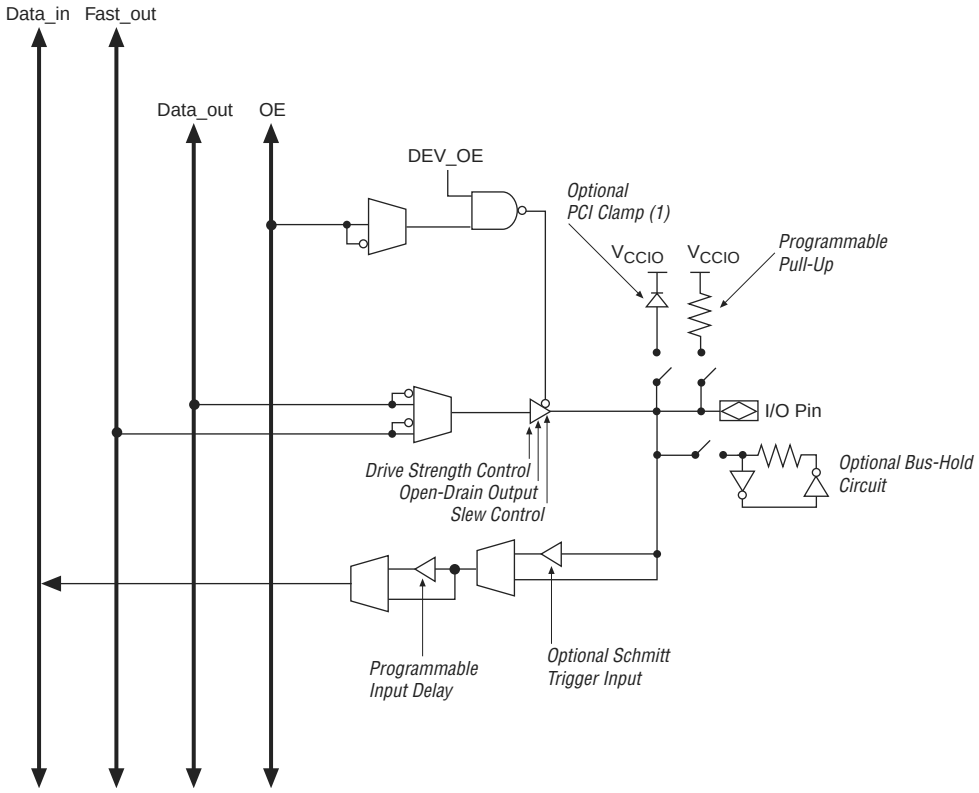


**Figure 2–19.** MAX II IOE Structure




**Note to Figure 2–19:**

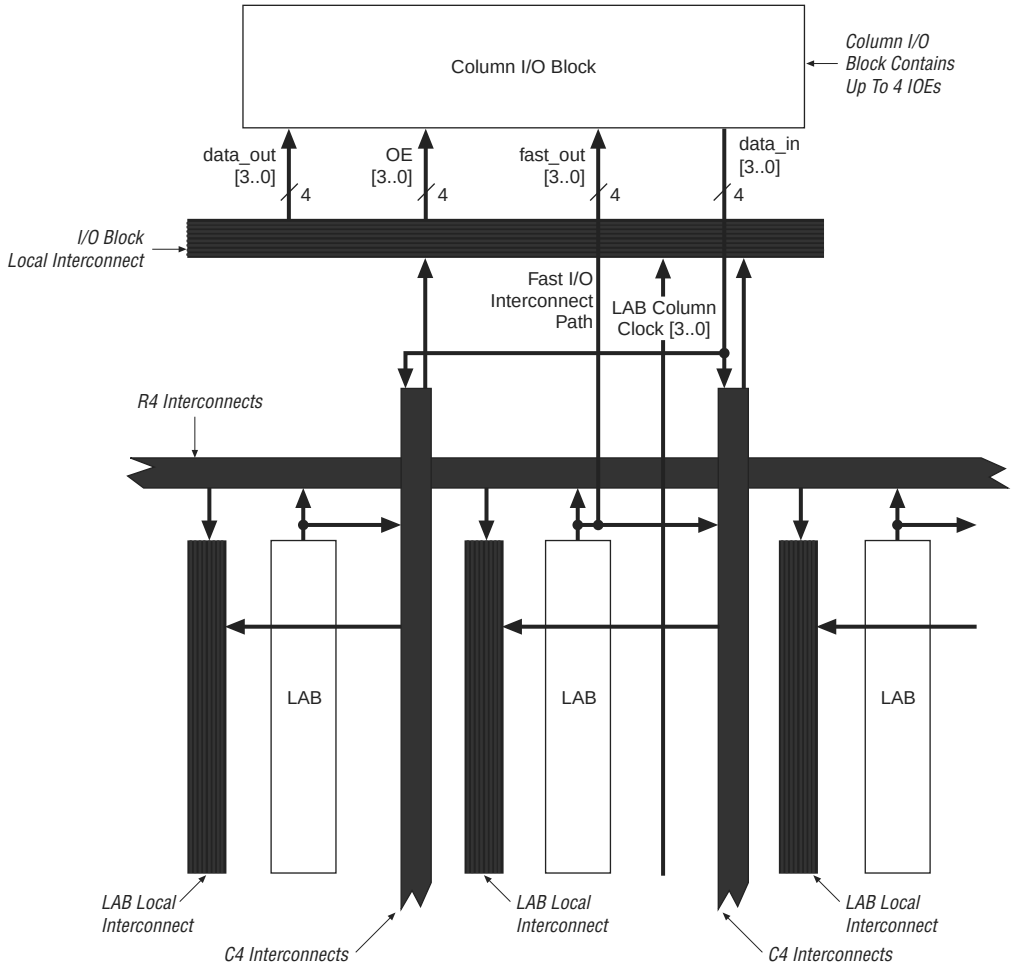
(1) Available in EPM1270 and EPM2210 devices only.

## I/O Blocks

The IOEs are located in I/O blocks around the periphery of the MAX II device. There are up to seven IOEs per row I/O block (5 maximum in the EPM240 device) and up to four IOEs per column I/O block. Each column or row I/O block interfaces with its adjacent LAB and MultiTrack interconnect to distribute signals throughout the device. The row I/O blocks drive row, column, or DirectLink interconnects. The column I/O blocks drive column interconnects.

Figure 2–21 shows how a column I/O block connects to the logic array.

**Figure 2–21.** Column I/O Block Connection to the Interconnect *(Note 1)*




**Note to Figure 2–21:**

(1) Each of the four IOEs in the column I/O block can have one `data_out` or `fast_out` output, one `OE` output, and one `data_in` input.

## I/O Standards and Banks

MAX II device IOEs support the following I/O standards:

- 3.3-V LVTTL/LVCMOS
- 2.5-V LVTTL/LVCMOS
- 1.8-V LVTTL/LVCMOS
- 1.5-V LVCMOS
- 3.3-V PCI

**Table 2–5.** MAX II Devices and Speed Grades that Support 3.3-V PCI Electrical Specifications and Meet PCI Timing

| Device | 33-MHz PCI | 66-MHz PCI |
|---|---|---|
| EPM1270 | All Speed Grades | –3 Speed Grade |
| EPM2210 | All Speed Grades | –3 Speed Grade |

## Schmitt Trigger

The input buffer for each MAX II device I/O pin has an optional Schmitt trigger setting for the 3.3-V and 2.5-V standards. The Schmitt trigger allows input buffers to respond to slow input edge rates with a fast output edge rate. Most importantly, Schmitt triggers provide hysteresis on the input buffer, preventing slow-rising noisy input signals from ringing or oscillating on the input signal driven into the logic array. This provides system noise tolerance on MAX II inputs, but adds a small, nominal input delay.

The JTAG input pins (TMS, TCK, and TDI) have Schmitt trigger buffers that are always enabled.

The TCK input is susceptible to high pulse glitches when the input signal fall time is greater than 200 ns for all I/O standards.

## Output Enable Signals

Each MAX II IOE output buffer supports output enable signals for tri-state control. The output enable signal can originate from the GCLK[3..0] global signals or from the MultiTrack interconnect. The MultiTrack interconnect routes output enable signals and allows for a unique output enable for each output or bidirectional pin.

MAX II devices also provide a chip-wide output enable pin (DEV_OE) to control the output enable for every output pin in the design. An option set before compilation in the Quartus II software controls this pin. This chip-wide output enable uses its own routing resources and does not use any of the four global resources. If this option is turned on, all outputs on the chip operate normally when DEV_OE is asserted. When the pin is deasserted, all outputs are tri-stated. If this option is turned off, the DEV_OE pin is disabled when the device operates in user mode and is available as a user I/O pin.

## Programmable Drive Strength

The output buffer for each MAX II device I/O pin has two levels of programmable drive strength control for each of the LVTTL and LVCMOS I/O standards. Programmable drive strength provides system noise reduction control for high performance I/O designs. Although a separate slew-rate control feature exists, using the lower drive strength setting provides signal slew-rate control to reduce system noise and signal overshoot without the large delay adder associated with the slew-rate control feature. Table 2–6 shows the possible settings for the I/O standards with drive strength control. The Quartus II software uses the maximum current strength as the default setting. The PCI I/O standard is always set at 20 mA with no alternate setting.

## Real-Time ISP

For systems that require more than DC logic level control of I/O pins, the real-time ISP feature allows you to update the CFM block with a new design image while the current design continues to operate in the SRAM logic array and I/O pins. A new programming file is updated into the MAX II device without halting the original design's operation, saving down-time costs for remote or field upgrades. The updated CFM block configures the new design into the SRAM upon the next power cycle. It is also possible to execute an immediate configuration of the SRAM without a power cycle by using a specific sequence of ISP commands. The configuration of SRAM without a power cycle takes a specific amount of time ($t_{CONFIG}$). During this time, the I/O pins are tri-stated and weakly pulled-up to $V_{CCIO}$.

## Design Security

All MAX II devices contain a programmable security bit that controls access to the data programmed into the CFM block. When this bit is programmed, design programming information, stored in the CFM block, cannot be copied or retrieved. This feature provides a high level of design security because programmed data within flash memory cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is erased. The SRAM is also invisible and cannot be accessed regardless of the security bit setting. The UFM block data is not protected by the security bit and is accessible through JTAG or logic array connections.

## Programming with External Hardware

MAX II devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera® ByteblasterMV™, MasterBlaster™, ByteBlaster™ II, and USB-Blaster cables.

BP Microsystems, System General, and other programming hardware manufacturers provide programming support for Altera devices. Check their websites for device support information.

# Referenced Documents

This chapter references the following documents:

- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *IEEE 1149.1 (JTAG) Boundary-Scan Testing for MAX II Devices* chapter in the *MAX II Device Handbook*
- *Real-Time ISP and ISP Clamp for MAX II Devices* chapter in the *MAX II Device Handbook*
- *Using Jam STAPL for ISP via an Embedded Processor* chapter in the *MAX II Device Handbook*

# Document Revision History

Table 3–5 shows the revision history for this chapter.

**Table 3–5.** Document Revision History

| Date and Revision | Changes Made | Summary of Changes |
|---|---|---|
| October 2008, version 1.6 | ■ Updated New Document Format. | — |
| December 2007, version 1.5 | ■ Added warning note after Table 3–1.<br>■ Updated Table 3–3 and Table 3–4.<br>■ Added "Referenced Documents" section. | — |
| December 2006, version 1.4 | ■ Added document revision history. | — |
| June 2005, version 1.3 | ■ Added text and Table 3-4. | — |
| June 2005, version 1.3 | ■ Updated text on pages 3-5 to 3-8. | — |
| June 2004, version 1.1 | ■ Corrected Figure 3-1. Added CFM acronym. | — |

## I/O Pins Remain Tri-Stated during Power-Up

A device that does not support hot-socketing may interrupt system operation or cause contention by driving out before or during power-up. In a hot socketing situation, the MAX II device's output buffers are turned off during system power-up. MAX II devices do not drive out until the device attains proper operating conditions and is fully configured. Refer to "Power-On Reset Circuitry" on page 4–5 for information about turn-on voltages.

## Signal Pins Do Not Drive the $V_{CCIO}$ or $V_{CCINT}$ Power Supplies

MAX II devices do not have a current path from I/O pins or GCLK[3..0] pins to the $V_{CCIO}$ or $V_{CCINT}$ pins before or during power-up. A MAX II device may be inserted into (or removed from) a system board that was powered up without damaging or interfering with system-board operation. When hot socketing, MAX II devices may have a minimal effect on the signal integrity of the backplane.

## AC and DC Specifications

You can power up or power down the $V_{CCIO}$ and $V_{CCINT}$ pins in any sequence. During hot socketing, the I/O pin capacitance is less than 8 pF. MAX II devices meet the following hot socketing specifications:

- The hot socketing DC specification is: $| I_{IOPIN} | < 300$ µA.
- The hot socketing AC specification is: $| I_{IOPIN} | < 8$ mA for 10 ns or less.

MAX II devices are immune to latch-up when hot socketing. If the TCK JTAG input pin is driven high during hot socketing, the current on that pin might exceed the specifications above.

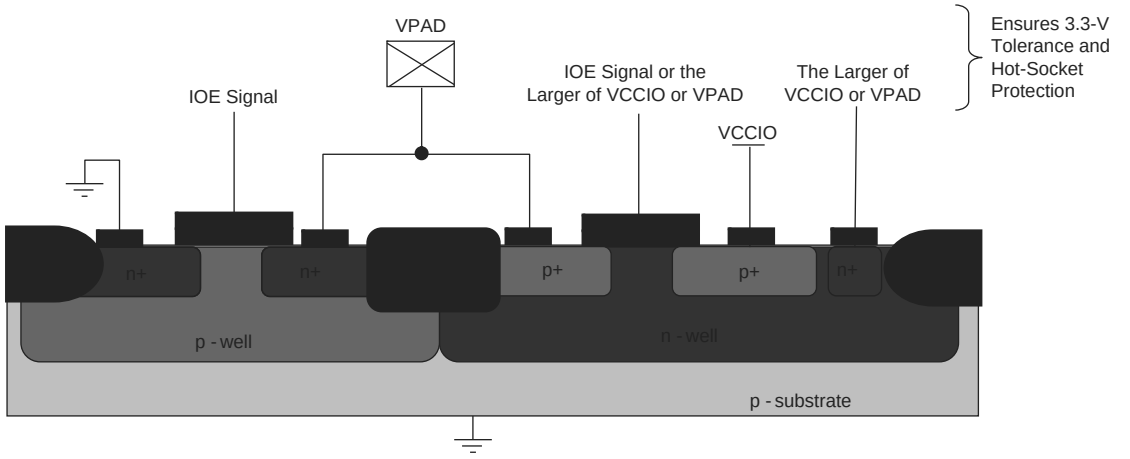
$I_{IOPIN}$ is the current at any user I/O pin on the device. The AC specification applies when the device is being powered up or powered down. This specification takes into account the pin capacitance but not board trace and external loading capacitance. Additional capacitance for trace, connector, and loading must be taken into consideration separately. The peak current duration due to power-up transients is 10 ns or less.

The DC specification applies when all $V_{CC}$ supplies to the device are stable in the powered-up or powered-down conditions.

# Hot Socketing Feature Implementation in MAX II Devices

The hot socketing feature turns off (tri-states) the output buffer during the power-up event (either $V_{CCINT}$ or $V_{CCIO}$ supplies) or power-down event. The hot-socket circuit generates an internal HOTSCKT signal when either $V_{CCINT}$ or $V_{CCIO}$ is below the threshold voltage during power-up or power-down. The HOTSCKT signal cuts off the output buffer to make sure that no DC current (except for weak pull-up leaking) leaks through the pin. When $V_{CC}$ ramps up very slowly during power-up, $V_{CC}$ may still be relatively low even after the power-on reset (POR) signal is released and device configuration is complete.

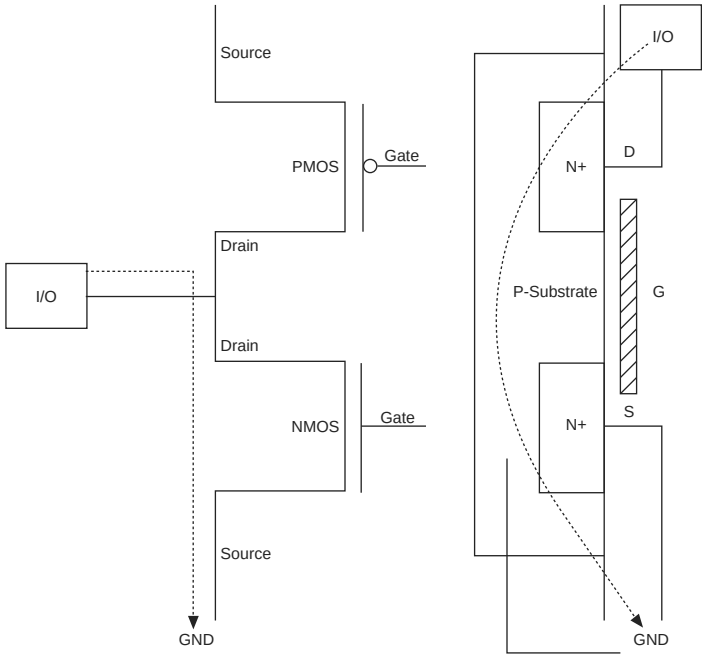
**Figure 4–2.** Transistor-Level Diagram of MAX II Device I/O Buffers




The CMOS output drivers in the I/O pins intrinsically provide electrostatic discharge (ESD) protection. There are two cases to consider for ESD voltage strikes: positive voltage zap and negative voltage zap.

A positive ESD voltage zap occurs when a positive voltage is present on an I/O pin due to an ESD charge event. This can cause the N+ (Drain)/ P-Substrate junction of the N-channel drain to break down and the N+ (Drain)/P-Substrate/N+ (Source) intrinsic bipolar transistor turn on to discharge ESD current from I/O pin to GND. The dashed line (see Figure 4–3) shows the ESD current discharge path during a positive ESD zap.

**Figure 4–3.** ESD Protection During Positive Voltage Zap



## Power-Up Characteristics

When power is applied to a MAX II device, the POR circuit monitors $V_{CCINT}$ and begins SRAM download at an approximate voltage of 1.7 V or 1.55 V for MAX IIG and MAX IIZ devices. From this voltage reference, SRAM download and entry into user mode takes 200 to 450 µs maximum, depending on device density. This period of time is specified as $t_{CONFIG}$ in the power-up timing section of the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*.

Entry into user mode is gated by whether all $V_{CCIO}$ banks are powered with sufficient operating voltage. If $V_{CCIN}$T and $V_{CCIO}$ are powered simultaneously, the device enters user mode within the $t_{CONFIG}$ specifications. If $V_{CCIO}$ is powered more than $t_{CONFIG}$ after $V_{CCINT}$, the device does not enter user mode until 2 µs after all $V_{CCIO}$ banks are powered.

For MAX II and MAX IIG devices, when in user mode, the POR circuitry continues to monitor the $V_{CCINT}$ (but not $V_{CCIO}$) voltage level to detect a brown-out condition. If there is a $V_{CCINT}$ voltage sag at or below 1.4 V during user mode, the POR circuit resets the SRAM and tri-states the I/O pins. Once $V_{CCINT}$ rises back to approximately 1.7 V (or 1.55 V for MAX IIG devices), the SRAM download restarts and the device begins to operate after $t_{CONFIG}$ time has passed.

For MAX IIZ devices, the POR circuitry does not monitor the $V_{CCINT}$ and $V_{CCIO}$ voltage levels after the device enters user mode. If there is a $V_{CCINT}$ voltage sag below 1.4 V during user mode, the functionality of the device will not be guaranteed and you must power down the $V_{CCINT}$ to 0 V for a minimum of 10 µs before powering the $V_{CCINT}$ and $V_{CCIO}$ up again. Once $V_{CCINT}$ rises from 0 V back to approximately 1.55 V, the SRAM download restarts and the device begins to operate after $t_{CONFIG}$ time has passed.

Figure 4–5 shows the voltages for POR of MAX II, MAX IIG, and MAX IIZ devices during power-up into user mode and from user mode to power-down or brown-out.

All $V_{CCINT}$ and $V_{CCIO}$ pins of all banks must be powered on MAX II devices before entering user mode.

## Programming/Erasure Specifications

Table 5–3 shows the MAX II device family programming/erasure specifications.

**Table 5–3.** MAX II Device Programming/Erasure Specifications

| Parameter | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|
| Erase and reprogram cycles | — | — | 100 *(1)* | Cycles |

**Note to Table 5–3:**

(1) This specification applies to the UFM and configuration flash memory (CFM) blocks.

## DC Electrical Characteristics

Table 5–4 shows the MAX II device family DC electrical characteristics.

**Table 5–4.** MAX II Device DC Electrical Characteristics *(Note 1)* (Part 1 of 2)

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin leakage current | $V_I = V_{CCIO}$ max to 0 V *(2)* | –10 | — | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O = V_{CCIO}$ max to 0 V *(2)* | –10 | — | 10 | µA |
| $I_{CCSTANDBY}$ | $V_{CCINT}$ supply current (standby) *(3)* | MAX II devices | — | 12 | — | mA |
| | | MAX IIG devices | — | 2 | — | mA |
| | | EPM240Z (Commercial grade) *(4)* | — | 25 | 90 | µA |
| | | EPM240Z (Industrial grade) *(5)* | — | 25 | 139 | µA |
| | | EPM570Z (Commercial grade) *(4)* | — | 27 | 96 | µA |
| | | EPM570Z (Industrial grade) *(5)* | — | 27 | 152 | µA |
| $V_{SCHMITT}$ *(6)* | Hysteresis for Schmitt trigger input *(7)* | $V_{CCIO}$ = 3.3 V | — | 400 | — | mV |
| | | $V_{CCIO}$ = 2.5 V | — | 190 | — | mV |
| $I_{CCPOWERUP}$ | $V_{CCINT}$ supply current during power-up *(8)* | MAX II devices | — | 55 | — | mA |
| | | MAX IIG and MAX IIZ devices | — | 40 | — | mA |
| $R_{PULLUP}$ | Value of I/O pin pull-up resistor during user mode and in-system programming | $V_{CCIO}$ = 3.3 V *(9)* | 5 | — | 25 | kΩ |
| | | $V_{CCIO}$ = 2.5 V *(9)* | 10 | — | 40 | kΩ |
| | | $V_{CCIO}$ = 1.8 V *(9)* | 25 | — | 60 | kΩ |
| | | $V_{CCIO}$ = 1.5 V *(9)* | 45 | — | 95 | kΩ |

**Table 5–20.** $t_{XZ}$ IOE Microparameter Adders for Slow Slew Rate

| Standard | | MAX II / MAX IIG | | | | | | MAX IIZ | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –3 Speed Grade | | –4 Speed Grade | | –5 Speed Grade | | –6 Speed Grade | | –7 Speed Grade | | –8 Speed Grade | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| 3.3-V LVTTL | 16 mA | — | 206 | — | –20 | — | –247 | — | 1,433 | — | 1,446 | — | 1,454 | ps |
| | 8 mA | — | 891 | — | 665 | — | 438 | — | 1,332 | — | 1,345 | — | 1,348 | ps |
| 3.3-V LVCMOS | 8 mA | — | 206 | — | –20 | — | –247 | — | 1,433 | — | 1,446 | — | 1,454 | ps |
| | 4 mA | — | 891 | — | 665 | — | 438 | — | 1,332 | — | 1,345 | — | 1,348 | ps |
| 2.5-V LVTTL / LVCMOS | 14 mA | — | 222 | — | –4 | — | –231 | — | 213 | — | 208 | — | 213 | ps |
| | 7 mA | — | 943 | — | 717 | — | 490 | — | 166 | — | 161 | — | 166 | ps |
| 3.3-V PCI | 20 mA | — | 161 | — | 210 | — | 258 | — | 1,332 | — | 1,345 | — | 1,348 | ps |

☞ The default slew rate setting for MAX II devices in the Quartus II design software is "fast".

**Table 5–21.** UFM Block Internal Timing Microparameters (Part 1 of 3)

| Symbol | Parameter | MAX II / MAX IIG | | | | | | MAX IIZ | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –3 Speed Grade | | –4 Speed Grade | | –5 Speed Grade | | –6 Speed Grade | | –7 Speed Grade | | –8 Speed Grade | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{ACLK}$ | Address register clock period | 100 | — | 100 | — | 100 | — | 100 | — | 100 | — | 100 | — | ns |
| $t_{ASU}$ | Address register shift signal setup to address register clock | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | ns |
| $t_{AH}$ | Address register shift signal hold to address register clock | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | ns |
| $t_{ADS}$ | Address register data in setup to address register clock | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | ns |
| $t_{ADH}$ | Address register data in hold from address register clock | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | ns |
| $t_{DCLK}$ | Data register clock period | 100 | — | 100 | — | 100 | — | 100 | — | 100 | — | 100 | — | ns |
| $t_{DSS}$ | Data register shift signal setup to data register clock | 60 | — | 60 | — | 60 | — | 60 | — | 60 | — | 60 | — | ns |
| $t_{DSH}$ | Data register shift signal hold from data register clock | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | ns |

**Table 5–21.** UFM Block Internal Timing Microparameters (Part 2 of 3)

| Symbol | Parameter | MAX II / MAX IIG | | | | | | MAX IIZ | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –3 Speed Grade | | –4 Speed Grade | | –5 Speed Grade | | –6 Speed Grade | | –7 Speed Grade | | –8 Speed Grade | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| $t_{DDS}$ | Data register data in setup to data register clock | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | ns |
| $t_{DDH}$ | Data register data in hold from data register clock | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | ns |
| $t_{DP}$ | Program signal to data clock hold time | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{PB}$ | Maximum delay between program rising edge to UFM busy signal rising edge | — | 960 | — | 960 | — | 960 | — | 960 | — | 960 | — | 960 | ns |
| $t_{BP}$ | Minimum delay allowed from UFM busy signal going low to program signal going low | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | ns |
| $t_{PPMX}$ | Maximum length of busy pulse during a program | — | 100 | — | 100 | — | 100 | — | 100 | — | 100 | — | 100 | µs |
| $t_{AE}$ | Minimum erase signal to address clock hold time | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{EB}$ | Maximum delay between the erase rising edge to the UFM busy signal rising edge | — | 960 | — | 960 | — | 960 | — | 960 | — | 960 | — | 960 | ns |
| $t_{BE}$ | Minimum delay allowed from the UFM busy signal going low to erase signal going low | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | 20 | — | ns |
| $t_{EPMX}$ | Maximum length of busy pulse during an erase | — | 500 | — | 500 | — | 500 | — | 500 | — | 500 | — | 500 | ms |
| $t_{DCO}$ | Delay from data register clock to data register output | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | — | 5 | ns |

**Figure 5–4.** UFM Program Waveforms

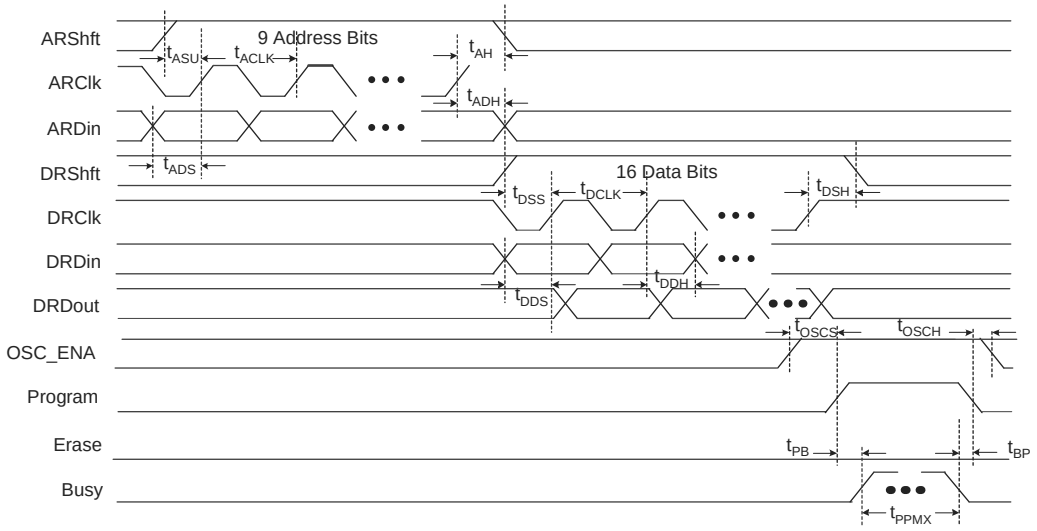



**Figure 5–5.** UFM Erase Waveform

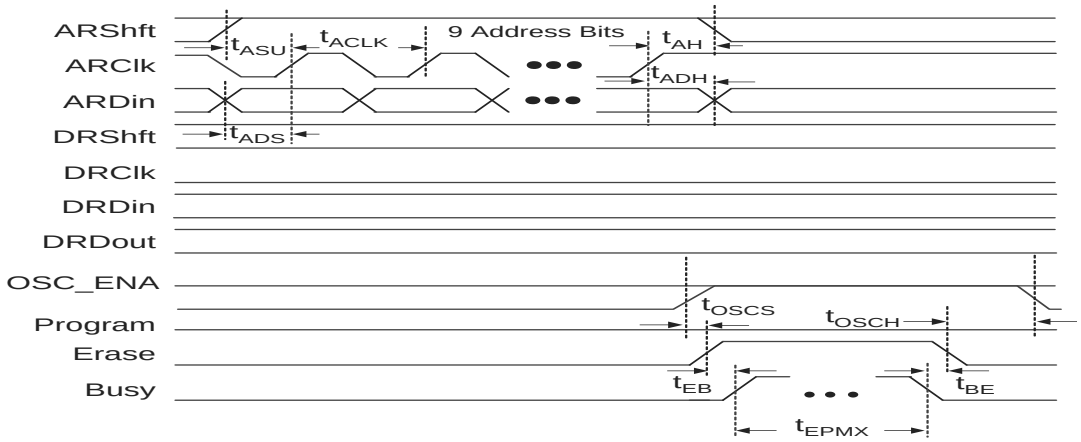



**Table 5–22.** Routing Delay Internal Timing Microparameters

| | MAX II / MAX IIG | | | | | | MAX IIZ | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | –3 Speed Grade | | –4 Speed Grade | | –5 Speed Grade | | –6 Speed Grade | | –7 Speed Grade | | –8 Speed Grade | | |
| **Routing** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** |
| $t_{C4}$ | — | 429 | — | 556 | — | 687 | — | *(1)* | — | *(1)* | — | *(1)* | ps |
| $t_{R4}$ | — | 326 | — | 423 | — | 521 | — | *(1)* | — | *(1)* | — | *(1)* | ps |
| $t_{LOCAL}$ | — | 330 | — | 429 | — | 529 | — | *(1)* | — | *(1)* | — | *(1)* | ps |

**Note to Table 5–22:**

(1) The numbers will only be available in a later revision.

Table 5–26 shows the external I/O timing parameters for EPM2210 devices.

**Table 5–26.** EPM2210 Global Clock External I/O Timing Parameters

| Symbol | Parameter | Condition | MAX II / MAX IIG | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | –3 Speed Grade | | –4 Speed Grade | | –5 Speed Grade | | |
| | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD1}$ | Worst case pin-to-pin delay through 1 look-up table (LUT) | 10 pF | — | 7.0 | — | 9.1 | — | 11.2 | ns |
| $t_{PD2}$ | Best case pin-to-pin delay through 1 LUT | 10 pF | — | 3.7 | — | 4.8 | — | 5.9 | ns |
| $t_{SU}$ | Global clock setup time | — | 1.2 | — | 1.5 | — | 1.9 | — | ns |
| $t_{H}$ | Global clock hold time | — | 0 | — | 0 | — | 0 | — | ns |
| $t_{CO}$ | Global clock to output delay | 10 pF | 2.0 | 4.6 | 2.0 | 6.0 | 2.0 | 7.4 | ns |
| $t_{CH}$ | Global clock high time | — | 166 | — | 216 | — | 266 | — | ps |
| $t_{CL}$ | Global clock low time | — | 166 | — | 216 | — | 266 | — | ps |
| $t_{CNT}$ | Minimum global clock period for 16-bit counter | — | 3.3 | — | 4.0 | — | 5.0 | — | ns |
| $f_{CNT}$ | Maximum global clock frequency for 16-bit counter | — | — | 304.0 *(1)* | — | 247.5 | — | 201.1 | MHz |

**Note to Table 5–26:**

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

## External Timing I/O Delay Adders

The I/O delay timing parameters for I/O standard input and output adders, and input delays are specified by speed grade independent of device density.

Table 5–27 through Table 5–31 show the adder delays associated with I/O pins for all packages. The delay numbers for –3, –4, and –5 speed grades shown in Table 5–27 through Table 5–33 are based on an EPM1270 device target, while –6, –7, and –8 speed grade values are based on an EPM570Z device target. If an I/O standard other than 3.3-V LVTTL is selected, add the input delay adder to the external $t_{SU}$ timing parameters shown in Table 5–23 through Table 5–26. If an I/O standard other than 3.3-V LVTTL with 16 mA drive strength and fast slew rate is selected, add the output delay adder to the external $t_{CO}$ and $t_{PD}$ shown in Table 5–23 through Table 5–26.

**Table 5–27.** External Timing Input Delay Adders (Part 1 of 2)

| I/O Standard | | MAX II / MAX IIG | | | | | | MAX IIZ | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | –3 Speed Grade | | –4 Speed Grade | | –5 Speed Grade | | –6 Speed Grade | | –7 Speed Grade | | –8 Speed Grade | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | Min | Max | |
| 3.3-V LVTTL | Without Schmitt Trigger | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | — | 0 | ps |
| | With Schmitt Trigger | — | 334 | — | 434 | — | 535 | — | 387 | — | 434 | — | 442 | ps |

**Table 5–33.** MAX II Maximum Output Clock Rate for I/O

| I/O Standard | | MAX II / MAX IIG | | | MAX IIZ | | |
|---|---|---|---|---|---|---|---|
| | | –3 Speed Grade | –4 Speed Grade | –5 Speed Grade | –6 Speed Grade | –7 Speed Grade | –8 Speed Grade |
| 3.3-V LVTTL | 304 | 304 | 304 | 304 | 304 | 304 | MHz |
| 3.3-V LVCMOS | 304 | 304 | 304 | 304 | 304 | 304 | MHz |
| 2.5-V LVTTL | 220 | 220 | 220 | 220 | 220 | 220 | MHz |
| 2.5-V LVCMOS | 220 | 220 | 220 | 220 | 220 | 220 | MHz |
| 1.8-V LVTTL | 200 | 200 | 200 | 200 | 200 | 200 | MHz |
| 1.8-V LVCMOS | 200 | 200 | 200 | 200 | 200 | 200 | MHz |
| 1.5-V LVCMOS | 150 | 150 | 150 | 150 | 150 | 150 | MHz |
| 3.3-V PCI | 304 | 304 | 304 | 304 | 304 | 304 | MHz |

## JTAG Timing Specifications

Figure 5–6 shows the timing waveforms for the JTAG signals.

**Figure 5–6.** MAX II JTAG Timing Waveforms

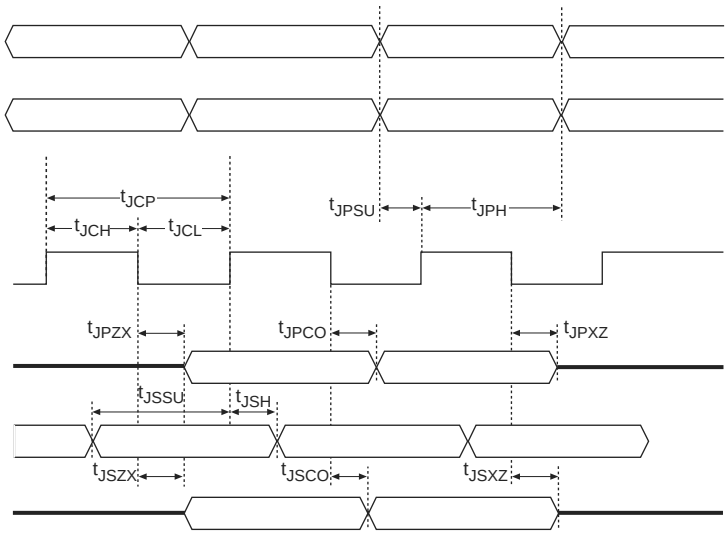



Table 5–34 shows the JTAG Timing parameters and values for MAX II devices.

**Table 5–34.** MAX II JTAG Timing Parameters (Part 1 of 2)

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ *(1)* | TCK clock period for $V_{CCIO1}$ = 3.3 V | 55.5 | — | ns |
| | TCK clock period for $V_{CCIO1}$ = 2.5 V | 62.5 | — | ns |
| | TCK clock period for $V_{CCIO1}$ = 1.8 V | 100 | — | ns |
| | TCK clock period for $V_{CCIO1}$ = 1.5 V | 143 | — | ns |
| $t_{JCH}$ | TCK clock high time | 20 | — | ns |
| $t_{JCL}$ | TCK clock low time | 20 | — | ns |