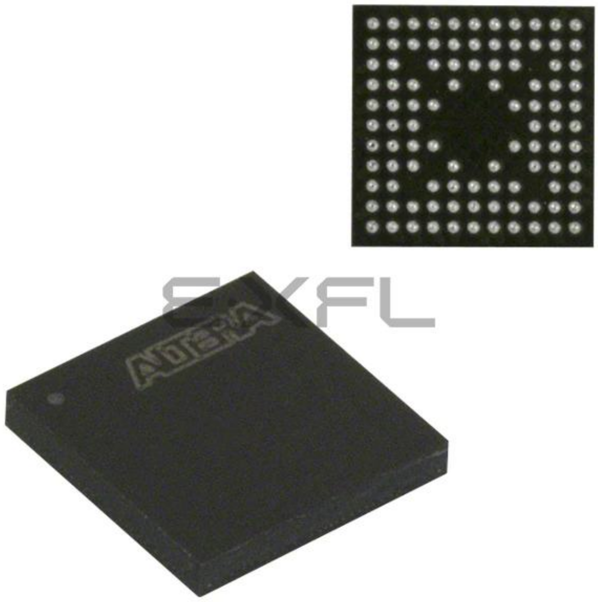
Intel - EPM570ZM100I8N Datasheet



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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	9 ns
Voltage Supply - Internal	1.71V ~ 1.89V
Number of Logic Elements/Blocks	570
Number of Macrocells	440
Number of Gates	-
Number of I/O	76
Operating Temperature	-40°C ~ 100°C (TJ)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-MBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/intel/epm570zm100i8n

Table 1–1 shows the MAX II family features.

Table 1–1. MAX II Family Features

Feature	EPM240 EPM240G	EPM570 EPM570G	EPM1270 EPM1270G	EPM2210 EPM2210G	EPM240Z	EPM570Z
LEs	240	570	1,270	2,210	240	570
Typical Equivalent Macrocells	192	440	980	1,700	192	440
Equivalent Macrocell Range	128 to 240	240 to 570	570 to 1,270	1,270 to 2,210	128 to 240	240 to 570
UFM Size (bits)	8,192	8,192	8,192	8,192	8,192	8,192
Maximum User I/O pins	80	160	212	272	80	160
t_{PD1} (ns) *(1)*	4.7	5.4	6.2	7.0	7.5	9.0
f_{CNT} (MHz) *(2)*	304	304	304	304	152	152
t_{SU} (ns)	1.7	1.2	1.2	1.2	2.3	2.2
t_{CO} (ns)	4.3	4.5	4.6	4.6	6.5	6.7

Notes to Table 1–1:

(1) t_{PD1} represents a pin-to-pin delay for the worst case I/O placement with a full diagonal path across the device and combinational logic implemented in a single LUT and LAB that is adjacent to the output pin.

(2) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay will run faster than this number.

For more information about equivalent macrocells, refer to the *MAX II Logic Element to Macrocell Conversion Methodology* white paper.

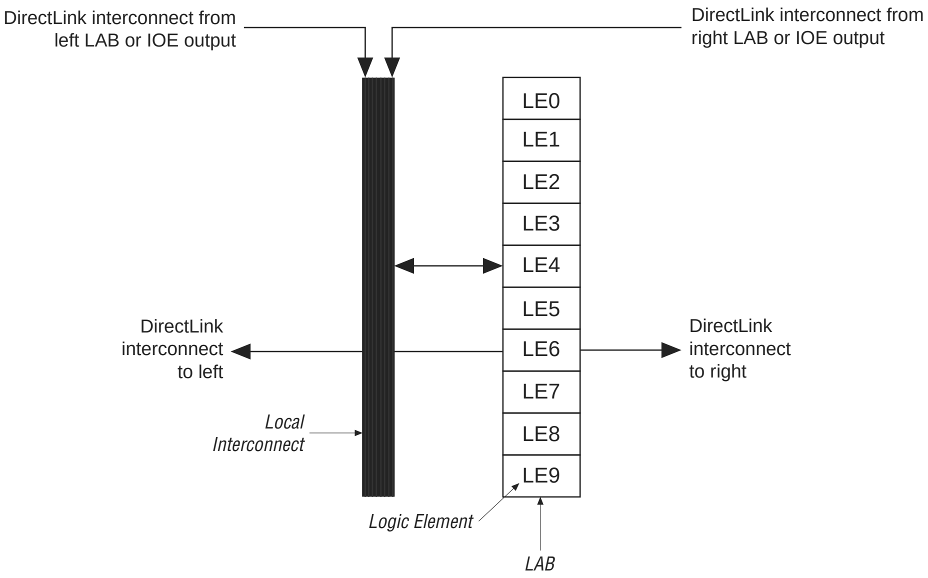
MAX II and MAX IIG devices are available in three speed grades: –3, –4, and –5, with –3 being the fastest. Similarly, MAX IIZ devices are available in three speed grades: –6, –7, and –8, with –6 being the fastest. These speed grades represent the overall relative performance, not any specific timing parameter. For propagation delay timing numbers within each speed grade and density, refer to the *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*.

Table 1–2 shows MAX II device speed-grade offerings.

Table 1–2. MAX II Speed Grades

Device	Speed Grade					
	–3	–4	–5	–6	–7	–8
EPM240 EPM240G	✓	✓	✓	—	—	—
EPM570 EPM570G	✓	✓	✓	—	—	—
EPM1270 EPM1270G	✓	✓	✓	—	—	—
EPM2210 EPM2210G	✓	✓	✓	—	—	—
EPM240Z	—	—	—	✓	✓	✓
EPM570Z	—	—	—	✓	✓	✓

Figure 2–4. DirectLink Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, a synchronous clear, an asynchronous preset/load, a synchronous load, and add/subtract control signals, providing a maximum of 10 control signals at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB’s clock and clock enable signals are linked. For example, any LE in a particular LAB using the `labclk1` signal also uses `labclkena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. Deasserting the clock enable signal turns off the LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. By default, the Quartus II software uses a `NOT` gate push-back technique to achieve preset. If you disable the `NOT` gate push-back option or assign a given register to power-up high using the Quartus II software, the preset is then achieved using the asynchronous load signal with asynchronous load data input tied high.

With the LAB-wide addnsub control signal, a single LE can implement a one-bit adder and subtractor. This saves LE resources and improves performance for logic functions such as correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB column clocks [3..0], driven by the global clock network, and LAB local interconnect generate the LAB-wide control signals. The MultiTrack interconnect structure drives the LAB local interconnect for non-global control signal generation. The MultiTrack interconnect’s inherent low skew allows clock and control signal distribution in addition to data. Figure 2–5 shows the LAB control signal generation circuit.

The UFM block communicates with the logic array similar to LAB-to-LAB interfaces. The UFM block connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. This block also has DirectLink interconnects for fast connections to and from a neighboring LAB. For more information about the UFM interface to the logic array, see "User Flash Memory Block" on page 2–18.

Table 2–2 shows the MAX II device routing scheme.

Table 2–2. MAX II Device Routing Scheme

Source	Destination										
	LUT Chain	**Register Chain**	**Local *(1)***	**DirectLink *(1)***	**R4 *(1)***	**C4 *(1)***	**LE**	**UFM Block**	**Column IOE**	**Row IOE**	**Fast I/O *(1)***
LUT Chain	—	—	—	—	—	—	✓	—	—	—	—
Register Chain	—	—	—	—	—	—	✓	—	—	—	—
Local Interconnect	—	—	—	—	—	—	✓	✓	✓	✓	—
DirectLink Interconnect	—	—	✓	—	—	—	—	—	—	—	—
R4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
C4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
LE	✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓
UFM Block	—	—	✓	✓	✓	✓	—	—	—	—	—
Column IOE	—	—	—	—	—	✓	—	—	—	—	—
Row IOE	—	—	—	✓	✓	✓	—	—	—	—	—

Note to Table 2–2:

(1) These categories are interconnects.

Global Signals

Each MAX II device has four dual-purpose dedicated clock pins (`GCLK[3..0]`, two pins on the left side and two pins on the right side) that drive the global clock network for clocking, as shown in Figure 2–13. These four pins can also be used as general-purpose I/O if they are not used to drive the global clock network.

The four global clock lines in the global clock network drive throughout the entire device. The global clock network can provide clocks for all resources within the device including LEs, LAB local interconnect, IOEs, and the UFM block. The global clock lines can also be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, or protocol control signals such as `TRDY` and `IRDY` for PCI. Internal logic can drive the global clock network for internally-generated global clocks and control signals. Figure 2–13 shows the various sources that drive the global clock network.

Internal Oscillator

As shown in Figure 2–15, the dedicated circuitry within the UFM block contains an oscillator. The dedicated circuitry uses this internally for its read and program operations. This oscillator's divide by 4 output can drive out of the UFM block as a logic interface clock source or for general-purpose logic clocking. The typical `OSC` output signal frequency ranges from 3.3 to 5.5 MHz, and its exact frequency of operation is not programmable.

Program, Erase, and Busy Signals

The UFM block’s dedicated circuitry automatically generates the necessary internal program and erase algorithm once the `PROGRAM` or `ERASE` input signals have been asserted. The `PROGRAM` or `ERASE` signal must be asserted until the busy signal deasserts, indicating the UFM internal program or erase operation has completed. The UFM block also supports JTAG as the interface for programming and/or reading.

For more information about programming and erasing the UFM block, refer to the *Using User Flash Memory in MAX II Devices* chapter in the *MAX II Device Handbook*.

Auto-Increment Addressing

The UFM block supports standard read or stream read operations. The stream read is supported with an auto-increment address feature. Deasserting the `ARSHIFT` signal while clocking the `ARCLK` signal increments the address register value to read consecutive locations from the UFM array.

Serial Interface

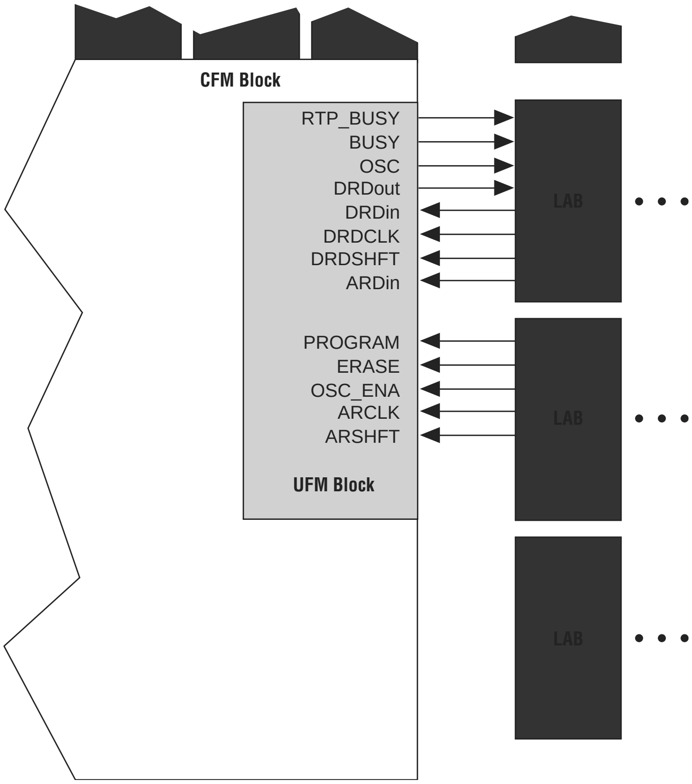
The UFM block supports a serial interface with serial address and data signals. The internal shift registers within the UFM block for address and data are 9 bits and 16 bits wide, respectively. The Quartus II software automatically generates interface logic in LEs for a parallel address and data interface to the UFM block. Other standard protocol interfaces such as SPI are also automatically generated in LE logic by the Quartus II software.

For more information about the UFM interface signals and the Quartus II LE-based alternate interfaces, refer to the *Using User Flash Memory in MAX II Devices* chapter in the *MAX II Device Handbook*.

UFM Block to Logic Array Interface

The UFM block is a small partition of the flash memory that contains the CFM block, as shown in Figure 2–1 and Figure 2–2. The UFM block for the EPM240 device is located on the left side of the device adjacent to the left most LAB column. The UFM block for the EPM570, EPM1270, and EPM2210 devices is located at the bottom left of the device. The UFM input and output signals interface to all types of interconnects (R4 interconnect, C4 interconnect, and DirectLink interconnect to/from adjacent LAB rows). The UFM signals can also be driven from global clocks, `GCLK[3..0]`. The interface region for the EPM240 device is shown in Figure 2–16. The interface regions for EPM570, EPM1270, and EPM2210 devices are shown in Figure 2–17.

Figure 2–17. EPM570, EPM1270, and EPM2210 UFM Block LAB Row Interface

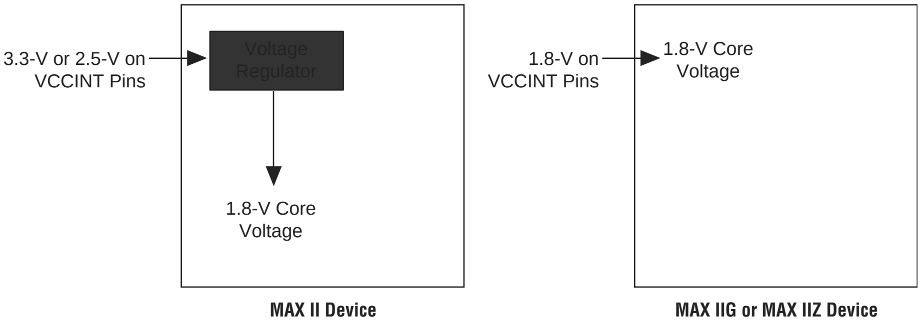


MultiVolt Core

The MAX II architecture supports the MultiVolt core feature, which allows MAX II devices to support multiple V_{CC} levels on the V_{CCINT} supply. An internal linear voltage regulator provides the necessary 1.8-V internal voltage supply to the device. The voltage regulator supports 3.3-V or 2.5-V supplies on its inputs to supply the 1.8-V internal voltage to the device, as shown in Figure 2–18. The voltage regulator is not guaranteed for voltages that are between the maximum recommended 2.5-V operating voltage and the minimum recommended 3.3-V operating voltage.

The MAX IIG and MAX IIZ devices use external 1.8-V supply. The 1.8-V V_{CC} external supply powers the device core directly.

Figure 2–18. MultiVolt Core Feature in MAX II Devices



I/O Structure

IOEs support many features, including:

- LVTTL and LVCMOS I/O standards
- 3.3-V, 32-bit, 66-MHz PCI compliance
- Joint Test Action Group (JTAG) boundary-scan test (BST) support
- Programmable drive strength control
- Weak pull-up resistors during power-up and in system programming
- Slew-rate control
- Tri-state buffers with individual output enable control
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Unique output enable per pin
- Open-drain outputs
- Schmitt trigger inputs
- Fast I/O connection
- Programmable input delay

MAX II device IOEs contain a bidirectional I/O buffer. Figure 2–19 shows the MAX II IOE structure. Registers from adjacent LABs can drive to or be driven from the IOE's bidirectional I/O buffers. The Quartus II software automatically attempts to place registers in the adjacent LAB with fast I/O connection to achieve the fastest possible clock-to-output and registered output enable timing. For input registers, the Quartus II software automatically routes the register to guarantee zero hold time. You can set timing assignments in the Quartus II software to achieve desired I/O timing.

Fast I/O Connection

A dedicated fast I/O connection from the adjacent LAB to the IOEs within an I/O block provides faster output delays for clock-to-output and t_{PD} propagation delays. This connection exists for data output signals, not output enable signals or input signals. Figure 2–20, Figure 2–21, and Figure 2–22 illustrate the fast I/O connection.

Connect `VCCIO` pins to either a 1.5-V, 1.8 V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (that is, when `VCCIO` pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When `VCCIO` pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems. Table 2–7 summarizes MAX II MultiVolt I/O support.

Table 2–7. MAX II MultiVolt I/O Support *(Note 1)*

	Input Signal					**Output Signal**				
VCCIO (V)	**1.5 V**	**1.8 V**	**2.5 V**	**3.3 V**	**5.0 V**	**1.5 V**	**1.8 V**	**2.5 V**	**3.3 V**	**5.0 V**
1.5	✓	✓	✓	✓	—	✓	—	—	—	—
1.8	✓	✓	✓	✓	—	✓ *(2)*	✓	—	—	—
2.5	—	—	✓	✓	—	✓ *(3)*	✓ *(3)*	✓	—	—
3.3	—	—	✓ *(4)*	✓	✓ *(5)*	✓ *(6)*	✓ *(6)*	✓ *(6)*	✓	✓ *(7)*

Notes to Table 2–7:

(1) To drive inputs higher than V_{CCIO} but less than 4.0 V including the overshoot, disable the I/O clamp diode. However, to drive 5.0-V inputs to the device, enable the I/O clamp diode to prevent V_I from rising above 4.0 V.

(2) When V_{CCIO} = 1.8 V, a MAX II device can drive a 1.5-V device with 1.8-V tolerant inputs.

(3) When V_{CCIO} = 2.5 V, a MAX II device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.

(4) When V_{CCIO} = 3.3 V and a 2.5-V input signal feeds an input pin, the VCCIO supply current will be slightly larger than expected.

(5) MAX II devices can be 5.0-V tolerant with the use of an external resistor and the internal I/O clamp diode on the EPM1270 and EPM2210 devices.

(6) When V_{CCIO} = 3.3 V, a MAX II device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

(7) When V_{CCIO} = 3.3 V, a MAX II device can drive a device with 5.0-V TTL inputs but not 5.0-V CMOS inputs. In the case of 5.0-V CMOS, open-drain setting with internal I/O clamp diode (available only on EPM1270 and EPM2210 devices) and external resistor is required.

For information about output pin source and sink current guidelines, refer to the *AN 428: MAX II CPLD Design Guidelines*.

Referenced Documents

This chapter referenced the following documents:

- *AN 428: MAX II CPLD Design Guidelines*
- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *Hot Socketing and Power-On Reset in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Using User Flash Memory in MAX II Devices* chapter in the *MAX II Device Handbook*

Table 3–1. MAX II JTAG Instructions (Part 2 of 2)

JTAG Instruction	Instruction Code	Description
`CLAMP` *(1)*	`00 0000 1010`	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the boundary scan test data to pass synchronously through selected devices to adjacent devices during normal device operation, while holding I/O pins to a state defined by the data in the boundary-scan register.
`USER0`	`00 0000 1100`	This instruction allows you to define the scan chain between `TDI` and `TDO` in the MAX II logic array. This instruction is also used for custom logic and JTAG interfaces.
`USER1`	`00 0000 1110`	This instruction allows you to define the scan chain between `TDI` and `TDO` in the MAX II logic array. This instruction is also used for custom logic and JTAG interfaces.
`IEEE 1532 instructions`	*(2)*	IEEE 1532 ISC instructions used when programming a MAX II device via the JTAG port.

Notes to Table 3–1:

(1) `HIGHZ`, `CLAMP`, and `EXTEST` instructions do not disable weak pull-up resistors or bus hold features.

(2) These instructions are shown in the 1532 BSDL files, which will be posted on the Altera® website at www.altera.com when they are available.

Unsupported JTAG instructions should not be issued to the MAX II device as this may put the device into an unknown state, requiring a power cycle to recover device operation.

The MAX II device instruction register length is 10 bits and the `USERCODE` register length is 32 bits. Table 3–2 and Table 3–3 show the boundary-scan register length and device `IDCODE` information for MAX II devices.

Table 3–2. MAX II Boundary-Scan Register Length

Device	Boundary-Scan Register Length
EPM240	240
EPM570	480
EPM1270	636
EPM2210	816

Table 3–3. 32-Bit MAX II Device IDCODE (Part 1 of 2)

	Binary IDCODE (32 Bits) *(1)*				
Device	Version (4 Bits)	Part Number	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*	HEX IDCODE
EPM240 EPM240G	`0000`	`0010 0000 1010 0001`	`000 0110 1110`	1	0x020A10DD
EPM570 EPM570G	`0000`	`0010 0000 1010 0010`	`000 0110 1110`	1	0x020A20DD
EPM1270 EPM1270G	`0000`	`0010 0000 1010 0011`	`000 0110 1110`	1	0x020A30DD
EPM2210 EPM2210G	`0000`	`0010 0000 1010 0100`	`000 0110 1110`	1	0x020A40DD

IEEE 1532 Support

The JTAG circuitry and ISP instruction set in MAX II devices is compliant to the IEEE 1532-2002 programming specification. This provides industry-standard hardware and software for in-system programming among multiple vendor programmable logic devices (PLDs) in a JTAG chain.

The MAX II 1532 BSDL files will be released on the Altera website when available.

Jam Standard Test and Programming Language (STAPL)

The Jam STAPL JEDEC standard, JESD71, can be used to program MAX II devices with in-circuit testers, PCs, or embedded processors. The Jam byte code is also supported for MAX II devices. These software programming protocols provide a compact embedded solution for programming MAX II devices.

For more information, refer to the *Using Jam STAPL for ISP via an Embedded Processor* chapter in the *MAX II Device Handbook*.

Programming Sequence

During in-system programming, 1532 instructions, addresses, and data are shifted into the MAX II device through the `TDI` input pin. Data is shifted out through the `TDO` output pin and compared against the expected data. Programming a pattern into the device requires the following six ISP steps. A stand-alone verification of a programmed pattern involves only stages 1, 2, 5, and 6. These steps are automatically executed by third-party programmers, the Quartus II software, or the Jam STAPL and Jam Byte-Code Players.

1. *Enter ISP*—The enter ISP stage ensures that the I/O pins transition smoothly from user mode to ISP mode.
2. *Check ID*—Before any program or verify process, the silicon ID is checked. The time required to read this silicon ID is relatively small compared to the overall programming time.
3. *Sector Erase*—Erasing the device in-system involves shifting in the instruction to erase the device and applying an erase pulse(s). The erase pulse is automatically generated internally by waiting in the run/test/idle state for the specified erase pulse time of 500 ms for the CFM block and 500 ms for each sector of the UFM block.
4. *Program*—Programming the device in-system involves shifting in the address, data, and program instruction and generating the program pulse to program the flash cells. The program pulse is automatically generated internally by waiting in the run/test/idle state for the specified program pulse time of 75 µs. This process is repeated for each address in the CFM and UFM blocks.
5. *Verify*—Verifying a MAX II device in-system involves shifting in addresses, applying the verify instruction to generate the read pulse, and shifting out the data for comparison. This process is repeated for each CFM and UFM address.
6. *Exit ISP*—An exit ISP stage ensures that the I/O pins transition smoothly from ISP mode to user mode.

Real-Time ISP

For systems that require more than DC logic level control of I/O pins, the real-time ISP feature allows you to update the CFM block with a new design image while the current design continues to operate in the SRAM logic array and I/O pins. A new programming file is updated into the MAX II device without halting the original design's operation, saving down-time costs for remote or field upgrades. The updated CFM block configures the new design into the SRAM upon the next power cycle. It is also possible to execute an immediate configuration of the SRAM without a power cycle by using a specific sequence of ISP commands. The configuration of SRAM without a power cycle takes a specific amount of time (t_{CONFIG}). During this time, the I/O pins are tri-stated and weakly pulled-up to V_{CCIO}.

Design Security

All MAX II devices contain a programmable security bit that controls access to the data programmed into the CFM block. When this bit is programmed, design programming information, stored in the CFM block, cannot be copied or retrieved. This feature provides a high level of design security because programmed data within flash memory cells is invisible. The security bit that controls this function, as well as all other programmed data, is reset only when the device is erased. The SRAM is also invisible and cannot be accessed regardless of the security bit setting. The UFM block data is not protected by the security bit and is accessible through JTAG or logic array connections.

Programming with External Hardware

MAX II devices can be programmed by downloading the information via in-circuit testers, embedded processors, the Altera® ByteblasterMV™, MasterBlaster™, ByteBlaster™ II, and USB-Blaster cables.

BP Microsystems, System General, and other programming hardware manufacturers provide programming support for Altera devices. Check their websites for device support information.

Referenced Documents

This chapter references the following documents:

- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *IEEE 1149.1 (JTAG) Boundary-Scan Testing for MAX II Devices* chapter in the *MAX II Device Handbook*
- *Real-Time ISP and ISP Clamp for MAX II Devices* chapter in the *MAX II Device Handbook*
- *Using Jam STAPL for ISP via an Embedded Processor* chapter in the *MAX II Device Handbook*

4. Hot Socketing and Power-On Reset in MAX II Devices

MII51004-2.1

Introduction

MAX® II devices offer hot socketing, also known as hot plug-in or hot swap, and power sequencing support. Designers can insert or remove a MAX II board in a system during operation without undesirable effects to the system bus. The hot socketing feature removes some of the difficulties designers face when using components on printed circuit boards (PCBs) that contain a mixture of 3.3-, 2.5-, 1.8-, and 1.5-V devices.

The MAX II device hot socketing feature provides:

- Board or device insertion and removal
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter contains the following sections:

- "MAX II Hot-Socketing Specifications" on page 4–1
- "Power-On Reset Circuitry" on page 4–5

MAX II Hot-Socketing Specifications

MAX II devices offer all three of the features required for the hot-socketing capability listed above without any external components or special design requirements. The following are hot-socketing specifications:

- The device can be driven before and during power-up or power-down without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.
- Signal pins do not drive the V_{CCIO} or V_{CCINT} power supplies. External input signals to device I/O pins do not power the device V_{CCIO} or V_{CCINT} power supplies via internal paths. This is true if the V_{CCINT} and the V_{CCIO} supplies are held at GND.

☞ Altera uses `GND` as reference for the hot-socketing and I/O buffers circuitry designs. You must connect the `GND` between boards before connecting the V_{CCINT} and the V_{CCIO} power supplies to ensure device reliability and compliance to the hot-socketing specifications.

Devices Can Be Driven before Power-Up

Signals can be driven into the MAX II device I/O pins and `GCLK[3..0]` pins before or during power-up or power-down without damaging the device. MAX II devices support any power-up or power-down sequence (V_{CCIO1}, V_{CCIO2}, V_{CCIO3}, V_{CCIO4}, V_{CCINT}), simplifying the system-level design.

I/O Pins Remain Tri-Stated during Power-Up

A device that does not support hot-socketing may interrupt system operation or cause contention by driving out before or during power-up. In a hot socketing situation, the MAX II device's output buffers are turned off during system power-up. MAX II devices do not drive out until the device attains proper operating conditions and is fully configured. Refer to "Power-On Reset Circuitry" on page 4–5 for information about turn-on voltages.

Signal Pins Do Not Drive the V_{CCIO} or V_{CCINT} Power Supplies

MAX II devices do not have a current path from I/O pins or `GCLK[3..0]` pins to the V_{CCIO} or V_{CCINT} pins before or during power-up. A MAX II device may be inserted into (or removed from) a system board that was powered up without damaging or interfering with system-board operation. When hot socketing, MAX II devices may have a minimal effect on the signal integrity of the backplane.

AC and DC Specifications

You can power up or power down the V_{CCIO} and V_{CCINT} pins in any sequence. During hot socketing, the I/O pin capacitance is less than 8 pF. MAX II devices meet the following hot socketing specifications:

- The hot socketing DC specification is: $| I_{IOPIN} | < 300\ \mu A$.
- The hot socketing AC specification is: $| I_{IOPIN} | < 8$ mA for 10 ns or less.

MAX II devices are immune to latch-up when hot socketing. If the `TCK` JTAG input pin is driven high during hot socketing, the current on that pin might exceed the specifications above.

I_{IOPIN} is the current at any user I/O pin on the device. The AC specification applies when the device is being powered up or powered down. This specification takes into account the pin capacitance but not board trace and external loading capacitance. Additional capacitance for trace, connector, and loading must be taken into consideration separately. The peak current duration due to power-up transients is 10 ns or less.

The DC specification applies when all V_{CC} supplies to the device are stable in the powered-up or powered-down conditions.

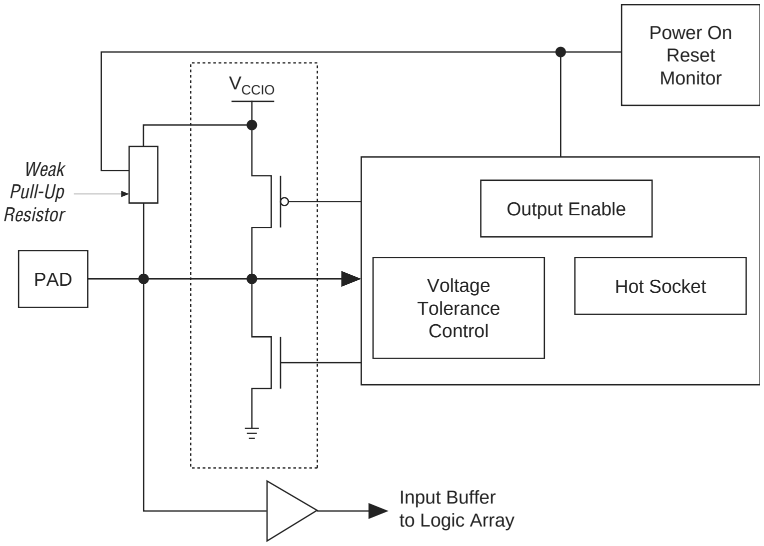
Hot Socketing Feature Implementation in MAX II Devices

The hot socketing feature turns off (tri-states) the output buffer during the power-up event (either V_{CCINT} or V_{CCIO} supplies) or power-down event. The hot-socket circuit generates an internal `HOTSCKT` signal when either V_{CCINT} or V_{CCIO} is below the threshold voltage during power-up or power-down. The `HOTSCKT` signal cuts off the output buffer to make sure that no DC current (except for weak pull-up leaking) leaks through the pin. When V_{CC} ramps up very slowly during power-up, V_{CC} may still be relatively low even after the power-on reset (POR) signal is released and device configuration is complete.

Make sure that the V_{CCINT} is within the recommended operating range even though SRAM download has completed.

Each I/O and clock pin has the circuitry shown in Figure 4–1.

Figure 4–1. Hot Socketing Circuit Block Diagram for MAX II Devices



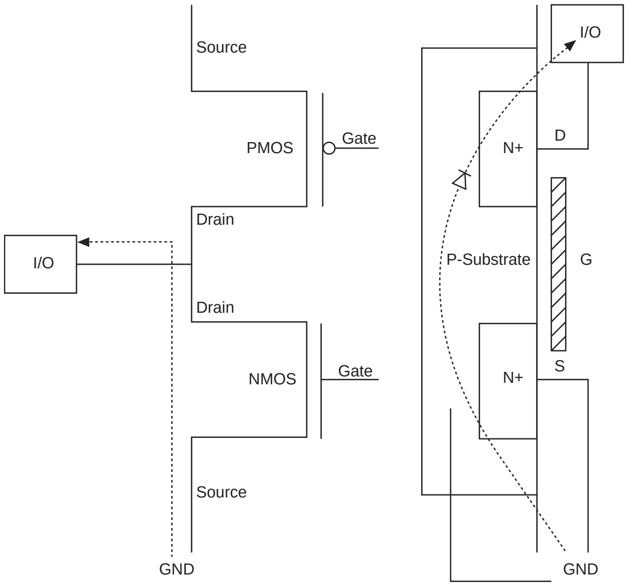
The POR circuit monitors V_{CCINT} and V_{CCIO} voltage levels and keeps I/O pins tri-stated until the device has completed its flash memory configuration of the SRAM logic. The weak pull-up resistor (R) from the I/O pin to V_{CCIO} is enabled during download to keep the I/O pins from floating. The 3.3-V tolerance control circuit permits the I/O pins to be driven by 3.3 V before V_{CCIO} and/or V_{CCINT} are powered, and it prevents the I/O pins from driving out when the device is not fully powered or operational. The hot socket circuit prevents I/O pins from internally powering V_{CCIO} and V_{CCINT} when driven by external signals before the device is powered.

For information about 5.0-V tolerance, refer to the *Using MAX II Devices in Multi-Voltage Systems* chapter in the *MAX II Device Handbook*.

Figure 4–2 shows a transistor-level cross section of the MAX II device I/O buffers. This design ensures that the output buffers do not drive when V_{CCIO} is powered before V_{CCINT} or if the I/O pad voltage is higher than V_{CCIO}. This also applies for sudden voltage spikes during hot insertion. The V_{PAD} leakage current charges the 3.3-V tolerant circuit capacitance.

When the I/O pin receives a negative ESD zap at the pin that is less than –0.7 V (0.7 V is the voltage drop across a diode), the intrinsic P-Substrate/N+ drain diode is forward biased. Therefore, the discharge ESD current path is from GND to the I/O pin, as shown in Figure 4–4.

Figure 4–4. ESD Protection During Negative Voltage Zap



Power-On Reset Circuitry

MAX II devices have POR circuits to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up. The POR circuit monitors these voltages, triggering download from the non-volatile configuration flash memory (CFM) block to the SRAM logic, maintaining tri-state of the I/O pins (with weak pull-up resistors enabled) before and during this process. When the MAX II device enters user mode, the POR circuit releases the I/O pins to user functionality. The POR circuit of the MAX II (except MAX IIZ) device continues to monitor the V_{CCINT} voltage level to detect a brown-out condition. The POR circuit of the MAX IIZ device does not monitor the V_{CCINT} voltage level after the device enters into user mode. More details are provided in the following sub-sections.

Programming/Erasure Specifications

Table 5–3 shows the MAX II device family programming/erasure specifications.

Table 5–3. MAX II Device Programming/Erasure Specifications

Parameter	Minimum	Typical	Maximum	Unit
Erase and reprogram cycles	—	—	100 *(1)*	Cycles

Note to Table 5–3:

(1) This specification applies to the UFM and configuration flash memory (CFM) blocks.

DC Electrical Characteristics

Table 5–4 shows the MAX II device family DC electrical characteristics.

Table 5–4. MAX II Device DC Electrical Characteristics *(Note 1)* (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIO}$max to 0 V *(2)*	–10	—	10	µA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIO}$max to 0 V *(2)*	–10	—	10	µA
$I_{CCSTANDBY}$	V_{CCINT} supply current (standby) *(3)*	MAX II devices	—	12	—	mA
		MAX IIG devices	—	2	—	mA
		EPM240Z (Commercial grade) *(4)*	—	25	90	µA
		EPM240Z (Industrial grade) *(5)*	—	25	139	µA
		EPM570Z (Commercial grade) *(4)*	—	27	96	µA
		EPM570Z (Industrial grade) *(5)*	—	27	152	µA
$V_{SCHMITT}$ *(6)*	Hysteresis for Schmitt trigger input *(7)*	V_{CCIO} = 3.3 V	—	400	—	mV
		V_{CCIO} = 2.5 V	—	190	—	mV
$I_{CCPOWERUP}$	V_{CCINT} supply current during power-up *(8)*	MAX II devices	—	55	—	mA
		MAX IIG and MAX IIZ devices	—	40	—	mA
R_{PULLUP}	Value of I/O pin pull-up resistor during user mode and in-system programming	V_{CCIO} = 3.3 V *(9)*	5	—	25	kΩ
		V_{CCIO} = 2.5 V *(9)*	10	—	40	kΩ
		V_{CCIO} = 1.8 V *(9)*	25	—	60	kΩ
		V_{CCIO} = 1.5 V *(9)*	45	—	95	kΩ

Table 5–13. MAX II Device Timing Model Status (Part 2 of 2)

Device	Preliminary	Final
EPM1270	—	✓
EPM2210	—	✓

Note to Table 5–13:

(1) The MAX IIZ device timing models are only available in the Quartus II software version 8.0 and later.

Performance

Table 5–14 shows the MAX II device performance for some common designs. All performance values were obtained with the Quartus II software compilation of megafunctions. Performance values for –3, –4, and –5 speed grades are based on an EPM1270 device target, while –6, –7, and –8 speed grades are based on an EPM570Z device target.

Table 5–14. MAX II Device Performance

Resource Used	Design Size and Function	Resources Used			Performance						Unit
					MAX II / MAX IIG			MAX IIZ			
		Mode	LEs	UFM Blocks	–3 Speed Grade	–4 Speed Grade	–5 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	
LE	16-bit counter *(1)*	—	16	0	304.0	247.5	201.1	184.1	123.5	118.3	MHz
	64-bit counter *(1)*	—	64	0	201.5	154.8	125.8	83.2	83.2	80.5	MHz
	16-to-1 multiplexer	—	11	0	6.0	8.0	9.3	17.4	17.3	20.4	ns
	32-to-1 multiplexer	—	24	0	7.1	9.0	11.4	12.5	22.8	25.3	ns
	16-bit XOR function	—	5	0	5.1	6.6	8.2	9.0	15.0	16.1	ns
	16-bit decoder with single address line	—	5	0	5.2	6.6	8.2	9.2	15.0	16.1	ns
UFM	512 × 16	None	3	1	10.0	10.0	10.0	10.0	10.0	10.0	MHz
	512 × 16	SPI *(2)*	37	1	8.0	8.0	8.0	9.7	9.7	9.7	MHz
	512 × 8	Parallel *(3)*	73	1	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	*(4)*	MHz
	512 × 16	I²C *(3)*	142	1	100 *(5)*	100 *(5)*	100 *(5)*	100 *(5)*	100 *(5)*	100 *(5)*	kHz

Notes to Table 5–14:

(1) This design is a binary loadable up counter.

(2) This design is configured for read-only operation in Extended mode. Read and write ability increases the number of LEs used.

(3) This design is configured for read-only operation. Read and write ability increases the number of LEs used.

(4) This design is asynchronous.

(5) The I²C megafunction is verified in hardware up to 100-kHz serial clock line (SCL) rate.

Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Table 5–15 through Table 5–22 describe the MAX II device internal timing microparameters for logic elements (LEs), input/output elements (IOEs), UFM blocks, and MultiTrack interconnects. The timing values for –3, –4, and –5 speed grades shown in Table 5–15 through Table 5–22 are based on an EPM1270 device target, while –6, –7, and –8 speed grade values are based on an EPM570Z device target.

For more explanations and descriptions about each internal timing microparameters symbol, refer to the *Understanding Timing in MAX II Devices* chapter in the *MAX II Device Handbook*.

Table 5–15. LE Internal Timing Microparameters

		MAX II / MAX IIG						**MAX IIZ**						
		–3 Speed Grade		**–4 Speed Grade**		**–5 Speed Grade**		**–6 Speed Grade**		**–7 Speed Grade**		**–8 Speed Grade**		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LUT}	LE combinational LUT delay	—	571	—	742	—	914	—	1,215	—	2,247	—	2,247	ps
t_{COMB}	Combinational path delay	—	147	—	192	—	236	—	243	—	305	—	309	ps
t_{CLR}	LE register clear delay	238	—	309	—	381	—	401	—	541	—	545	—	ps
t_{PRE}	LE register preset delay	238	—	309	—	381	—	401	—	541	—	545	—	ps
t_{SU}	LE register setup time before clock	208	—	271	—	333	—	260	—	319	—	321	—	ps
t_{H}	LE register hold time after clock	0	—	0	—	0	—	0	—	0	—	0	—	ps
t_{CO}	LE register clock-to-output delay	—	235	—	305	—	376	—	380	—	489	—	494	ps
t_{CLKHL}	Minimum clock high or low time	166	—	216	—	266	—	253	—	335	—	339	—	ps
t_{C}	Register control delay	—	857	—	1,114	—	1,372	—	1,356	—	1,722	—	1,741	ps

Table 5–21. UFM Block Internal Timing Microparameters (Part 3 of 3)

		MAX II / MAX IIG						MAX IIZ						
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
Symbol	**Parameter**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{OE}	Delay from data register clock to data register output	180	—	180	—	180	—	180	—	180	—	180	—	ns
t_{RA}	Maximum read access time	—	65	—	65	—	65	—	65	—	65	—	65	ns
t_{OSCS}	Maximum delay between the `OSC_ENA` rising edge to the erase/program signal rising edge	250	—	250	—	250	—	250	—	250	—	250	—	ns
t_{OSCH}	Minimum delay allowed from the erase/program signal going low to `OSC_ENA` signal going low	250	—	250	—	250	—	250	—	250	—	250	—	ns

Figure 5–3 through Figure 5–5 show the read, program, and erase waveforms for UFM block timing parameters shown in Table 5–21.

Figure 5–3. UFM Read Waveforms

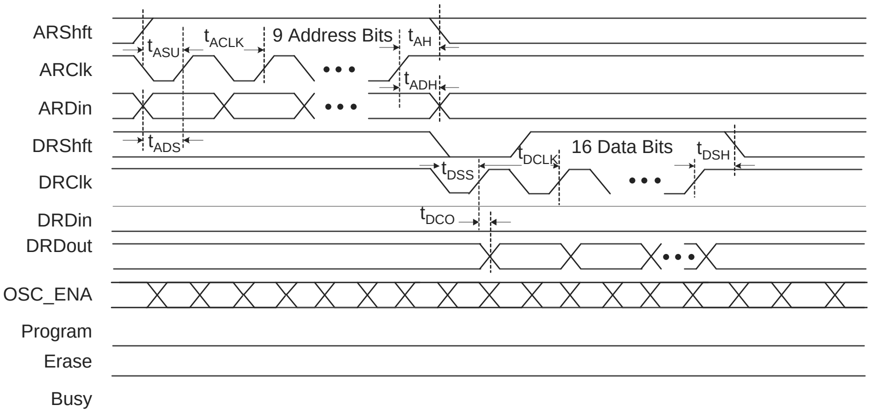


Table 5–27. External Timing Input Delay Adders (Part 2 of 2)

I/O Standard		**MAX II / MAX IIG**						**MAX IIZ**						**Unit**
		–3 Speed Grade		**–4 Speed Grade**		**–5 Speed Grade**		**–6 Speed Grade**		**–7 Speed Grade**		**–8 Speed Grade**		
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
3.3-V LVCMOS	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	334	—	434	—	535	—	387	—	434	—	442	ps
2.5-V LVTTL / LVCMOS	Without Schmitt Trigger	—	23	—	30	—	37	—	42	—	43	—	43	ps
	With Schmitt Trigger	—	339	—	441	—	543	—	429	—	476	—	483	ps
1.8-V LVTTL / LVCMOS	Without Schmitt Trigger	—	291	—	378	—	466	—	378	—	373	—	373	ps
1.5-V LVCMOS	Without Schmitt Trigger	—	681	—	885	—	1,090	—	681	—	622	—	658	ps
3.3-V PCI	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	—	0	ps

Table 5–28. External Timing Input Delay t_{GLOB} Adders for GCLK Pins

I/O Standard		**MAX II / MAX IIG**						**MAX IIZ**						**Unit**
		–3 Speed Grade		**–4 Speed Grade**		**–5 Speed Grade**		**–6 Speed Grade**		**–7 Speed Grade**		**–8 Speed Grade**		
		Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
3.3-V LVTTL	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	308	—	400	—	493	—	387	—	434	—	442	ps
3.3-V LVCMOS	Without Schmitt Trigger	—	0	—	0	—	0	—	0	—	0	—	0	ps
	With Schmitt Trigger	—	308	—	400	—	493	—	387	—	434	—	442	ps
2.5-V LVTTL / LVCMOS	Without Schmitt Trigger	—	21	—	27	—	33	—	42	—	43	—	43	ps
	With Schmitt Trigger	—	423	—	550	—	677	—	429	—	476	—	483	ps
1.8-V LVTTL / LVCMOS	Without Schmitt Trigger	—	353	—	459	—	565	—	378	—	373	—	373	ps
1.5-V LVCMOS	Without Schmitt Trigger	—	855	—	1,111	—	1,368	—	681	—	622	—	658	ps
3.3-V PCI	Without Schmitt Trigger	—	6	—	7	—	9	—	0	—	0	—	0	ps

Table 5–29. External Timing Output Delay and t_{OD} Adders for Fast Slew Rate

I/O Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	8 mA	—	65	—	84	—	104	—	–6	—	–2	—	–3	ps
3.3-V LVCMOS	8 mA	—	0	—	0	—	0	—	0	—	0	—	0	ps
	4 mA	—	65	—	84	—	104	—	–6	—	–2	—	–3	ps
2.5-V LVTTL / LVCMOS	14 mA	—	122	—	158	—	195	—	–63	—	–71	—	–88	ps
	7 mA	—	193	—	251	—	309	—	10	—	–1	—	1	ps
1.8-V LVTTL / LVCMOS	6 mA	—	568	—	738	—	909	—	128	—	118	—	118	ps
	3 mA	—	654	—	850	—	1,046	—	352	—	327	—	332	ps
1.5-V LVCMOS	4 mA	—	1,059	—	1,376	—	1,694	—	421	—	400	—	400	ps
	2 mA	—	1,167	—	1,517	—	1,867	—	757	—	743	—	743	ps
3.3-V PCI	20 mA	—	3	—	4	—	5	—	–6	—	–2	—	–3	ps

Table 5–30. External Timing Output Delay and t_{OD} Adders for Slow Slew Rate

I/O Standard		MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
3.3-V LVTTL	16 mA	—	7,064	—	6,745	—	6,426	—	5,966	—	5,992	—	6,118	ps
	8 mA	—	7,946	—	7,627	—	7,308	—	6,541	—	6,570	—	6,720	ps
3.3-V LVCMOS	8 mA	—	7,064	—	6,745	—	6,426	—	5,966	—	5,992	—	6,118	ps
	4 mA	—	7,946	—	7,627	—	7,308	—	6,541	—	6,570	—	6,720	ps
2.5-V LVTTL / LVCMOS	14 mA	—	10,434	—	10,115	—	9,796	—	9,141	—	9,154	—	9,297	ps
	7 mA	—	11,548	—	11,229	—	10,910	—	9,861	—	9,874	—	10,037	ps
1.8-V LVTTL / LVCMOS	6 mA	—	22,927	—	22,608	—	22,289	—	21,811	—	21,854	—	21,857	ps
	3 mA	—	24,731	—	24,412	—	24,093	—	23,081	—	23,034	—	23,107	ps
1.5-V LVCMOS	4 mA	—	38,723	—	38,404	—	38,085	—	39,121	—	39,124	—	39,124	ps
	2 mA	—	41,330	—	41,011	—	40,692	—	40,631	—	40,634	—	40,634	ps
3.3-V PCI	20 mA	—	261	—	339	—	418	—	6,644	—	6,627	—	6,914	ps