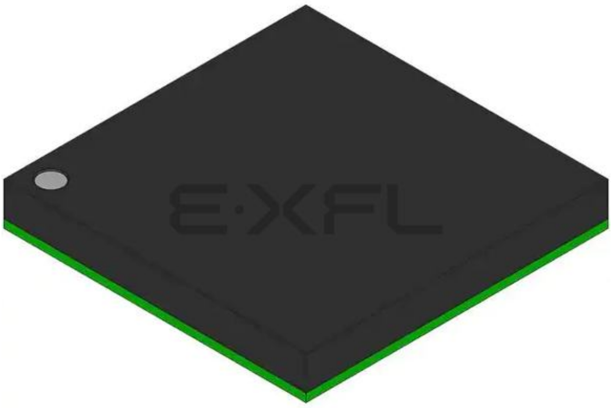

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Understanding Embedded - CPLDs (Complex Programmable Logic Devices)

Embedded - CPLDs, or Complex Programmable Logic Devices, are highly versatile digital logic devices used in electronic systems. These programmable components are designed to perform complex logical operations and can be customized for specific applications. Unlike fixed-function ICs, CPLDs offer the flexibility to reprogram their configuration, making them an ideal choice for various embedded systems. They consist of a set of logic gates and programmable interconnects, allowing designers to implement complex logic circuits without needing custom hardware.

Applications of Embedded - CPLDs

Details	
Product Status	Active
Programmable Type	In System Programmable
Delay Time tpd(1) Max	9 ns
Voltage Supply - Internal	1.71V ~ 1.89V
Number of Logic Elements/Blocks	570
Number of Macrocells	440
Number of Gates	-
Number of I/O	116
Operating Temperature	0°C ~ 85°C (TJ)
Mounting Type	Surface Mount
Package / Case	144-TFBGA
Supplier Device Package	144-MBGA (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=epm570zm144c7n

MAX II devices are available in space-saving FineLine BGA, Micro FineLine BGA, and thin quad flat pack (TQFP) packages (refer to Table 1–3 and Table 1–4). MAX II devices support vertical migration within the same package (for example, you can migrate between the EPM570, EPM1270, and EPM2210 devices in the 256-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins and JTAG pins are the same and power pins are subsets or supersets for a given package across device densities. The largest density in any package has the highest number of power pins; you must lay out for the largest planned density in a package to provide the necessary power pins for migration. For I/O pin migration across densities, cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins can be migrated. The Quartus® II software can automatically cross-reference and place all pins for you when given a device migration list.

Table 1–3. MAX II Packages and User I/O Pins

Device	68-Pin Micro FineLine BGA *(1)*	100-Pin Micro FineLine BGA *(1)*	100-Pin FineLine BGA	100-Pin TQFP	144-Pin TQFP	144-Pin Micro FineLine BGA *(1)*	256-Pin Micro FineLine BGA *(1)*	256-Pin FineLine BGA	324-Pin FineLine BGA
EPM240 EPM240G	—	80	80	80	—	—	—	—	—
EPM570 EPM570G	—	76	76	76	116	—	160	160	—
EPM1270 EPM1270G	—	—	—	—	116	—	212	212	—
EPM2210 EPM2210G	—	—	—	—	—	—	—	204	272
EPM240Z	54	80	—	—	—	—	—	—	—
EPM570Z	—	76	—	—	—	116	160	—	—

Note to Table 1–3:

(1) Packages available in lead-free versions only.

Table 1–4. MAX II TQFP, FineLine BGA, and Micro FineLine BGA Package Sizes

Package	68-Pin Micro FineLine BGA	100-Pin Micro FineLine BGA	100-Pin FineLine BGA	100-Pin TQFP	144-Pin TQFP	144-Pin Micro FineLine BGA	256-Pin Micro FineLine BGA	256-Pin FineLine BGA	324-Pin FineLine BGA
Pitch (mm)	0.5	0.5	1	0.5	0.5	0.5	0.5	1	1
Area (mm2)	25	36	121	256	484	49	121	289	361
Length × width (mm × mm)	5 × 5	6 × 6	11 × 11	16 × 16	22 × 22	7 × 7	11 × 11	17 × 17	19 × 19

MAX II devices have an internal linear voltage regulator which supports external supply voltages of 3.3 V or 2.5 V, regulating the supply down to the internal operating voltage of 1.8 V. MAX IIG and MAX IIZ devices only accept 1.8 V as the external supply voltage. MAX IIZ devices are pin-compatible with MAX IIG devices in the 100-pin Micro FineLine BGA and 256-pin Micro FineLine BGA packages. Except for external supply voltage requirements, MAX II and MAX II G devices have identical pin-outs and timing specifications. Table 1–5 shows the external supply voltages supported by the MAX II family.

Table 1–5. MAX II External Supply Voltages

Devices	EPM240 EPM570 EPM1270 EPM2210	EPM240G EPM570G EPM1270G EPM2210G EPM240Z EPM570Z *(1)*
MultiVolt core external supply voltage (V_{CCINT}) *(2)*	3.3 V, 2.5 V	1.8 V
MultiVolt I/O interface voltage levels (V_{CCIO})	1.5 V, 1.8 V, 2.5 V, 3.3 V	1.5 V, 1.8 V, 2.5 V, 3.3 V

Notes to Table 1–5:

(1) MAX IIG and MAX IIZ devices only accept 1.8 V on their `VCCINT` pins. The 1.8-V V_{CCINT} external supply powers the device core directly.

(2) MAX II devices operate internally at 1.8 V.

Referenced Documents

This chapter references the following documents:

- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *MAX II Logic Element to Macrocell Conversion Methodology* white paper

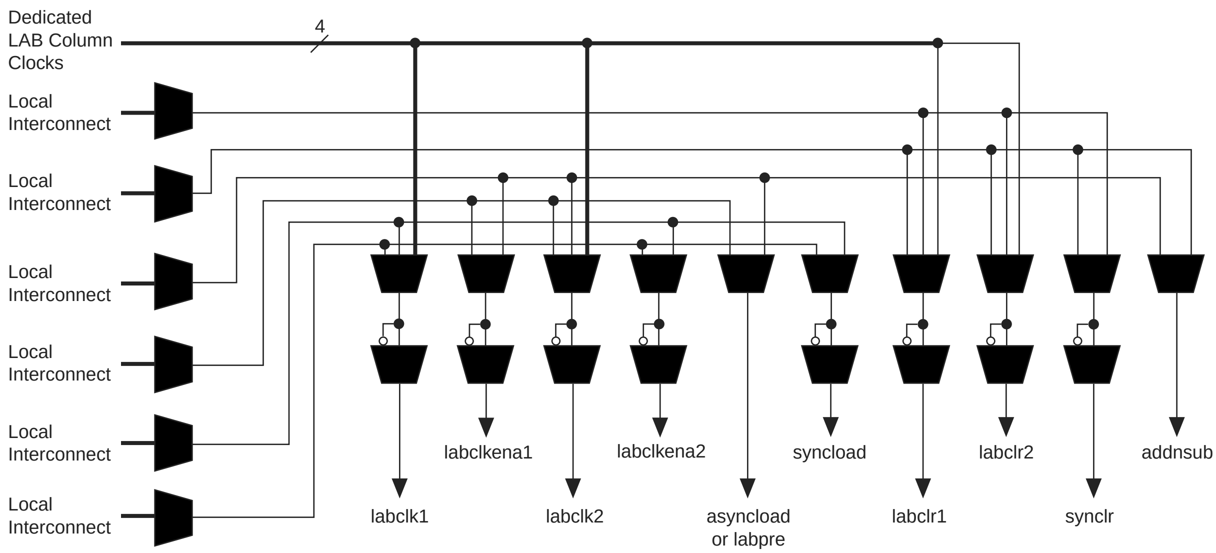
Document Revision History

Table 1–6 shows the revision history for this chapter.

Table 1–6. Document Revision History

Date and Revision	Changes Made	Summary of Changes
August 2009, version 1.9	■ Updated Table 1–2.	Added information for speed grade –8
October 2008, version 1.8	■ Updated “Introduction” section. ■ Updated new Document Format.	—
December 2007, version1.7	■ Updated Table 1–1 through Table 1–5. ■ Added “Referenced Documents” section.	Updated document with MAX IIZ information.
December 2006, version 1.6	■ Added document revision history.	—
August 2006, version 1.5	■ Minor update to features list.	—
July 2006, version 1.4	■ Minor updates to tables.	—

Figure 2–5. LAB-Wide Control Signals

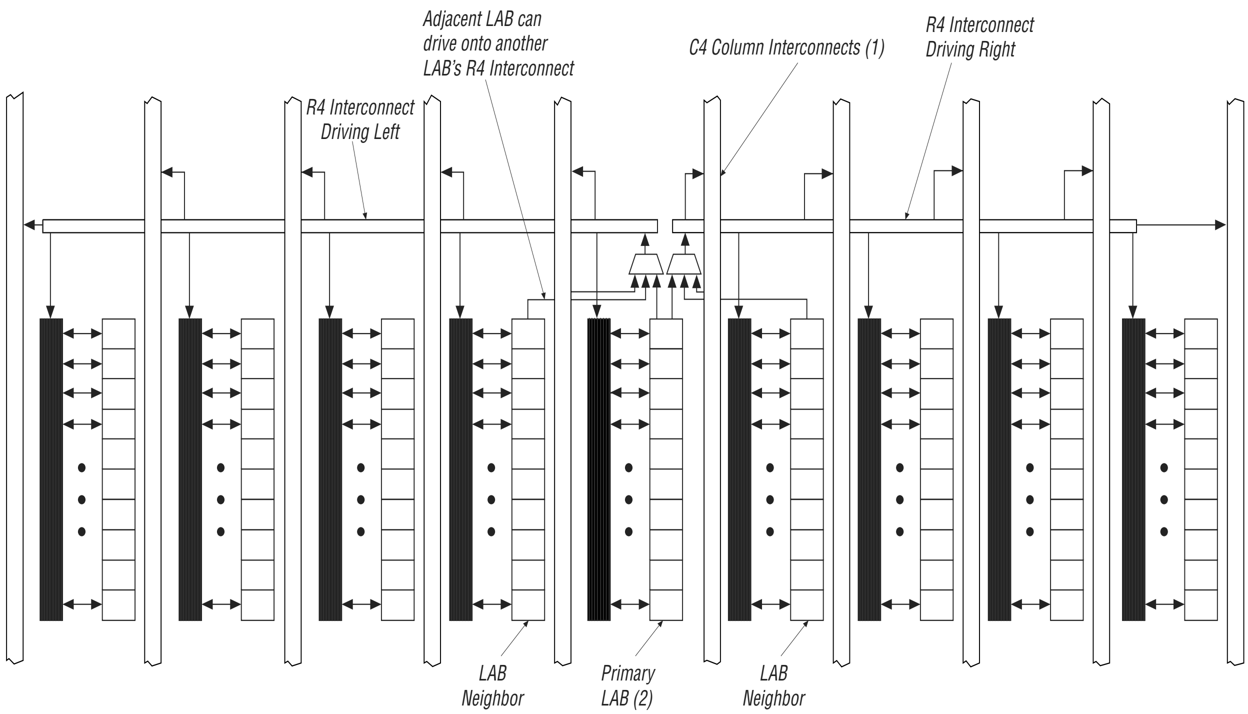


Logic Elements

The smallest unit of logic in the MAX II architecture, the LE, is compact and provides advanced features with efficient logic utilization. Each LE contains a four-input LUT, which is a function generator that can implement any function of four variables. In addition, each LE contains a programmable register and carry chain with carry-select capability. A single LE also supports dynamic single-bit addition or subtraction mode selectable by an LAB-wide control signal. Each LE drives all types of interconnects: local, row, column, LUT chain, register chain, and DirectLink interconnects. See Figure 2–6.

The R4 interconnects span four LABs and are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. Figure 2–10 shows R4 interconnect connections from an LAB. R4 interconnects can drive and be driven by row IOEs. For LAB interfacing, a primary LAB or horizontal LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 interconnects for connections from one row to another.

Figure 2–10. R4 Interconnect Connections



Notes to Figure 2–10:

(1) C4 interconnects can drive R4 interconnects.

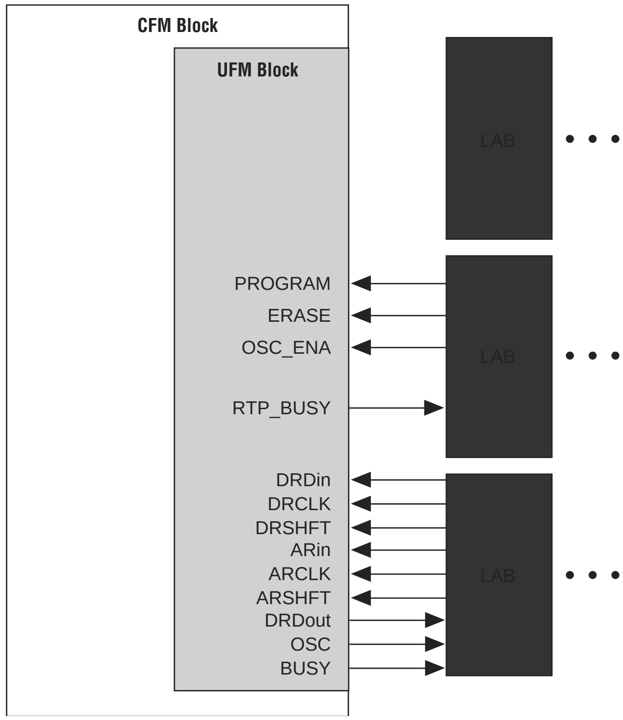
(2) This pattern is repeated for every LAB in the LAB row.

The column interconnect operates similarly to the row interconnect. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs and row and column IOEs. These column resources include:

- LUT chain interconnects within an LAB
- Register chain interconnects within an LAB
- C4 interconnects traversing a distance of four LABs in an up and down direction

MAX II devices include an enhanced interconnect structure within LABs for routing LE output to LE input connections faster using LUT chain connections and register chain connections. The LUT chain connection allows the combinational output of an LE to directly drive the fast input of the LE right below it, bypassing the local interconnect. These resources can be used as a high-speed connection for wide fan-in

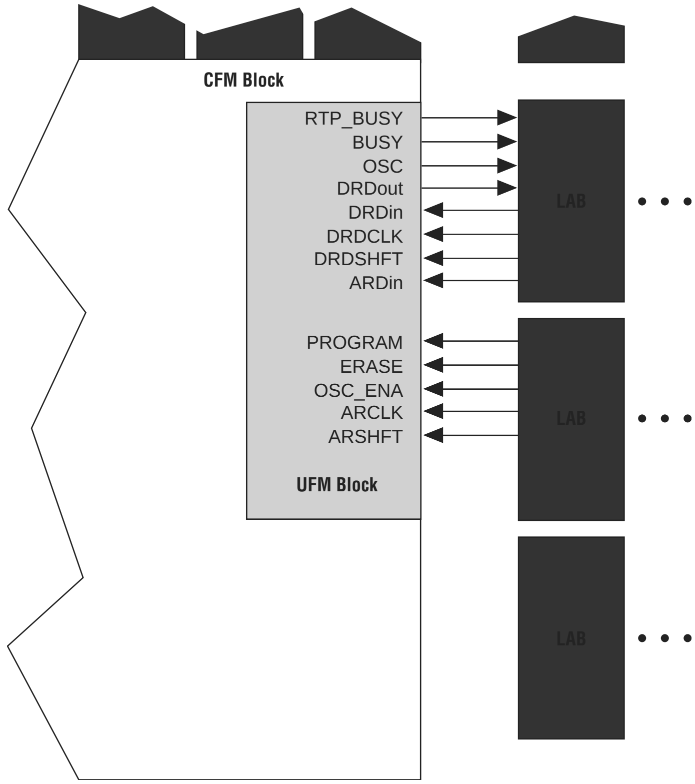
Figure 2–16. EPM240 UFM Block LAB Row Interface *(Note 1)*



Note to Figure 2–16:

(1) The UFM block inputs and outputs can drive to/from all types of interconnects, not only DirectLink interconnects from adjacent row LABs.

Figure 2–17. EPM570, EPM1270, and EPM2210 UFM Block LAB Row Interface

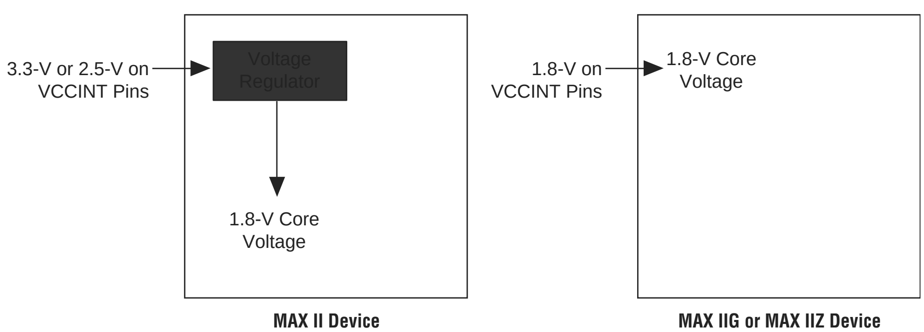


MultiVolt Core

The MAX II architecture supports the MultiVolt core feature, which allows MAX II devices to support multiple V_{CC} levels on the V_{CCINT} supply. An internal linear voltage regulator provides the necessary 1.8-V internal voltage supply to the device. The voltage regulator supports 3.3-V or 2.5-V supplies on its inputs to supply the 1.8-V internal voltage to the device, as shown in Figure 2–18. The voltage regulator is not guaranteed for voltages that are between the maximum recommended 2.5-V operating voltage and the minimum recommended 3.3-V operating voltage.

The MAX IIG and MAX IIZ devices use external 1.8-V supply. The 1.8-V V_{CC} external supply powers the device core directly.

Figure 2–18. MultiVolt Core Feature in MAX II Devices



Bus Hold

Each MAX II device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Since the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. The designer can select this feature individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the device cannot use the programmable pull-up option.

The bus-hold circuitry uses a resistor to pull the signal level to the last driven state. The *DC and Switching Characteristics* chapter in the *MAX II Device Handbook* gives the specific sustaining current for each V_{CCIO} voltage level driven through this resistor and overdrive current used to identify the next-driven input level.

The bus-hold circuitry is only active after the device has fully initialized. The bus-hold circuit captures the value on the pin present at the moment user mode is entered.

Programmable Pull-Up Resistor

Each MAX II device I/O pin provides an optional programmable pull-up resistor during user mode. If the designer enables this feature for an I/O pin, the pull-up resistor holds the output to the V_{CCIO} level of the output pin's bank.

☞ The programmable pull-up resistor feature should not be used at the same time as the bus-hold feature on a given I/O pin.

Programmable Input Delay

The MAX II IOE includes a programmable input delay that is activated to ensure zero hold times. A path where a pin directly drives a register, with minimal routing between the two, may require the delay to ensure zero hold time. However, a path where a pin drives a register through long routing or through combinational logic may not require the delay to achieve a zero hold time. The Quartus II software uses this delay to ensure zero hold times when needed.

MultiVolt I/O Interface

The MAX II architecture supports the MultiVolt I/O interface feature, which allows MAX II devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation (V_{CCINT}), and up to four sets for input buffers and I/O output driver buffers (V_{CCIO}), depending on the number of I/O banks available in the devices where each set of VCC pins powers one I/O bank. The EPM240 and EPM570 devices have two I/O banks respectively while the EPM1270 and EPM2210 devices have four I/O banks respectively.

Connect VCCIO pins to either a 1.5-V, 1.8 V, 2.5-V, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (that is, when VCCIO pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems. Table 2–7 summarizes MAX II MultiVolt I/O support.

Table 2–7. MAX II MultiVolt I/O Support *(Note 1)*

VCCIO (V)	Input Signal					Output Signal				
	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.5	✓	✓	✓	✓	—	✓	—	—	—	—
1.8	✓	✓	✓	✓	—	✓ *(2)*	✓	—	—	—
2.5	—	—	✓	✓	—	✓ *(3)*	✓ *(3)*	✓	—	—
3.3	—	—	✓ *(4)*	✓	✓ *(5)*	✓ *(6)*	✓ *(6)*	✓ *(6)*	✓	✓ *(7)*

Notes to Table 2–7:

(1) To drive inputs higher than V_{CCIO} but less than 4.0 V including the overshoot, disable the I/O clamp diode. However, to drive 5.0-V inputs to the device, enable the I/O clamp diode to prevent V_I from rising above 4.0 V.

(2) When V_{CCIO} = 1.8 V, a MAX II device can drive a 1.5-V device with 1.8-V tolerant inputs.

(3) When V_{CCIO} = 2.5 V, a MAX II device can drive a 1.5-V or 1.8-V device with 2.5-V tolerant inputs.

(4) When V_{CCIO} = 3.3 V and a 2.5-V input signal feeds an input pin, the VCCIO supply current will be slightly larger than expected.

(5) MAX II devices can be 5.0-V tolerant with the use of an external resistor and the internal I/O clamp diode on the EPM1270 and EPM2210 devices.

(6) When V_{CCIO} = 3.3 V, a MAX II device can drive a 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.

(7) When V_{CCIO} = 3.3 V, a MAX II device can drive a device with 5.0-V TTL inputs but not 5.0-V CMOS inputs. In the case of 5.0-V CMOS, open-drain setting with internal I/O clamp diode (available only on EPM1270 and EPM2210 devices) and external resistor is required.

For information about output pin source and sink current guidelines, refer to the *AN 428: MAX II CPLD Design Guidelines*.

Referenced Documents

This chapter referenced the following documents:

- *AN 428: MAX II CPLD Design Guidelines*
- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *Hot Socketing and Power-On Reset in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Using User Flash Memory in MAX II Devices* chapter in the *MAX II Device Handbook*

3. JTAG and In-System Programmability

MII51003-1.6

Introduction

This chapter discusses how to use the IEEE Standard 1149.1 Boundary-Scan Test (BST) circuitry in MAX II devices and includes the following sections:

- "IEEE Std. 1149.1 (JTAG) Boundary-Scan Support" on page 3–1
- "In System Programmability" on page 3–4

IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All MAX® II devices provide Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry that complies with the IEEE Std. 1149.1-2001 specification. JTAG boundary-scan testing can only be performed at any time after V_{CCINT} and all V_{CCIO} banks have been fully powered and a t_{CONFIG} amount of time has passed. MAX II devices can also use the JTAG port for in-system programming together with either the Quartus® II software or hardware using Programming Object Files (**.pof**), JamTM Standard Test and Programming Language (STAPL) Files (**.jam**), or Jam Byte-Code Files (**.jbc**).

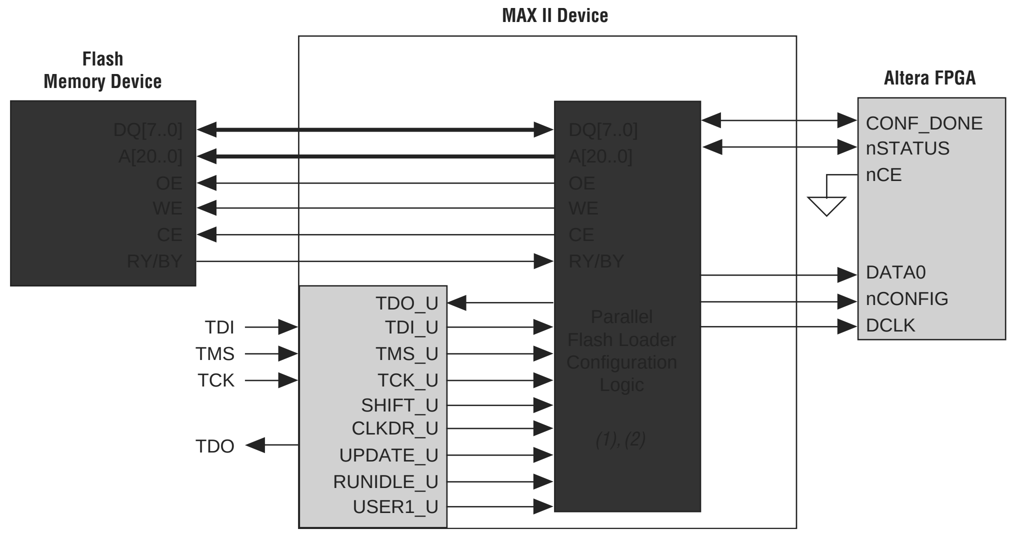
The JTAG pins support 1.5-V, 1.8-V, 2.5-V, or 3.3-V I/O standards. The supported voltage level and standard are determined by the V_{CCIO} of the bank where it resides. The dedicated JTAG pins reside in Bank 1 of all MAX II devices.

MAX II devices support the JTAG instructions shown in Table 3–1.

Table 3–1. MAX II JTAG Instructions (Part 1 of 2)

JTAG Instruction	Instruction Code	Description
`SAMPLE/PRELOAD`	`00 0000 0101`	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins.
`EXTEST` *(1)*	`00 0000 1111`	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
`BYPASS`	`11 1111 1111`	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
`USERCODE`	`00 0000 0111`	Selects the 32-bit `USERCODE` register and places it between the `TDI` and `TDO` pins, allowing the `USERCODE` to be serially shifted out of `TDO`. This register defaults to all 1's if not specified in the Quartus II software.
`IDCODE`	`00 0000 0110`	Selects the `IDCODE` register and places it between `TDI` and `TDO`, allowing the `IDCODE` to be serially shifted out of `TDO`.
`HIGHZ` *(1)*	`00 0000 1011`	Places the 1-bit bypass register between the `TDI` and `TDO` pins, which allows the boundary scan test data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.

Figure 3–1. MAX II Parallel Flash Loader



Notes to Figure 3–1:

(1) This block is implemented in LEs.

(2) This function is supported in the Quartus II software.

In System Programmability

MAX II devices can be programmed in-system via the industry standard 4-pin IEEE Std. 1149.1 (JTAG) interface. In-system programmability (ISP) offers quick, efficient iterations during design development and debugging cycles. The logic, circuitry, and interconnects in the MAX II architecture are configured with flash-based SRAM configuration elements. These SRAM elements require configuration data to be loaded each time the device is powered. The process of loading the SRAM data is called configuration. The on-chip configuration flash memory (CFM) block stores the SRAM element's configuration data. The CFM block stores the design's configuration pattern in a reprogrammable flash array. During ISP, the MAX II JTAG and ISP circuitry programs the design pattern into the CFM block's non-volatile flash array.

The MAX II JTAG and ISP controller internally generate the high programming voltages required to program the CFM cells, allowing in-system programming with any of the recommended operating external voltage supplies (that is, 3.3 V/2.5 V or 1.8 V for the MAX IIG and MAX IIZ devices). ISP can be performed anytime after V_{CCINT} and all V_{CCIO} banks have been fully powered and the device has completed the configuration power-up time. By default, during in-system programming, the I/O pins are tri-stated and weakly pulled-up to V_{CCIO} to eliminate board conflicts. The in-system programming clamp and real-time ISP feature allow user control of I/O state or behavior during ISP.

For more information, refer to "In-System Programming Clamp" on page 3–6 and "Real-Time ISP" on page 3–7.

These devices also offer an `ISP_DONE` bit that provides safe operation when in-system programming is interrupted. This `ISP_DONE` bit, which is the last bit programmed, prevents all I/O pins from driving until the bit is programmed.

Table 3–4 shows the programming times for MAX II devices using in-circuit testers to execute the algorithm vectors in hardware. Software-based programming tools used with download cables are slightly slower because of data processing and transfer limitations.

Table 3–4. MAX II Device Family Programming Times

Description	EPM240 EPM240G EPM240Z	EPM570 EPM570G EPM570Z	EPM1270 EPM1270G	EPM2210 EPM2210G	Unit
Erase + Program (1 MHz)	1.72	2.16	2.90	3.92	sec
Erase + Program (10 MHz)	1.65	1.99	2.58	3.40	sec
Verify (1 MHz)	0.09	0.17	0.30	0.49	sec
Verify (10 MHz)	0.01	0.02	0.03	0.05	sec
Complete Program Cycle (1 MHz)	1.81	2.33	3.20	4.41	sec
Complete Program Cycle (10 MHz)	1.66	2.01	2.61	3.45	sec

UFM Programming

The Quartus II software, with the use of POF, Jam, or JBC files, supports programming of the user flash memory (UFM) block independent of the logic array design pattern stored in the CFM block. This allows updating or reading UFM contents through ISP without altering the current logic array design, or vice versa. By default, these programming files and methods will program the entire flash memory contents, which includes the CFM block and UFM contents. The stand-alone embedded Jam STAPL player and Jam Byte-Code Player provides action commands for programming or reading the entire flash memory (UFM and CFM together) or each independently.

For more information, refer to the *Using Jam STAPL for ISP via an Embedded Processor* chapter in the *MAX II Device Handbook*.

In-System Programming Clamp

By default, the IEEE 1532 instruction used for entering ISP automatically tri-states all I/O pins with weak pull-up resistors for the duration of the ISP sequence. However, some systems may require certain pins on MAX II devices to maintain a specific DC logic level during an in-field update. For these systems, an optional in-system programming clamp instruction exists in MAX II circuitry to control I/O behavior during the ISP sequence. The in-system programming clamp instruction enables the device to sample and sustain the value on an output pin (an input pin would remain tri-stated if sampled) or to explicitly set a logic high, logic low, or tri-state value on any pin. Setting these options is controlled on an individual pin basis using the Quartus II software.

For more information, refer to the *Real-Time ISP and ISP Clamp for MAX II Devices* chapter in the *MAX II Device Handbook*.

Referenced Documents

This chapter refereces the following documents:

- *DC and Switching Characteristics* chapter in the *MAX II Device Handbook*
- *Using MAX II Devices in Multi-Voltage Systems* chapter in the *MAX II Device Handbook*

Document Revision History

Table 4–1 shows the revision history for this chapter.

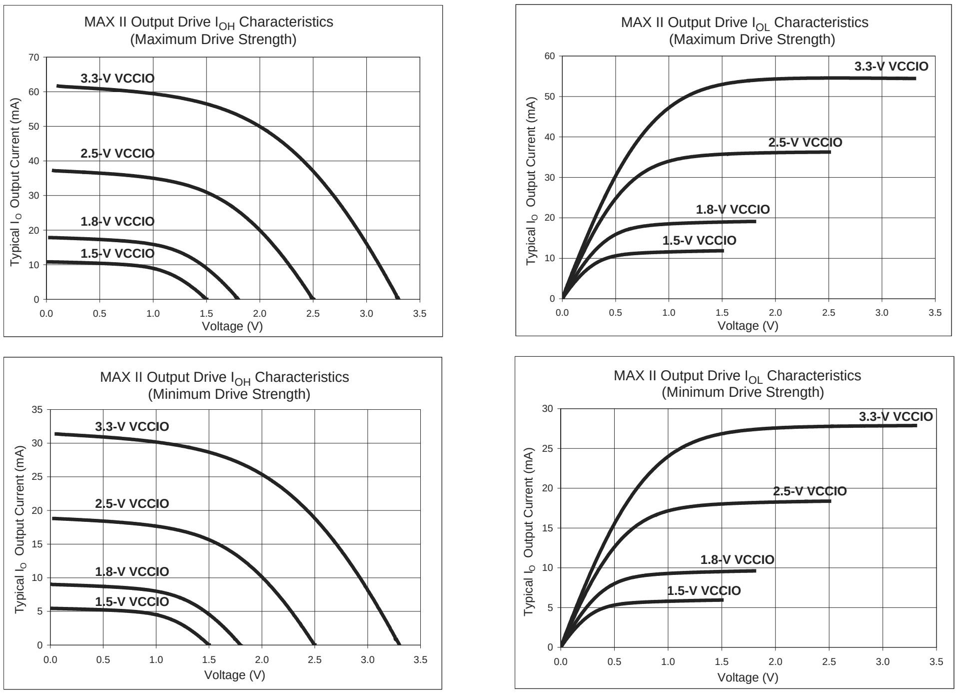
Table 4–1. Document Revision History

Date and Revision	Changes Made	Summary of Changes
October 2008, version2.1	■ Updated "MAX II Hot-Socketing Specifications" and "Power-On Reset Circuitry" sections. ■ Updated New Document Format.	—
December 2007, version 2.0	■ Updated "Hot Socketing Feature Implementation in MAX II Devices" section. ■ Updated "Power-On Reset Circuitry" section. ■ Updated Figure 4–5. ■ Added "Referenced Documents" section.	Updated document with MAX IIZ information.
December 2006, version 1.5	■ Added document revision history.	—
February 2006, version 1.4	■ Updated "MAX II Hot-Socketing Specifications" section. ■ Updated "AC and DC Specifications" section. ■ Updated "Power-On Reset Circuitry" section.	—
June 2005, version 1.3	■ Updated AC and DC specifications on page 4-2.	—
December 2004, version 1.2	■ Added content to Power-Up Characteristics section. ■ Updated Figure 4-5.	—
June 2004, version 1.1	■ Corrected Figure 4-2.	—

Output Drive Characteristics

Figure 5–1 shows the typical drive strength characteristics of MAX II devices.

Figure 5–1. Output Drive Characteristics of MAX II Devices



Note to Figure 5–1:

(1) The DC output current per pin is subject to the absolute maximum rating of Table 5–1.

I/O Standard Specifications

Table 5–5 through Table 5–10 show the MAX II device family I/O standard specifications.

Table 5–5. 3.3-V LVTTL Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.5	0.8	V
V_{OH}	High-level output voltage	IOH = –4 mA *(1)*	2.4	—	V
V_{OL}	Low-level output voltage	IOL = 4 mA *(1)*	—	0.45	V

Table 5–6. 3.3-V LVCMOS Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	I/O supply voltage	—	3.0	3.6	V
V_{IH}	High-level input voltage	—	1.7	4.0	V
V_{IL}	Low-level input voltage	—	–0.5	0.8	V

Internal Timing Parameters

Internal timing parameters are specified on a speed grade basis independent of device density. Table 5–15 through Table 5–22 describe the MAX II device internal timing microparameters for logic elements (LEs), input/output elements (IOEs), UFM blocks, and MultiTrack interconnects. The timing values for –3, –4, and –5 speed grades shown in Table 5–15 through Table 5–22 are based on an EPM1270 device target, while –6, –7, and –8 speed grade values are based on an EPM570Z device target.

For more explanations and descriptions about each internal timing microparameters symbol, refer to the *Understanding Timing in MAX II Devices* chapter in the *MAX II Device Handbook*.

Table 5–15. LE Internal Timing Microparameters

Symbol	Parameter	MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{LUT}	LE combinational LUT delay	—	571	—	742	—	914	—	1,215	—	2,247	—	2,247	ps
t_{COMB}	Combinational path delay	—	147	—	192	—	236	—	243	—	305	—	309	ps
t_{CLR}	LE register clear delay	238	—	309	—	381	—	401	—	541	—	545	—	ps
t_{PRE}	LE register preset delay	238	—	309	—	381	—	401	—	541	—	545	—	ps
t_{SU}	LE register setup time before clock	208	—	271	—	333	—	260	—	319	—	321	—	ps
t_H	LE register hold time after clock	0	—	0	—	0	—	0	—	0	—	0	—	ps
t_{CO}	LE register clock-to-output delay	—	235	—	305	—	376	—	380	—	489	—	494	ps
t_{CLKHL}	Minimum clock high or low time	166	—	216	—	266	—	253	—	335	—	339	—	ps
t_C	Register control delay	—	857	—	1,114	—	1,372	—	1,356	—	1,722	—	1,741	ps

Table 5–21. UFM Block Internal Timing Microparameters (Part 3 of 3)

Symbol	Parameter	MAX II / MAX IIG						MAX IIZ						Unit
		–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{OE}	Delay from data register clock to data register output	180	—	180	—	180	—	180	—	180	—	180	—	ns
t_{RA}	Maximum read access time	—	65	—	65	—	65	—	65	—	65	—	65	ns
t_{OSCS}	Maximum delay between the OSC_ENA rising edge to the erase/program signal rising edge	250	—	250	—	250	—	250	—	250	—	250	—	ns
t_{OSCH}	Minimum delay allowed from the erase/program signal going low to OSC_ENA signal going low	250	—	250	—	250	—	250	—	250	—	250	—	ns

Figure 5–3 through Figure 5–5 show the read, program, and erase waveforms for UFM block timing parameters shown in Table 5–21.

Figure 5–3. UFM Read Waveforms

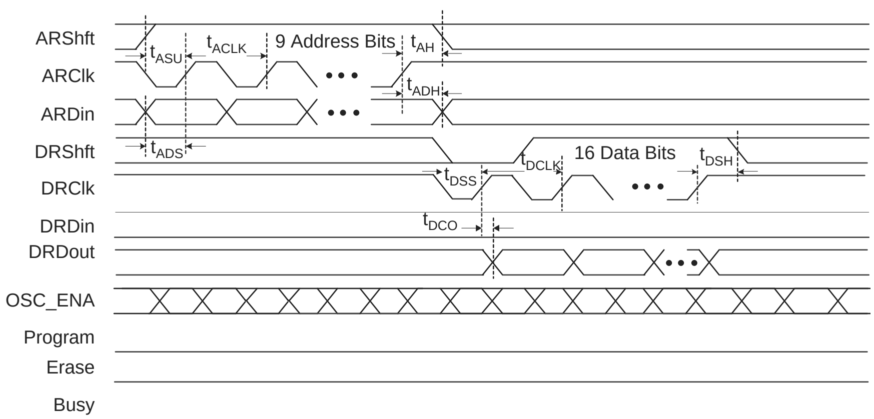


Table 5–24. EPM570 Global Clock External I/O Timing Parameters (Part 2 of 2)

Symbol	Parameter	Condition	MAX II / MAX IIG						MAX IIZ						Unit
			–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	304.0 *(1)*	—	247.5	—	201.1	—	184.1	—	123.5	—	118.3	MHz

Note to Table 5–24:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5–25 shows the external I/O timing parameters for EPM1270 devices.

Table 5–25. EPM1270 Global Clock External I/O Timing Parameters

Symbol	Parameter	Condition	MAX II / MAX IIG						Unit
			–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		
			Min	Max	Min	Max	Min	Max	
t_{PD1}	Worst case pin-to-pin delay through 1 look-up table (LUT)	10 pF	—	6.2	—	8.1	—	10.0	ns
t_{PD2}	Best case pin-to-pin delay through 1 LUT	10 pF	—	3.7	—	4.8	—	5.9	ns
t_{SU}	Global clock setup time	—	1.2	—	1.5	—	1.9	—	ns
t_H	Global clock hold time	—	0	—	0	—	0	—	ns
t_{CO}	Global clock to output delay	10 pF	2.0	4.6	2.0	5.9	2.0	7.3	ns
t_{CH}	Global clock high time	—	166	—	216	—	266	—	ps
t_{CL}	Global clock low time	—	166	—	216	—	266	—	ps
t_{CNT}	Minimum global clock period for 16-bit counter	—	3.3	—	4.0	—	5.0	—	ns
f_{CNT}	Maximum global clock frequency for 16-bit counter	—	—	304.0 *(1)*	—	247.5	—	201.1	MHz

Note to Table 5–25:

(1) The maximum frequency is limited by the I/O standard on the clock input pin. The 16-bit counter critical delay performs faster than this global clock input pin maximum frequency.

Table 5–31. MAX II IOE Programmable Delays

Parameter	MAX II / MAX IIG						MAX IIZ						Unit
	–3 Speed Grade		–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		–7 Speed Grade		–8 Speed Grade		
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Input Delay from Pin to Internal Cells = 1	—	1,225	—	1,592	—	1,960	—	1,858	—	2,171	—	2,214	ps
Input Delay from Pin to Internal Cells = 0	—	89	—	115	—	142	—	569	—	609	—	616	ps

Maximum Input and Output Clock Rates

Table 5–32 and Table 5–33 show the maximum input and output clock rates for standard I/O pins in MAX II devices.

Table 5–32. MAX II Maximum Input Clock Rate for I/O

I/O Standard		MAX II / MAX IIG			MAX IIZ			Unit
		–3 Speed Grade	–4 Speed Grade	–5 Speed Grade	–6 Speed Grade	–7 Speed Grade	–8 Speed Grade	
3.3-V LVTTL	Without Schmitt Trigger	304	304	304	304	304	304	MHz
	With Schmitt Trigger	250	250	250	250	250	250	MHz
3.3-V LVCMOS	Without Schmitt Trigger	304	304	304	304	304	304	MHz
	With Schmitt Trigger	250	250	250	250	250	250	MHz
2.5-V LVTTL	Without Schmitt Trigger	220	220	220	220	220	220	MHz
	With Schmitt Trigger	188	188	188	188	188	188	MHz
2.5-V LVCMOS	Without Schmitt Trigger	220	220	220	220	220	220	MHz
	With Schmitt Trigger	188	188	188	188	188	188	MHz
1.8-V LVTTL	Without Schmitt Trigger	200	200	200	200	200	200	MHz
1.8-V LVCMOS	Without Schmitt Trigger	200	200	200	200	200	200	MHz
1.5-V LVCMOS	Without Schmitt Trigger	150	150	150	150	150	150	MHz
3.3-V PCI	Without Schmitt Trigger	304	304	304	304	304	304	MHz

Table 5–34. MAX II JTAG Timing Parameters (Part 2 of 2)

Symbol	Parameter	Min	Max	Unit
t_{JPSU}	JTAG port setup time *(2)*	8	—	ns
t_{JPH}	JTAG port hold time	10	—	ns
t_{JPCO}	JTAG port clock to output *(2)*	—	15	ns
t_{JPZX}	JTAG port high impedance to valid output *(2)*	—	15	ns
t_{JPXZ}	JTAG port valid output to high impedance *(2)*	—	15	ns
t_{JSSU}	Capture register setup time	8	—	ns
t_{JSH}	Capture register hold time	10	—	ns
t_{JSCO}	Update register clock to output	—	25	ns
t_{JSZX}	Update register high impedance to valid output	—	25	ns
t_{JSXZ}	Update register valid output to high impedance	—	25	ns

Notes to Table 5–34:

(1) Minimum clock period specified for 10 pF load on the TDO pin. Larger loads on TDO will degrade the maximum TCK frequency.

(2) This specification is shown for 3.3-V LVTTL/LVCMOS and 2.5-V LVTTL/LVCMOS operation of the JTAG pins. For 1.8-V LVTTL/LVCMOS and 1.5-V LVCMOS, the t_{JPSU} minimum is 6 ns and t_{JPCO}, t_{JPZX}, and t_{JPXZ} are maximum values at 35 ns.

Referenced Documents

This chapter references the following documents:

- *I/O Structure* section in the *MAX II Architecture* chapter in the *MAX II Device Handbook*
- *Hot Socketing and Power-On Reset in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Operating Requirements for Altera Devices Data Sheet*
- *PowerPlay Power Analysis* chapter in volume 3 of the *Quartus II Handbook*
- *Understanding and Evaluating Power in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Understanding Timing in MAX II Devices* chapter in the *MAX II Device Handbook*
- *Using MAX II Devices in Multi-Voltage Systems* chapter in the *MAX II Device Handbook*

Table 5–35. Document Revision History (Part 2 of 2)

Date and Revision	Changes Made	Summary of Changes
June 2005, version 1.3	■ Updated the R_{PULLUP} parameter in Table 5-4. ■ Added Note 2 to Tables 5-8 and 5-9. ■ Updated Table 5-13. ■ Added "Output Drive Characteristics" section. ■ Added I^2C mode and Notes 5 and 6 to Table 5-14. ■ Updated timing values to Tables 5-14 through 5-33.	—
December 2004, version 1.2	■ Updated timing Tables 5-2, 5-4, 5-12, and Tables 15-14 through 5-34. ■ Table 5-31 is new.	—
June 2004, version 1.1	■ Updated timing Tables 5-15 through 5-32.	—