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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	25MHz
Connectivity	EBI/EMI, I²C, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	36
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.25K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 4.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w79l633a25pl

4. Pin Description

SYMBOL	TYPE	DESCRIPTIONS
$\overline{EA}$	I	**EXTERNAL ACCESS ENABLE:** This pin forces the processor to execute the external ROM. The ROM address and data are not presented on the bus if the $\overline{EA}$ pin is high.
$\overline{PSEN}$	O H	**PROGRAM STORE ENABLE:** $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.
ALE	O H	**ADDRESS LATCH ENABLE:** ALE enables the address latch that separates the address from the data on Port 0.
RST	I L	**RESET:** Set this pin high for two machine cycles while the oscillator is running to reset the device.
XTAL1	I	**CRYSTAL 1:** Crystal oscillator input or external clock input.
XTAL2	O	**CRYSTAL 2:** Crystal oscillator output.
V_{SS}	I	**GROUND**: ground potential.
V_{DD}	I	**POWER SUPPLY:** Supply voltage for operation.
P0.0–P0.7	I/O D S H	**PORT 0:** 8-bit, bi-directional I/O port with internal pull-up resisters. This port also provides a multiplexed, low-order address / data bus during accesses to external memory.
P1.0–P1.7	I/O S H	**PORT 1:** 8-bit, bi-directional I/O port with internal pull-up resistors. This port also provides alternate functions as below. P1.0 ~ P1.5 provide PWM0 ~ PWM5. P1.4 ~ P1.7 provide ADC0 ~ ADC3. P1.0 alternately provides Timer2 external count input.(T2) P1.1 alternately provides Timer2 Reload/Capture/Direction control.(T2Ex)
P2.0–P2.7	I/O S H	**PORT 2:** 8-bit, bi-directional I/O port with internal pull-ups. This port also provides the upper address bits when accessing external memory. P2.4 to P2.7 can be software configured as I2C serial ports
P3.0–P3.7	I/O S H	**PORT 3:** 8-bit, bi-directional I/O port with internal pull-up resistors. All bits have alternate functions, which are described below: RXD (P3.0): Serial Port 0 input TXD (P3.1): Serial Port 0 output $\overline{INT0}$ (P3.2): External Interrupt 0 $\overline{INT1}$(P3.3): External Interrupt 1 T0 (P3.4):Timer 0 External Input T1 (P3.5):Timer 1 External Input $\overline{WR}$ (P3.6): External Data Memory Write Strobe $\overline{RD}$ (P3.7): External Data Memory Read Strobe
P4.0–P4.3	I/O S H	**PORT 4:** 4-bit bi-directional I/O port. The P4.3 also provides the alternate function $\overline{REBOOT}$ which is H/W reboot from LD flash.

* **Note :** TYPE I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain S: Schmitt Trigger

4.1 Port 4

SFR P4 at address A5H, is a 4-bit multipurpose programmable I/O port which functions are I/O, insert wait function and chip-select function. The Port 4 has four different operation modes:

In mode 0, P4.0 ~ P4.3 is a 4-bit bi-directional I/O port which is the same as port 1. The default Port 4 is a general I/O function.

In mode1, P4.0 ~ P4.3 are read data strobe signals which are synchronized with $\overline{RD}$ signal at specified addresses. These read data strobe signals can be used as chip-select signals for external peripherals.

In mode2, P4.0 ~ P4.3 are write data strobe signals which are synchronized with $\overline{WR}$ signal at specified addresses. These write data strobe signals can be used as chip-select signals for external peripherals.

In mode3, P4.0 ~ P4.3 are read/write data strobe signals which are synchronized with $\overline{RD}$ or $\overline{WR}$ signal at specified addresses. These read/write data strobe signals can be used as chip-select signals for external peripherals.

In mode1~mode3, Port 4 is configured with the feature of chip-select signals, the address range for chip-select signals depends on the contents of registers P4xAH and P4xAL, which contain the high-order byte and low-order byte, respectively, of the 16-bit address comparator for P4.x. The registers P4CONA and P4CONB contain the control bits to configure the Port 4 operation mode. This is illustrated in the following schematic.

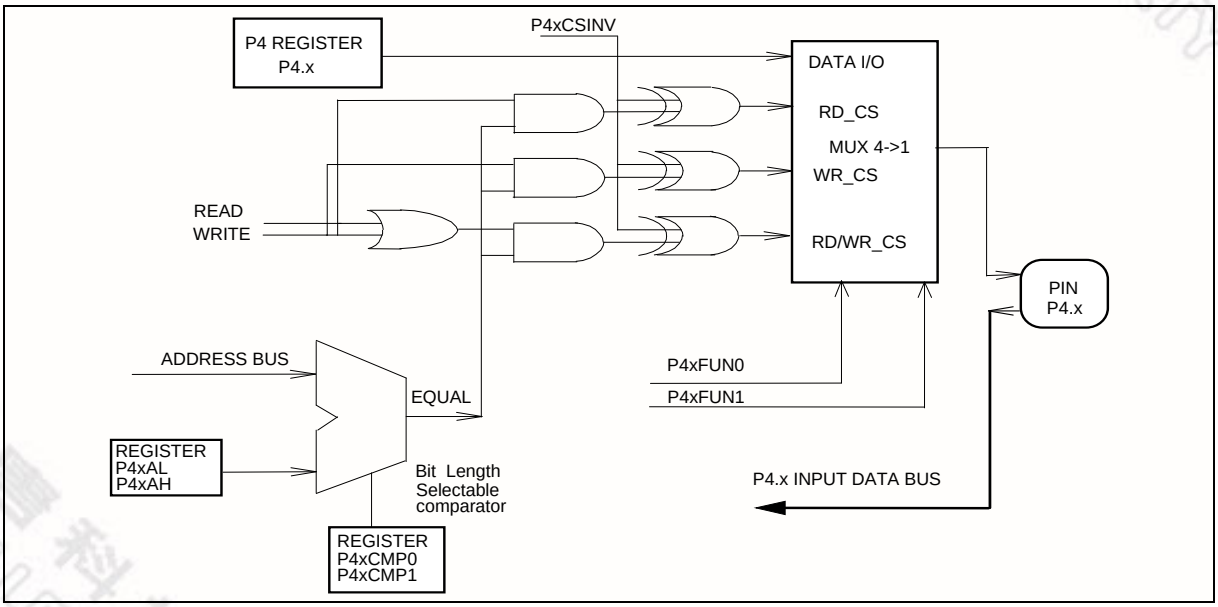


Figure 4-1

For example, the following program sets up P4.0 as a write-strobe signal for I/O port addresses 1234H – 1237H with positive polarity, while P4.1 – P4.3 are used as general I/O ports.

```
MOV  P40AH, #12H
MOV  P40AL, #34H      ; Base I/O address 1234H for P4.0
MOV  P4CONA, #00001010B    ; P4.0 is a write-strobe signal; address lines A0 and A1 are masked.
MOV  P4CONB, #00H   ; P4.1 – P4.3 are general I/O ports
```

5.2 Data Memory

The W79E(L)633 can access up to 64Kbytes of external Data Memory. This memory region is accessed by the MOVX instructions. Unlike the 8051 derivatives, the W79E(L)633 contains on-chip 1K-bytes of Data Memory, which only can be accessed by MOVX instructions. The 1-Kbytes of SRAM located between address 0000h and 03FFh is enabled by setting DMEO bit of PMR register. If MOVX instruction accesses the addresses greater than 03FFh CPU will automatically access external memory through Port 0 and 2. In default condition the 1K-bytes SRAM is disabled and any MOVX directed to the space between 0000h and FFFFh goes to the expanded bus on the Port 0 and 2. The W79E(L)633 also has the standard 256 bytes of on-chip Scratchpad RAM. This can be accessed either by direct addressing or by indirect addressing. There are also some Special Function Registers (SFRs), which can only be accessed by direct addressing. Since the Scratchpad RAM is only 256 bytes, it can be used only when data contents are small.

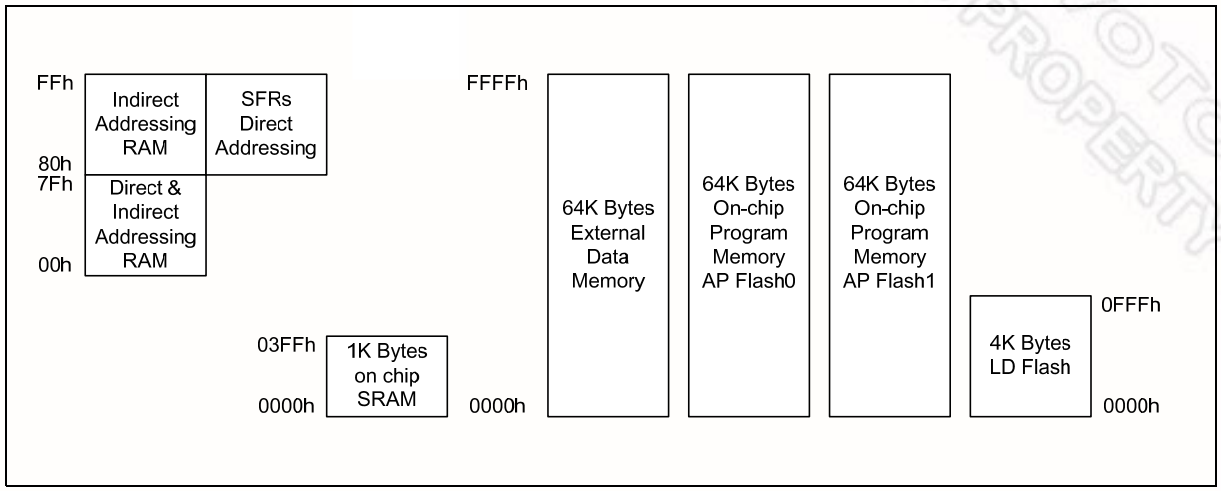


Figure 5-1 Memory Map

Special Function Registers, continued

SYMBOL	DEFINITION	ADDRESS	MSB		BIT_ADDRESS, SYMBOL				LSB		RESET
PWM4	PWM4 Output	CFH									0000 0000B
PWMCON2	PWM Control Register 2	CEH	-	-	-	-	PWM5OE	PWM4OE	ENPWM5	ENPWM4	0000 0000B
TH2	T2 reg. High	CDH									0000 0000B
TL2	T2 reg. Low	CCH									0000 0000B
RCAP2H	T2 Capture Low	CBH									0000 0000B
RCAP2L	T2 Capture High	CAH									0000 0000B
T2MOD	Timer 2 Mode	C9H	-	-	-	-	T2CR	-	-	DCEN	xxxx 0xx0B
T2CON	Timer 2 Control	C8H	(CF) TF2	(CE) EXF2	(CD) RCLK	(CC) TCLK	(CB) EXEN2	(CA) TR2	(C9) C/T2	(C8) CP/RL2	0000 0000B
TA	Time Access Register	C7H									0000 0000B
ADCPS	ADC Input Pin Switch	C6H					ADCPS.3	ADCPS.2	ADCPS.1	ADCPS.0	0000 0000B
STATUS	Status Register	C5H	-	HIP	LIP	-	-	-	-	-	x00x xxxxB
PMR	Power Management Register	C4H	-	-	-	-	-	ALEOFF	-	DME0	xxxx x0x0B
PWM5	PWM5 Output	C3H									0000 0000B
ADCH	ADC converter Result High Byte	C2H	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2	xxxx xxxxxB
ADCL	ADC converter Result Low Byte	C1H	ADCLK1	ADCLK0	-	-	-	-	ADC.1	ADC.0	00xx xxxxxB
ADCCON	ADC Control Register	C0H	ADCEN	-	ADCEX	ADCI	ADCS	AADR2	AADR1	AADR0	0x000000B
SADEN	Slave Address Mask	B9H									0000 0000B
IP	Interrupt Priority	B8H	(BF) -	(BE) PADC	(BD) PT2	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	x000 0000B
P3	Port 3	B0H	(B7) RD	(B6) WR	(B5) T1	(B4) T0	(B3) INT1	(B2) INT0	(B1) TXD	(B0) RXD	1111 1111B
SFRCN	F/W Flash Control	AFH	BANK	WFWIN	NOE	NCE	CTRL3	CTRL2	CTRL1	CTRL0	0011 1111B
SFRFD	F/W Flash Data	AEH									xxxx xxxxxB
SFRAH	F/W Flash High Address	ADH									0000 0000B
SFRAL	F/W Flash Low Address	ACH									0000 0000B
ROMCON	ROM Control	ABH	-	-	-	-	EN128K	DCP12	DCP11	DCP10	00000111B
SADDR	Slave Address	A9H									0000 0000B
IE	Interrupt Enable	A8H	(AF) EA	(AE) EADC	(AD) ET2	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0000 0000B
P4	Port 4	A5H	-	-	-	-					xxxx 1111B
P4CSIN	P4 CS SIGN	A2H	P43CSINV	P42CSINV	P41CSINV	P40CSINV	-	PWDNH	RMWFP	-	0000 0000B
XRAMAH	RAM High byte Address	A1H	-	-	-	-	-	-	0	0	0000 0000B

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General-purpose digital input port or analog input port AD0~AD7. For digital input, port-read instructions read the port pins, while read-modify-write instructions read the port latch. Additional functions are described below.

	ALTERNATE FUNCTION1	ALTERNATE FUNCTION2	ALTERNATE FUNCTION3
P1.0	T2: External input for Timer/Counter 2	PWM0: PWM output ch0	-
P1.1	T2EX: Timer/Counter 2 Capture/Reload Trigger	PWM1: PWM output ch1	-
P1.2	STADC: External rising edge input to start ADC	PWM2: PWM output ch2	-
P1.3	-	PWM3: PWM output ch3	-
P1.4	-	PWM4: PWM output ch4	ADC0: Analog input0
P1.5	-	PWM5: PWM output ch5	ADC1: Analog input1
P1.6	-	-	ADC2: Analog input2
P1.7	-	-	ADC3: Analog input3

Port 4 Control Register A

Bit:	7	6	5	4	3	2	1	0
	P41M1	P41M0	P41C1	P41C0	P40M1	P40M0	P40C1	P40C0

Mnemonic: P4CONA Address: 92h

Port 4 Control Register B

Bit:	7	6	5	4	3	2	1	0
	P43M1	P43M0	P43C1	P43C0	P42M1	P42M0	P42C1	P42C0

Mnemonic: P4CONB Address: 93h

BIT NAME	FUNCTION
P4xM1, P4xM0	Port 4 alternate modes. =00: Mode 0. P4.x is a general purpose I/O port which is the same as Port 1. =01: Mode 1. P4.x is a Read Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0. =10: Mode 2. P4.x is a Write Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0. =11: Mode 3. P4.x is a Read/Write Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0
P4xC1, P4xC0	Port 4 Chip-select Mode address comparison: =00: Compare the full address (16 bits length) with the base address registers P4xAH and P4xAL. =01: Compare the 15 high bits (A15-A1) of address bus with the base address registers P4xAH and P4xAL. =10: Compare the 14 high bits (A15-A2) of address bus with the base address registers P4xAH and P4xAL. =11: Compare the 8 high bits (A15-A8) of address bus with the base address registers P4xAH and P4xAL.

P4.0 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

```
CKCON       REG   8EH
                  MOV   TA, #AAH
                  MOV   TA, #55H
                  SETB  WDCON.0              ; Reset Watchdog Timer
                  ORL   CKCON, #11000000B    ; Select 26 bits Watchdog Timer
                  MOV   TA, #AAH
                  MOV   TA, #55H
                  ORL   WDCON, #00000010B    ; Enable watchdog
```

The other bits in WDCON have unrestricted write access.

PWM Pre-scale Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-

Mnemonic: PWMP Address: D9h

PWMP.7-0 Adjust PWM frequency. $Fpwm = \frac{Fosc}{2 \times (1 + PWMP) \times 255}$

PWM0

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-

Mnemonic: PWM0 Address: DAh

PWM0.7-0 Adjust PWM0 duty cycle. PWMn high/low ratio of $PWMn = \frac{PWMn}{255 - (PWMn)}$

PWM1

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-

Mnemonic: PWM1 Address: DBh

PWM1.7-0 Adjust PWM1 duty cycle.

PWM Control Register1

Bit:	7	6	5	4	3	2	1	0
	PWM3OE	PWM2OE	ENPWM3	ENPWM2	PWM1OE	PWM0OE	ENPWM1	ENPWM0

Mnemonic: PWMCON1 Address: DCh

ACCUMULATOR

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

ACC.7-0 The A (or ACC) register is the standard 8051/52 accumulator.

EXTENDED INTERRUPT ENABLE

Bit:	7	6	5	4	3	2	1	0
	-	-	-	EWDI	-	-	EI2C2	EI2C1

Mnemonic: EIE Address: E8h

EWDI Enable Watchdog timer interrupt

EI2C2 Enable I2C channel 2 interrupt

EI2C1 Enable I2C channel 1 interrupt

I2C Control Register Channel 1

Bit:	7	6	5	4	3	2	1	0
	-	ENS1	STA	STO	SI	AA	-	-

Mnemonic: I2CON Address: E9h

ENS1 Enable channel 1 of I2C serial function block. When ENS1=1 the channel 1 of I2C serial function enables. The port latches of SDA1 and SCL1 must be set to logic high.

STA I2C START Flag. Setting STA to logic 1 to enter master mode, the I2C hardware sends a START or repeat START condition to bus when the bus is free.

STO I2C STOP Flag. In master mode, setting STO to transmit a STOP condition to bus then I2C hardware checks the bus condition, if a STOP condition is detected this flag will be cleared by hardware automatically. In a slave mode, setting STO resets I2C hardware to the defined “not addressed” slave mode.

SI I2C Port 1 Interrupt Flag. When a new SIO1 state is present in the S1STA register, the SI flag is set by hardware, and if the EA and EI2C1 bits are both set, the I2C1 interrupt is requested. SI must be cleared by software.

AA Assert Acknowledge Flag. If AA is set to logic 1, an acknowledged signal (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line. If AA is cleared, a non-acknowledged signal (high level to SDA) will be returned during the acknowledge clock pulse on the SCL line.

Bit0 Must be zero always

I2C Channel 1 Address Register 0

Bit:	7	6	5	4	3	2	1	0
	I2ADDR.7	I2ADDR.6	I2ADDR.5	I2ADDR.4	I2ADDR.3	I2ADDR.2	I2ADDR.1	GC

Mnemonic: I2ADDR10 Address: EAh

I2ADDR10.7-1 I2C1 Slave Address0. The 8051 uC can read from and write to this 8-bit, directly addressable SFR. The contents of the register are irrelevant when I2C is in master mode. In the slave mode, the seven most significant bits must be loaded with the MCU’s own slave address. The I2C hardware will react if the contents of I2ADDR10 are matched with the received slave address.

I2C Baud Rate Control Register Channel 2

Bit:	7	6	5	4	3	2	1	0
	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0

Mnemonic: I2CLK2 Address: FEh

I2CLK2.7-0 The I2C clock rate control

I2C Timer Counter Register Channel 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	ENTI2	DIV42	TIF2

Mnemonic: I2TIMER2 Address: FFh

ENTI2 Enable I2C 14-bits Time-out Counter. Setting ENTI to logic high will firstly reset the time-out counter and then start up counting. Clearing ENTI disables the 14-bit time-out counter. ENTI can be set to logic high only when SI=0.

DIV42 I2C Time-out Counter Clock Frequency Selection. DIV42= 0 the clock frequency is coherent to the system clock Fosc. DIV42 = 1 the clock frequency is Fosc/4.

TIF2 I2C Time-out Flag. When the time-out counter overflows hardware will set this flag and request the I2C2 interrupt if I2C2 interrupt is enabled (EI2C1=1). This bit must be cleared by software.

Stretching only affects the MOVX instruction. There is no effect on any other instruction or its timing, it is as if the state of the CPU is held for the desired period. The timing waveforms when the stretch value is zero, one, and two are shown below.

Table 7-2 Data Memory Cycle Stretch Values

M2	M1	M0	MACHINE CYCLES	$\overline{RD}$ OR $\overline{WR}$ STROBE WIDTH IN CLOCKS	$\overline{RD}$ OR $\overline{WR}$ STROBE WIDTH @ 25 MHZ	$\overline{RD}$ OR $\overline{WR}$ STROBE WIDTH @ 40 MHZ
0	0	0	2	2	80 nS	50 nS
0	0	1	3 (default)	4	160 nS	100 nS
0	1	0	4	8	320 nS	200 nS
0	1	1	5	12	480 nS	300 nS
1	0	0	6	16	640 nS	400 nS
1	0	1	7	20	800 nS	500 nS
1	1	0	8	24	960 nS	600 nS
1	1	1	9	28	1120 nS	700 nS

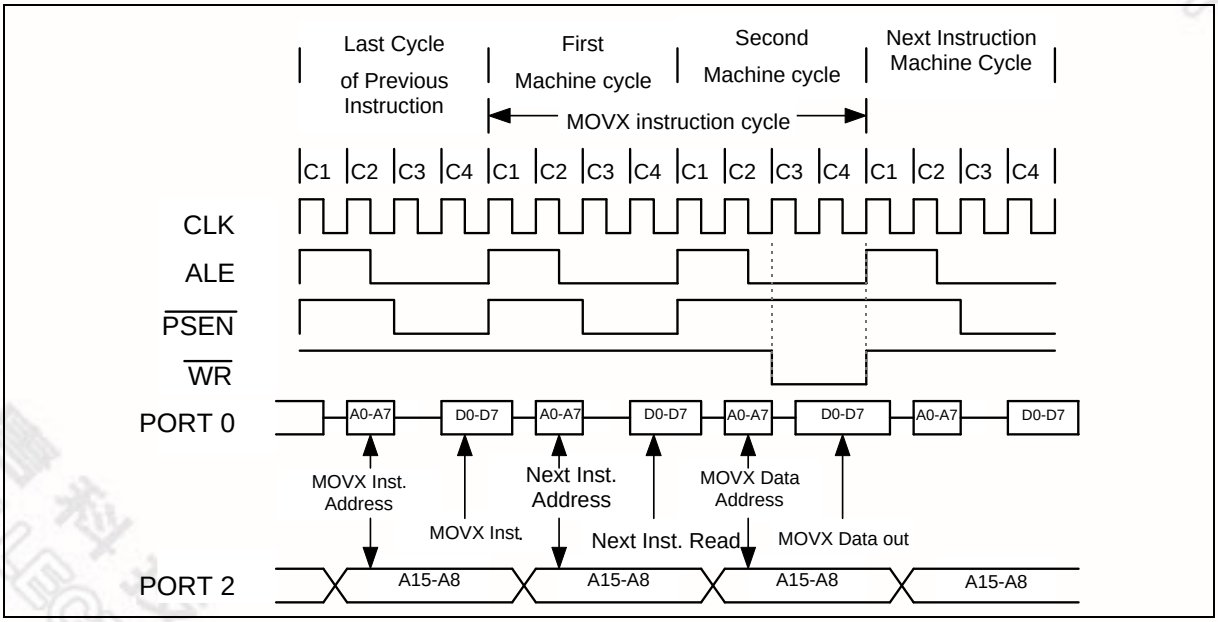


Figure 7-6 Data Memory Write with Stretch Value = 0

When the selected time-out occurs, the watchdog interrupt flag WDIF (WDCON.3) is set. Then, if there is no RWT and if the Watchdog Timer reset EWT (WDCON.1) is enabled, the Watchdog Timer reset occurs 512 clocks later. This reset lasts two machine cycles, and the Watchdog Timer reset flag WTRF (WDCON.2) is set, which indicates that the Watchdog Timer caused the reset.

The Watchdog Timer is disabled by a power-on/fail reset. The external reset and Watchdog Timer reset can not disable Watchdog Timer but restart the Timer.

The control bits that support the Watchdog Timer are discussed below.

Watchdog Timer Control (WDCON)

7	-	Reserved.
6	POR	Power-on reset flag. The hardware sets this flag during power–up, and it can only be cleared by software. This flag can also be written by software.
5-4	-	Reserved.
3	WDIF	Watchdog Timer Interrupt Flag. If the watchdog interrupt is enabled, the hardware sets this bit to indicate that the watchdog interrupt has occurred. If the interrupt is not enabled, this bit indicates that the time-out period has elapsed. This bit must be cleared by software.
2	WTRF	Watchdog Timer Reset Flag. If EWT is 0, the Watchdog Timer has no affect on this bit. Otherwise, the hardware sets this bit when the Watchdog Timer causes a reset. It can be cleared by software or a power-fail reset. It can be also read by software, which helps determine the cause of a reset.
1	EWT	Enable Watchdog-Timer Reset. Set this bit to enable the Watchdog Timer Reset function.
0	RWT	Reset Watchdog Timer. Set this bit to reset the Watchdog Timer before a time-out occurs. This bit is automatically cleared by the hardware.

The EWT, WDIF and RWT bits are protected by the Timed Access procedure. This procedure prevents software, especially errant code, from accidentally enabling or disabling the Watchdog Timer. An example is provided below.

```
        org     63h
        mov     TA,#AAH
        mov     TA,#55H
        clr     WDIF
        jnb     execute_reset_flag,bypass_reset     ; Test if CPU need to reset.
        jmp     $                                   ; Wait to reset
bypass_reset:
        mov     TA,#AAH
        mov     TA,#55H
        setb    RWT
        reti

        org     300h
```

```
start:
        mov     ckcon,#01h              ; select 2 ^ 17 timer
;       mov     ckcon,#61h              ; select 2 ^ 20 timer
;       mov     ckcon,#81h              ; select 2 ^ 23 timer
;       mov     ckcon,#c1h              ; select 2 ^ 26 timer
        mov     TA,#aah
        mov     TA,#55h
        mov     WDCON,#00000011B
        setb    EWDI
        setb    ea
        jmp     $                       ; wait time out
```

Clock Control

WD1, WD0: CKCON.7, CKCON.6 - Watchdog Timer Mode select bits. These two bits select the time-out interval for the Watchdog Timer. The reset interval is 512 clocks longer than the selected interval. The default time-out is 2^{17} clocks, the shortest time-out period.

14. Serial Port

The W79E(L)633 serial port is a full-duplex port, and the W79E(L)633 provides additional features, such as Frame Error Detection and Automatic Address Recognition. The serial port is capable of synchronous and asynchronous communication. In synchronous mode, the W79E(L)633 generates the clock and operates in half-duplex mode. In asynchronous mode, the serial port can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF, but any write to SBUF writes to the transmit register while any read from SBUF reads from the receive buffer. The serial port can operate in four modes, as described below.

14.1 Mode 0

This mode provides half-duplex, synchronous communication with external devices. In this mode, serial data is transmitted and received on the RXD line, and the W79E(L)633 provides the shift clock on TxD, whether the device is transmitting or receiving. Eight bits are transmitted or received per frame, LSB first. The baud rate is 1/12 or 1/4 of the oscillator frequency, as determined by the SM2 bit (SCON.5; 0 = 1/12; 1 = 1/4). This programmable baud rate is the only difference between the standard 8051/52 and the W79E(L)633 in mode 0.

Any write to SBUF starts transmission. The shift clock is activated, and data is shifted out on RxD until all eight bits are transmitted. If SM2 is 1, the data appears on RxD one clock period before the falling edge of the shift clock on TxD. Then, the clock remains low for two clock periods before going high again. If SM2 is 0, the data appears on RxD three clock periods before the falling edge of the shift clock on TxD, and the clock on TxD remains low for six clock periods before going high again. This ensures that, at the receiving end, the data on the RxD line can be clocked on the rising edge of the shift clock or latched when the clock is low. The TI flag is set high in C1 following the end of transmission. The functional block diagram is shown below.

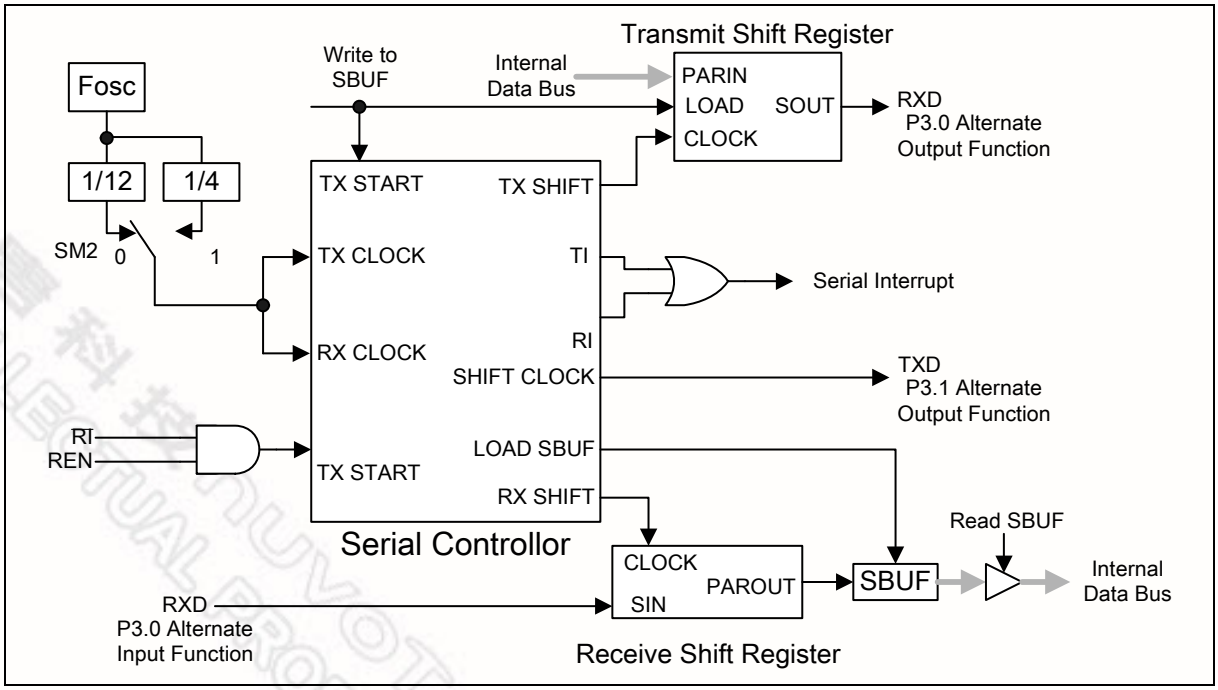


Figure 14-1 Serial Port Mode 0

15.3.3 Slave/Transmitter Mode

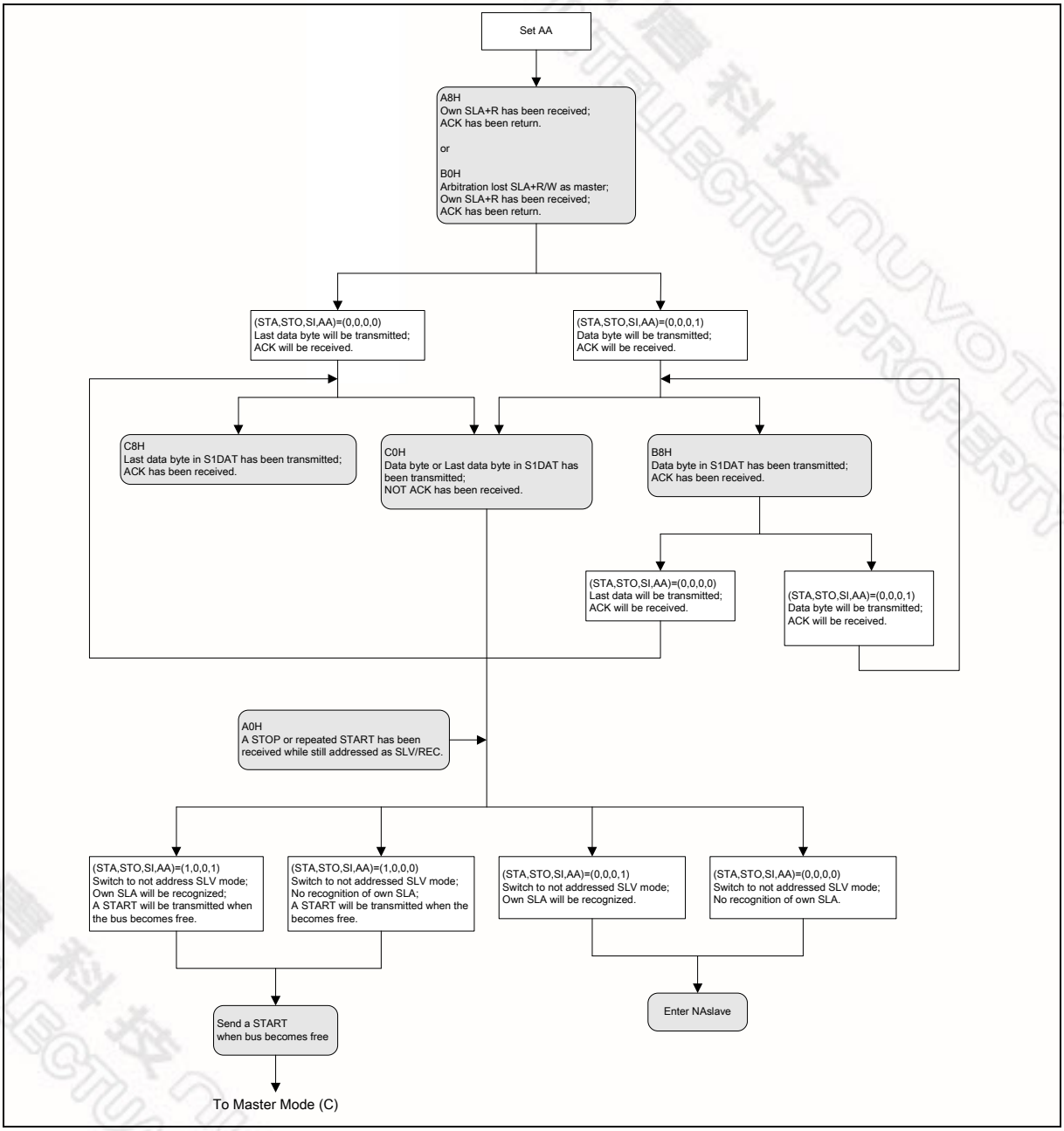


Figure 15-7 Slave Transmitter Mode

15.3.4 Slave/Receiver Mode

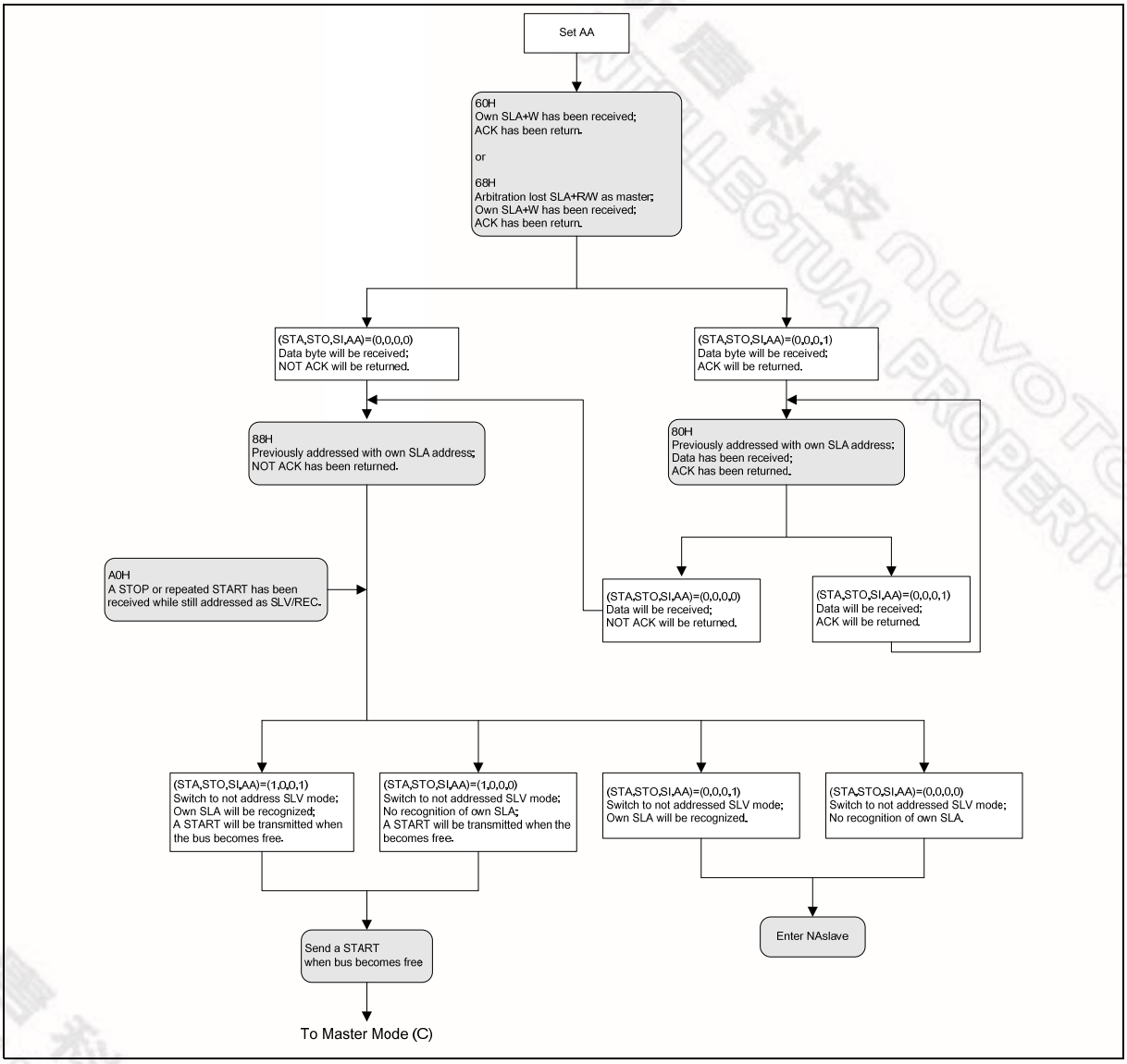


Figure 15-8 Slave Receiver Mode

16.3 ADC Control Registers

ADC Control Register

Bit:	7	6	5	4	3	2	1	0
	ADCEN	-	ADCEX	ADCI	ADCS	AADR2	AADR1	AADR0

Mnemonic: ADCCON Address: C0h

ADCEN Enable A/D Converter Function. Set ADCEN to logic high to enable ADC block.

ADCEX Enable external start control of ADC conversion by a rising edge from P1.2. ADCEX=0: Disable external start. ADCEX=1: Enable external start control.

ADCI A/D Converting Complete/Interrupt Flag. This flag is set when ADC conversion is completed and will cause a hardware interrupt if ADC interrupt is enabled. It is cleared by software only.

ADCS A/D Converting Start. Setting this bit by software starts the conversion of the selected ADC input. ADCS remains high while ADC is converting signal and will be automatically cleared by hardware when ADC conversion is completed.

AADR[2:0] Select and enable analog input channel from ADC0 to ADC3.

The ADCI and ADCS control the ADC conversion as below:

ADCI	ADCS	ADC STATUS
0	0	ADC not busy; A conversion can be started.
0	1	ADC busy; Start of a new conversion is blocked.
1	0	Conversion completed; Start of a new conversion requires ADCI = 0.
1	1	This is an internal temporary state that user can ignore it.

ADC Converter Result Low Register

Bit:	7	6	5	4	3	2	1	0
	ADCLK1	ADCLK0	-	-	-	-	ADC.1	ADC.0

Mnemonic: ADCL Address: C1h

ADCLK[1:0] ADC Clock Frequency Select. The 10-bit ADC needs a clock to drive the converting that the clock frequency may not over 4MHz. ADCLK[1:0] controls the frequency of the clock to ADC block as below table.

ADCLK1	ADCLK0	ADC CLOCK FREQUENCY
0	0	Crystal clock / 4 (Default)
0	1	Crystal clock / 8
1	0	Crystal clock / 16
1	1	Reserved

ADC[1:0] 2 LSB of 10-bit A/D conversion result. The 2 bits are read only.

20. In-System Programming

20.1 The Loader Program Locates at LDFlash Memory

CPU is Free Run at APFlash memory. CHPCON register had been set #03H value before CPU has entered idle state. CPU will switch to LDFlash memory and execute a reset action. H/W reboot mode will switch to LDFlash memory, too. Set SFRCN register where it locates at user's loader program to update APFlash bank 0 or bank 1 memory. Set a SWRESET (CHPCON=#83H) to switch back APFlash after CPU has updated APFlash program. CPU will restart to run program from reset state.

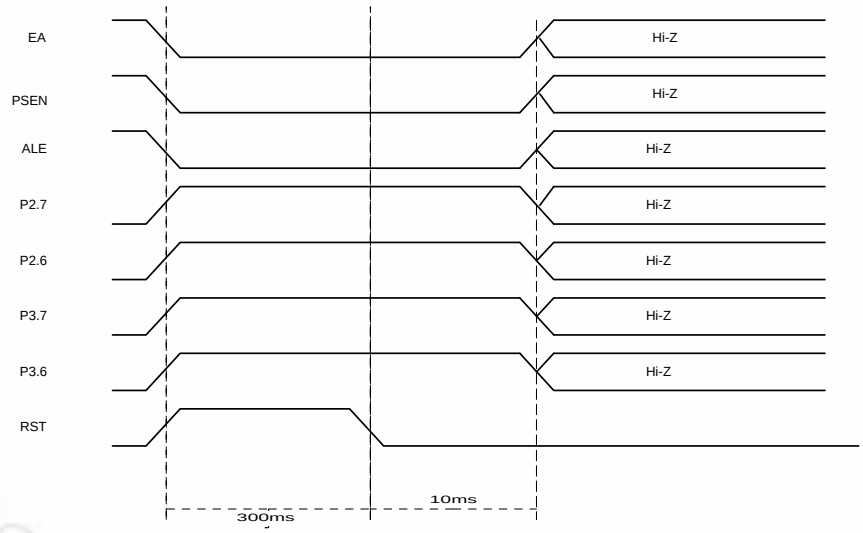
20.2 The Loader Program Locates at APFlash Memory

CPU is Free Run at APFlash memory. CHPCON register had been set #01H value before CPU has entered idle state. Set SFRCN register to update LDFlash or another bank of APFlash program. CPU will continue to run user's APFlash program after CPU has updated program. Please refer demonstrative code to understand other detail description.

21. H/W Writer Mode

This mode is for the writer to write / read Flash EPROM operation. A general user may not enter this mode.

The Timing For Entering Flash EPROM Mode on the Programmer



DC Characteristics, continued

PARAMETER	SYMBOL	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Input High Voltage XTAL1[*3]	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Sink current P1, P3, P4	Isk1	4	8	mA	VDD =4.5V Vs = 0.45V
Sink current P0,P2, ALE, $\overline{PSEN}$	Isk2	10	14	mA	VDD =4.5V VOL = 0.45V
Source current P1, P3, P4	Isr1	-180	-360	uA	VDD =4.5V VOL = 2.4V
Source current P0, P2, ALE, $\overline{PSEN}$	Isr2	-10	-14	mA	VDD =4.5V VOL = 2.4V
Output Low Voltage P1, P3, P4	VOL1	-	0.45	V	VDD = 4.5V IOL = +6 mA
Output Low Voltage P0, P2, ALE, $\overline{PSEN}$ [*2]	VOL2	-	0.45	V	VDD = 4.5V IOL = +10 mA
Output High Voltage P1, P3, P4	VOH1	2.4	-	V	VDD = 4.5V IOH = -180 μA
Output High Voltage P0, P2, ALE, $\overline{PSEN}$ [*2]	VOH2	2.4	-	V	VDD = 4.5V IOH = -10mA

Notes:

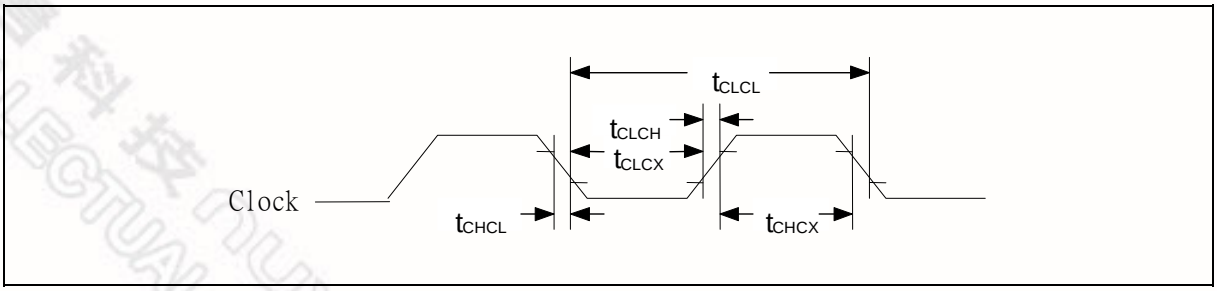
*1. RST pin is a Schmitt trigger input.

*2. P0, ALE and $\overline{PSEN}$ are tested in the external access mode.

*3. XTAL1 is a CMOS input.

*4. Pins of P0, P1, P2, P3, P4 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when VIN approximates to 2V.

23.3 AC Characteristics



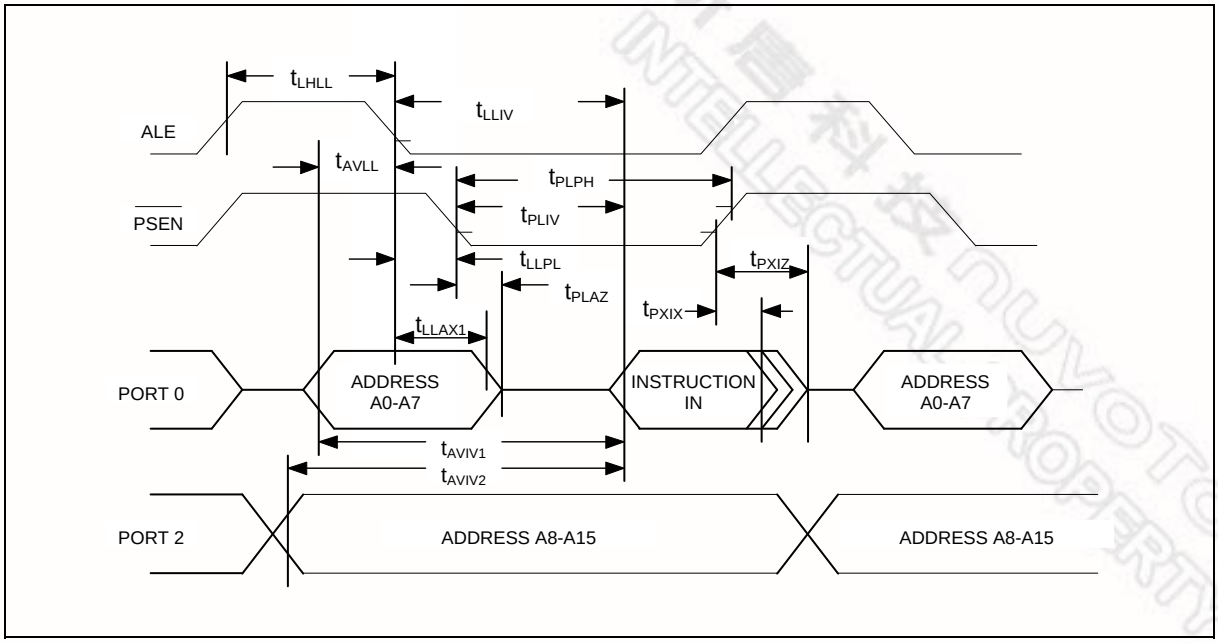
Note: Duty cycle is 50%.

23.3.3 MOVX Characteristics Using Stretch Memory Cycle

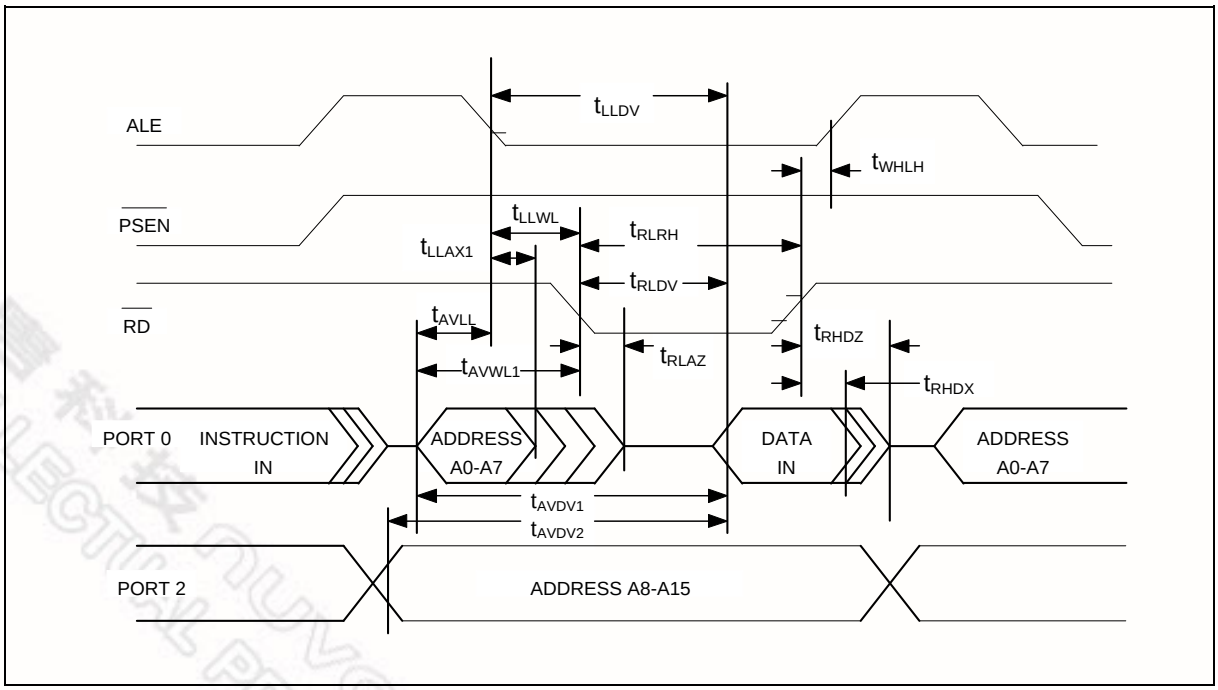
PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS	STRECH
Data Access ALE Pulse Width	t_{LLHL2}	$1.5t_{CLCL} - 5$ $2.0t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
Address Hold After ALE Low for MOVX write	t_{LLAX2}	$0.5t_{CLCL} - 5$		nS	
$\overline{RD}$ Pulse Width	t_{RLRH}	$2.0t_{CLCL} - 5$ $t_{MCS} - 10$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
$\overline{WR}$ Pulse Width	t_{WLWH}	$2.0t_{CLCL} - 5$ $t_{MCS} - 10$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2.0t_{CLCL} - 20$ $t_{MCS} - 20$	nS	$t_{MCS} = 0$ $t_{MCS}>0$
Data Hold after Read	t_{RHDX}	0		nS	
Data Float after Read	t_{RHDZ}		$t_{CLCL} - 5$ $2.0t_{CLCL} - 5$	nS	$t_{MCS} = 0$ $t_{MCS}>0$
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL} - 5$ $t_{MCS} + 2t_{CLCL} - 40$	nS	$t_{MCS} = 0$ $t_{MCS}>0$
Port 0 Address to Valid Data In	t_{AVDV1}		$3.0t_{CLCL} - 20$ $2.0t_{CLCL} - 5$	nS	$t_{MCS} = 0$ $t_{MCS}>0$
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL} - 5$ $1.5t_{CLCL} - 5$	$0.5t_{CLCL} + 5$ $1.5t_{CLCL} + 5$	nS	$t_{MCS} = 0$ $t_{MCS}>0$
Port 0 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL}	$t_{CLCL} - 5$ $2.0t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
Port 2 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL} - 5$ $2.5t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
Data Valid to WR Transition	t_{QVWX}	-5 $1.0t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
Data Hold after Write	t_{WHQX}	$t_{CLCL} - 5$ $2.0t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
$\overline{RD}$ Low to Address Float	t_{RLAZ}		$0.5t_{CLCL} - 5$	nS	
$\overline{RD}$ or WR high to ALE high	t_{WHLH}	0 $1.0t_{CLCL} - 5$	10 $1.0t_{CLCL} + 5$	nS	$t_{MCS} = 0$ $t_{MCS}>0$

Note: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the time period of t_{MCS} for each selection of the Stretch value.

23.6 Program Memory Read Cycle



23.7 Data Memory Read Cycle



```
SFRAL       EQU         ACH
SFRAH       EQU         ADH
SFRFD EQU           AEH
SFRCN EQU           AFH

        ORG 000H
        LJMP 100H           ; JUMP TO MAIN PROGRAM
;*********************************************************************
;* 1. TIMER0 SERVICE VECTOR ORG = 0BH
;*********************************************************************
        ORG 000BH
        CLR  TR0            ; TR0 = 0, STOP TIMER0
        MOV  TL0, R6
        MOV  TH0, R7
        RETI
;*********************************************************************
;*  4KB LDFlash MAIN PROGRAM
;*********************************************************************
        ORG 100H
MAIN_4K:
        MOV  TA,#AAH
        MOV  TA,#55H
        MOV  CHPCON,#03H    ; CHPCON = 03H, ENABLE IN-SYSTEM PROGRAMMING.
        MOV  SFRCN,#0H
        MOV  TCON,#00H      ; TCON = 00H, TR = 0 TIMER0 STOP
        MOV  TMOD,#01H      ; TMOD = 01H, SET TIMER0 A 16BIT TIMER
        MOV  IP,#00H        ; IP = 00H
        MOV  IE,#82H        ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV  R6,#F0H
        MOV  R7,#FFH
        MOV  TL0,R6
        MOV  TH0,R7
        MOV  TCON,#10H      ; TCON = 10H, TR0 = 1, GO
        MOV  PCON,#01H      ; ENTER IDLE MODE

 UPDATE_APFlash:
        MOV  TCON,#00H      ; TCON = 00H , TR = 0 TIM0 STOP
        MOV  IP,#00H        ; IP = 00H
        MOV  IE,#82H        ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV  TMOD,#01H      ; TMOD = 01H, MODE1
        MOV  R6,#D0H        ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15 ms
                            ;DEPENDING ON USER'S SYSTEM CLOCK RATE.
        MOV  R7,#8AH
```