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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Power Line Communications
Core Processor	External
Program Memory Type	-
Controller Series	-
RAM Size	-
Interface	SPI
Number of I/O	-
Voltage - Supply	3V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atpl230a-aku-r

3. Signal Description

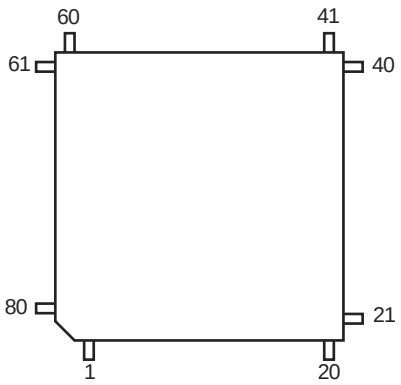
Table 3-1. Signal Description List

Signal Name	Function	Type	Active Level	Voltage reference	Comments
Power Supplies					
VDDIO	3.3V digital supply. Digital power supply must be decoupled by external capacitors	Power			3.0V to 3.6V
VDDIN	3.3V Digital LDO input supply	Power			3.0V to 3.6V
VDDIN AN	3.3V Analog LDO input supply	Power			3.0V to 3.6V
VDDOUT AN	1.2V Analog LDO output. A capacitor in the range 0.1µF - 10µF must be connected to each pin	Power			1.2V
VDDOUT	1.2V Digital LDO output. A capacitor in the range 0.1µF - 10µF must be connected to each pin	Power			1.2V
VDDPLL	1.2V PLL supply. It must be decoupled by a 100nF external capacitor, and connected to VDDOUT through a filter (Cut off frequency: 25kHz)	Power			1.2V
GND(1)	Digital Ground	Power			
AGND(1)	Analog Ground	Power			
Clocks, Oscillators and PLLs					
CLKEA(2)	External Clock Oscillator • CLKEA must be connected to one terminal of a crystal (when a crystal is being used) or used as input for external clock signal	Input		VDDIO	
CLKEB(2)	External Clock Oscillator • CLKEB must be connected to one terminal of a crystal (when a crystal is being used) or must be floating when an external clock signal is connected through CLKEA	I/O		VDDIO	
CLKOUT	10MHz External Clock Output	Output		VDDIO	
Reset/Test					
ARST	Asynchronous Reset	Input	Low	VDDIO	Internal pull up(3)
SRST	Synchronous Reset	Input	Low	VDDIO	Internal pull up(3)
PLL INIT	PLL Initialization Signal	Input	Low	VDDIO	Internal pull up(3)
PPLC (PRIME Power Line Communications) Transceiver					
EMIT [0:11](4)	PLC Tri-state Transmission ports	Output		VDDIO	
AGC [0:5]	Automatic Gain Control: • These digital tri-state outputs are managed by AGC hardware logic to drive external circuitry when input signal attenuation is needed	Output		VDDIO	

4. Package and Pinout

4.1 80-Lead LQFP Package Outline

Figure 4-1. Orientation of the 80-Lead LQFP Package



4.2 80-Lead LQFP Pinout

Table 4-1. 80 - Lead LQFP Pinout

1	NC	21	VDDIO	41	GND	61	GND
2	NC	22	NC	42	EMIT8	62	AGND
3	NC	23	CLKOUT	43	EMIT9	63	VDDOUT AN
4	ARST	24	CS	44	EMIT10	64	VIMA
5	PLL INIT	25	SCK	45	EMIT11	65	VIPA
6	GND	26	MOSI	46	VDDIO	66	VDDOUT AN
7	CLKEA	27	MISO	47	GND	67	AGND
8	GND	28	VDDIO	48	VDDOUT	68	VRP
9	CLKEB	29	GND	49	TXRX0	69	VRM
10	VDDIO	30	EMIT0	50	TXRX1	70	VRC
11	GND	31	EMIT1	51	GND	71	VDDIN AN
12	VDDPLL	32	EMIT2	52	AGC2	72	AGND
13	GND	33	EMIT3	53	AGC5	73	AGND
14	VDDIN	34	VDDIO	54	AGC1	74	VDDIN AN
15	VDDIN	35	GND	55	AGC4	75	GND
16	GND	36	EMIT4	56	AGC0	76	VDDIO
17	VDDOUT	37	EMIT5	57	AGC3	77	VZ CROSS
18	GND	38	EMIT6	58	VDDIO	78	NC
19	NC	39	EMIT7	59	GND	79	NC
20	SRST	40	VDDIO	60	EINT	80	NC

The ATPL230A SPI allows an external device (working as a master), to communicate with the ATPL230A (working as a slave). Below is a brief description of the SPI signals:

- **CS, Chip Select (pin no.24):** This input enables/disables the slave SPI. The ATPL230A is configured to work always as a slave. When disabled (CS pin is tied high), the other SPI signals (SCK, MOSI and MISO) are not taken into account.

  CS = '0': SPI enabled.

  CS = '1': SPI disabled.

- **SCK, Serial Peripheral Interface Clock (pin no.25):** In reception (master slave), data is read from MOSI line in the rising edge of the SPI clock. In transmission (slave master), data is released to MISO in the falling edge of the SPI clock.

  It is recommended not to work with clock frequencies above 10MHz.

  This input only will be taken into account when CS='0'.

- **MOSI, Master Out Slave In (pin no.26):** MOSI is the slave's data input line. Data is read from MOSI line in the rising edge of SCK.

  This input only will be taken into account when CS='0'.

- **MISO, Master In Slave Out (pin no.27):** MISO is the slave's data output line. Data is released to MISO in the falling edge of SCK.

Furthermore, ATPL230A SPI bridge uses an additional line to send interrupts to the host CPU:

- **EINT (pin no.60):** This signal is an interrupt from ATPL230A PHY layer to the microcontroller.

  In reception, every time a PLC message is received, the PHY Layer generates two interrupts. One of them when the physical header is correctly received (two first symbols), and the other one when the message is completely received.

  In transmission, an interrupt will be generated every time a complete message has been sent.

  This signal is low level active.

6.2 SPI Operation

When establishing a SPI communication (CS line is set to '0' by the master), the first byte sent through MOSI line corresponds to the operation code. Four different operation types are defined over ATPL230A SPI. The operation codes are shown in the following table:

Table 6-1. Operation Codes

Operation	Mask type	OpCode
Read	---	0x63
Write	---	0x2A
Mask	AND	0x4C
	OR	0x71
	XOR	0x6D
Write_rep	---	0x1E

Following the operation code, the second and third bytes correspond to the SRAM address (16-bit address). Depending on the operation code, the master will "read data from"/"write data to"/"mask data in"/"write some data to" that address.

After the address, a dummy byte is sent.

Table 7-1. Register Mapping

Address	Register	Name	Access	Reset
0xFF9C	Reserved	-	-	0x01
0xFF9D	Reserved	-	-	0x01
0xFF9E	Reserved	-	-	0x27
0xFF9F	Reserved	-	-	0x0A
0xFFA0 - 0xFFAF	Peripheral AES Key Register	AES_KEY	Read/Write	0x00..00
0xFFB0 - 0xFFBF	Peripheral AES Data Field Register	AES_DATA	Read/Write	0x00..00
0xFFC0	Peripheral AES Control Register	AES_CTL	Read/Write	0x04
0xFFE2 - 0xFFE3	Reserved	-	-	0x0424
0xFFE4 - 0xFFE5		-	-	0x0424
0xFFE6 - 0xFFE7		-	-	0x0424
0xFFE8 - 0xFFE9		-	-	0x0424
0xFFEA - 0xFFEB		-	-	0x0424
0xFFEC - 0xFFED		-	-	0x0424
0xFFEE - 0xFFEF		-	-	0x0424
0xFFF0 - 0xFFF1		-	-	0x0424
0xFFF2 - 0xFFF3		-	-	0x0424
0xFFF4 - 0xFFF5		-	-	0x0424
0xFFF6 - 0xFFF7		-	-	0x0424
0xFFF8 - 0xFFF9		-	-	0x0424

8.3.1.9 Peripheral CRC Polynomial Register

Name: VCRC_POLY

Address: 0xFF0E (MSB) – 0xFF11 (LSB)

Access: Read/Write

Reset: 0x04C11DB7

31	30	..	..	..	..	1	0
VCRC_POLY (31:0)							

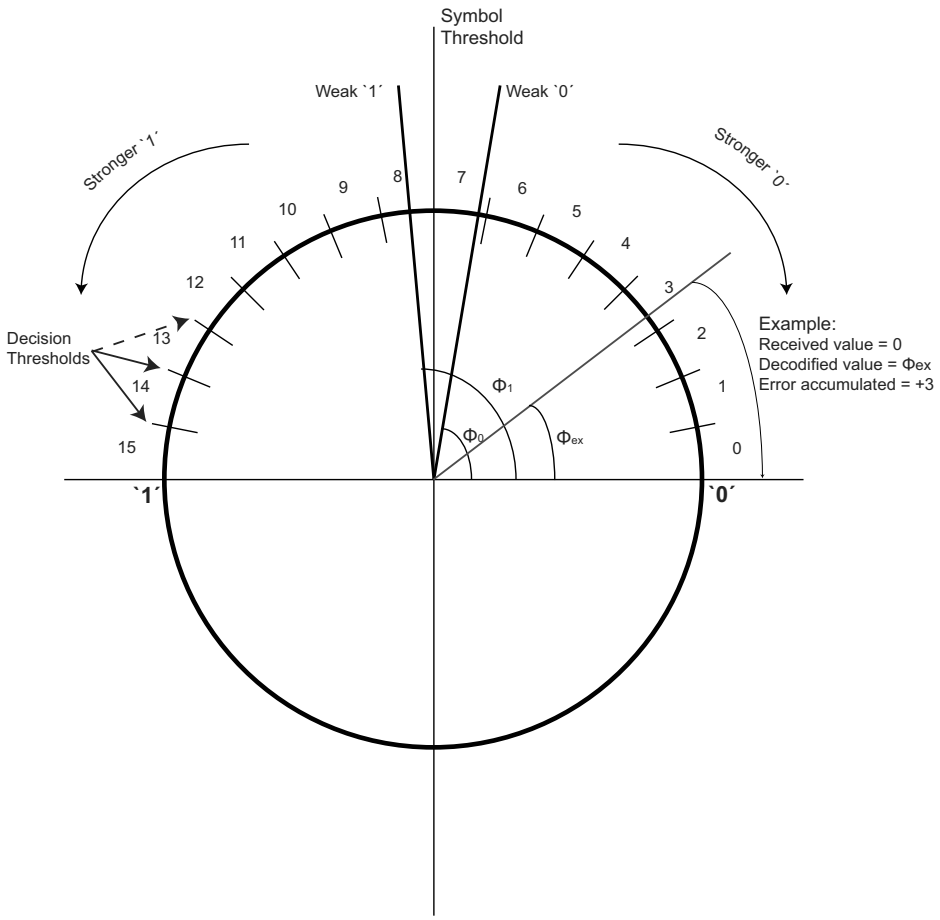
This is a 32 bits register used to store the CRC polynomial mathematical expression. Each register bit location represents an exponential degree of the polynomial. Meaning that, for a register value of 0x04C11DB7; the corresponding polynomial expression is x^32 + x^26 + x^23 + x^22 + x^16 + x^12 + x^11 + x^10 + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1. Note that, the first exponential degree (x^32) is taken by the feedback of the circuit itself.

To configure the system in CRC mode, the bit VCRC_POLY(0) must be set to ‘1’. Otherwise, if VCRC_POLY(0) is set to ‘0’ the system works in LFSR (Linear Feedback Shift Register) mode.

arithmetic average of the accumulated errors in each one of the four replicated symbols. The value is cleared by hardware each time a new message is received in BUF_RX3.

** Viterbi Soft Decision: in "soft" decision there are sixteen decision levels. Once decodified, a strong '0' is represented by a value of "0", while a strong '1' is represented by a value of "15". The rest of values are intermediate, so "7" is used to represent a weak '0' and "8" represents a weak '1'. Soft decision calculates the error in one bit received as the distance in decision levels between the value received (a value in the range 0 to 15) and the corrected one (0 or 15).*

Figure 8-2. Example of Viterbi Soft detection decision levels in a BPSK constellation



8.3.3.5 False Positive Configuration Register

Name: FALSE_POSITIVE_CONFIG

Address: 0xFEC4

Access: Read/Write

Reset: 0x10

7	6	5	4	3	2	1	0
-	-	ERR_CRC8_MAC_HD	ERR_PROTOCOL	ERR_LEN	ERR_PAD_LEN	ERR_PDU	ERR_SP

Through FALSE_POSITIVE_CONFIG register the user is able to configure FALSE_POSITIVE register behavior. When a flag of this register is set to '1', the correspondent field of the packet is included in the false positive computation algorithm. False positive algorithm is only enabled in PRIME v1.3 mode. See "False Positive Counter Register"

- **ERR_CRC8_MAC_HD:**

  Bad CRC8 MAC value (The one located at the header part of the packet).

- **ERR_PROTOCOL:**

  Unsupported protocol field.

- **ERR_LEN:**

  Invalid LEN field value. LEN field is located in the PRIME PPDU header and it defines the length of the payload (after coding) in OFDM symbols. See PRIME specification for further details about PPDU structure.

- **ERR_PAD_LEN:**

  Invalid PAD_LEN value. PAD_LEN field is located in the PRIME PPDU header and it defines the length of the PAD field (after coding) in bytes. See PRIME specification for further details about PPDU structure.

- **ERR_PDU:**

  Unsupported Header Type.

- **ERR_SP:**

  Unsupported Security Protocol.

9.3 PHY Layer Registers

9.3.1 PHY Configuration Registers

9.3.1.1 PHY Layer Special Function Register

Name: PHY_SFR

Address: 0xFE2A

Access: Read/Write

Reset: 0x87

7	6	5	4	3	2	1	0
BCH_ERR	CD	UMD	-	-	-	-	INT_PHY

- **BCH_ERR: Busy Channel Error Flag**

  This bit is cleared to ‘0’ by hardware to indicate the presence of an OFDM signal at the transmission instant. Otherwise, this field value is ‘1’.

  This bit is used for returning a result of “Busy Channel” in the PHY_DATA confirm primitive (see PRIME specification).

- **CD: Carrier Detect bit**

  This bit is set to ‘1’ by hardware when an OFDM signal is detected, and it is active during the whole reception.

  This bit is used in channel access (CSMA-CA algorithm) for performing channel-sensing.

- **UMD: Unsupported Modulation Scheme flag**

  This flag is set to ‘1’ by hardware every time a header with correct CRC is received, but the PROTOCOL field in this header indicates a modulation scheme not supported by the system.

- **INT_PHY: Physical Layer interruption**

  This bit is internally connected to the EINT pin.

  It is Low level active and it is set to '0' by the PHY layer to trigger an interrupt in the external host.

  In reception, every time a PLC message is received, the PHY layer generates two interrupts. One of them when the physical header is correctly received (two first symbols), and the other one when the message is completely received.

  In transmission, an interrupt will be generated every time a complete message has been sent.

  The signal is cleared by writing '1' in the bit PHY_SFR(0).

9.3.1.2 Channel selector Register

Name: CTPS

Address: 0xFEFA (MSB) – 0xFEFD (LSB)

Access: Read/Write

Reset: 0x000150C7

31	30	29	28	27	26	25	24
-	-	-	-	-	-	-	CTPS (24)
23	22	21	20	19	18	17	16
CTPS(23:16)							
15	14	13	12	11	10	9	8
CTPS(15:8)							
7	6	5	4	3	2	1	0
CTPS(7:0)							

Configures the channel:

Value	Name	Description
0x000150C7	CHANNEL1	42 - 89 kHz
0x00026A44	CHANNEL2	97 - 144 kHz
0x000383C1	CHANNEL3	151 - 198 kHz
0x00049D3D	CHANNEL4	206 - 253 kHz
0x0005B6BA	CHANNEL5	261 - 308 kHz
0x0006D036	CHANNEL6	315 - 362 kHz
0x0007E9B3	CHANNEL7	370 - 417 kHz
0x00090330	CHANNEL8	425 - 472 kHz

9.3.2.3 RX Interrupts Register

Name: TXRXBUF_RX_INT

Address: 0xFDD4

Access: Read/Write

Reset: 0x00

7	6	5	4	3	2	1	0
PI_RX3	PI_RX2	PI_RX1	PI_RX0	HI_RX3	HI_RX2	HI_RX1	HI_RX0

Interrupt Reception Register: When there is some issue with the reception, the micro is warned and then micro tests what buffer is affected through this register.

- **PI_RX3: Notice Payload Interrupt Reception Buffer 3**
- **PI_RX2: Notice Payload Interrupt Reception Buffer 2**
- **PI_RX1: Notice Payload Interrupt Reception Buffer 1**
- **PI_RX0: Notice Payload Interrupt Reception Buffer 0**
- **HI_RX3: Notice Header Interrupt Reception Buffer 3**
- **HI_RX2: Notice Header Interrupt Reception Buffer 2**
- **HI_RX1: Notice Header Interrupt Reception Buffer 1**
- **HI_RX0: Notice Header Interrupt Reception Buffer 0**

9.3.2.6 Robust RX Mode Register

Name: TXRXBUF_RXCONF_ROBO_MODE

Address: 0xFDF3

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
RC_RX3		RC_RX2		RC_RX1		RC_RX0	

This register shows the reception mode of each RX buffer:

- **RC_RX0:** Buffer 0 reception mode.
- **RC_RX1:** Buffer 1 reception mode.
- **RC_RX2:** Buffer 2 reception mode.
- **RC_RX3:** Buffer 3 reception mode.

Value	Name	Description
0	PRIME 1.3	Mode PRIME v1.3
1	Reserved	Reserved
2	PRIME 1.4	PRIME v1.4 reception mode
3	PRIME 1.4 c	PRIME v1.4 reception backwards compatible mode

9.3.3.3 Maximum RSSI Registers

Name: TXRXBUF_RSSIMAX_RX0

Address: 0xFD73

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIMAX_RX0							

This register stores the maximum RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX0. The measurement is done at symbol level. The value is stored in dB.

Name: TXRXBUF_RSSIMAX_RX1

Address: 0xFD74

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIMAX_RX1							

This register stores the maximum RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX1. The measurement is done at symbol level. The value is stored in dB.

Name: TXRXBUF_RSSIMAX_RX2

Address: 0xFD75

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIMAX_RX2							

This register stores the maximum RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX2. The measurement is done at symbol level. The value is stored in dB.

Name: TXRXBUF_RSSIMAX_RX3

Address: 0xFD76

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIMAX_RX3							

This register stores the maximum RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX3. The measurement is done at symbol level. The value is stored in dB.

9.3.3.5 Average CINR Registers

Name: TXRXBUF_CINRAVG_RX0

Address: 0xFD7B

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_CINRAVG_RX0							

This register stores the average CINR (Carrier to Interference + Noise ratio) value measured in the last message received in BUF_RX0. The measurement is done at symbol level. The value is stored in ¼ dB steps.

Name: TXRXBUF_CINRAVG_RX1

Address: 0xFD7C

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_CINRAVG_RX1							

This register stores the average CINR (Carrier to Interference + Noise ratio) value measured in the last message received in BUF_RX1. The measurement is done at symbol level. The value is stored in ¼ dB steps.

Name: TXRXBUF_CINRAVG_RX2

Address: 0xFD7D

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_CINRAVG_RX2							

This register stores the average CINR (Carrier to Interference + Noise ratio) value measured in the last message received in BUF_RX2. The measurement is done at symbol level. The value is stored in ¼ dB steps.

Name: TXRXBUF_CINRAVG_RX3

Address: 0xFD7E

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_CINRAVG_RX3							

This register stores the average CINR (Carrier to Interference + Noise ratio) value measured in the last message received in BUF_RX3. The measurement is done at symbol level. The value is stored in ¼ dB steps.

9.3.4.2 Signal Amplitude Registers

Name: TXRXBUF_SGNL_AMP_TX0
Address: 0xFD24
Access: Read/Write
Reset: 0x60

7	6	5	4	3	2	1	0
TXRXBUF_SGNL_AMP_TX0							

This register stores the amplitude value for the transmitted frame (only header+payload; chirp not affected), when BUF_TX0 is used. If this value is equal to 0xFF, the header+payload transmitted are not attenuated. If this register is equal to 0x00, the header+payload are nullified.

Name: TXRXBUF_SGNL_AMP_TX1
Address: 0xFD25
Access: Read/Write
Reset: 0x60

7	6	5	4	3	2	1	0
TXRXBUF_SGNL_AMP_TX1							

This register stores the amplitude value for the transmitted frame (only header+payload; chirp not affected), when BUF_TX1 is used. If this value is equal to 0xFF, the header+payload transmitted are not attenuated. If this register is equal to 0x00, the header+payload are nullified.

Name: TXRXBUF_SGNL_AMP_TX2
Address: 0xFD26
Access: Read/Write
Reset: 0x60

7	6	5	4	3	2	1	0
TXRXBUF_SGNL_AMP_TX2							

This register stores the amplitude value for the transmitted frame (only header+payload; chirp not affected), when BUF_TX2 is used. If this value is equal to 0xFF, the header+payload transmitted are not attenuated. If this register is equal to 0x00, the header+payload are nullified.

Name: TXRXBUF_SGNL_AMP_TX3
Address: 0xFD27
Access: Read/Write
Reset: 0x60

7	6	5	4	3	2	1	0
TXRXBUF_SGNL_AMP_TX3							

This register stores the amplitude value for the transmitted frame (only header+payload; chirp not affected), when BUF_TX3 is used. If this value is equal to 0xFF, the header+payload transmitted are not attenuated. If this register is equal to 0x00, the header+payload are nullified.

9.3.5 TX Buffers Registers

9.3.5.1 TX Time Registers

Name: TXRXBUF_EMITIME_TX0
Address: 0xFD00 - 0xFD03
Access: Read/Write
Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_EMITIME_TX0 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_EMITIME_TX0 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_EMITIME_TX0 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_EMITIME_TX0 (7:0)							

Transmission time of Buffer 0.

Name: TXRXBUF_EMITIME_TX1
Address: 0xFD04 - 0xFD07
Access: Read/Write
Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_EMITIME_TX1 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_EMITIME_TX1 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_EMITIME_TX1 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_EMITIME_TX1 (7:0)							

Transmission time of Buffer 1.

Name: TXRXBUF_EMITIME_TX2
Address: 0xFD08 - 0xFD0B
Access: Read/Write
Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_EMITIME_TX2 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_EMITIME_TX2 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_EMITIME_TX2 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_EMITIME_TX2 (7:0)							

Transmission time of Buffer 2.

Name: TXRXBUF_EMITIME_TX3
Address: 0xFD0C - 0xFD0F
Access: Read/Write
Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_EMITIME_TX3 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_EMITIME_TX3 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_EMITIME_TX3 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_EMITIME_TX3 (7:0)							

Transmission time of Buffer 3.

These registers contain the time value (referenced to the 20-bit PHY layer global timer) when a programmed transmission in the corresponding buffer shall begin.

Name: TXRXBUF_TXCONF_TX2

Address: 0xFD3E

Access: Read/Write

Reset: 0xA0

7	6	5	4	3	2	1	0
-	TRS2	ATR2	-	FE2	EB2	DC2	DR2

- **TRS2: TxRx established by software in buffer 2.** TxRx established by software for activated/deactivated TXRX signal before/after each transmission to work properly transistors when this feature has been selected.
  0: Disabled
  1: Enabled
- **ATR2: TxRx control mode in buffer 2.** Establishing software/hardware control of TXRX signal for transmitting.
  1**:** by hardware
  0: by software
- **FE2: Transmission forced/unforced in buffer 2.** When force transmission is required, if it is possible (Carrier Detection or Reception are in course and not disable) and suitable buffer is enabled, a transmission is immediately started.
  0: Transmission unforced
  1: Transmission forced
- **EB2: Buffer 0 enabled/disabled in buffer 2.** Enable buffer that it has been required.
  0: Disabled
  1: Enabled
- **DC2: Carrier Detect enabled/disabled for transmission in buffer 2.** Starting transmission though carrier detection is in course.
  0: Enabled
  1: Disabled
- **DR2: Reception enabled/disabled for transmission in buffer 2.** Starting transmission though reception is in course.
  0: Enabled
  1: Disabled

9.3.6.2 TXRX Polarity Selector Register

Name: AFE_CTL

Address: 0xFE90

Access: Read/Write

Reset: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	-	-	TXRX1_POL	TXRX0_POL

- **TXRX1_POL: TXRX1 pin polarity control**
  0: TXRX1 pin output = ‘0’ in transmission and ‘1’ in reception.
  1: TXRX1 pin output = ‘1’ in transmission and ‘0’ in reception.

- **TXRX0_POL: TXRX0 pin polarity control**
  0: TXRX0 pin output = ‘0’ in transmission and ‘1’ in reception.
  1: TXRX0 pin output = ‘1’ in transmission and ‘0’ in reception.

Name: TXRXBUF_ZCT_RX2

Address: 0xFD9B - 0xFD9E

Access: Read-only

Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_ZCT_RX2 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_ZCT_RX2 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_ZCT_RX2 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_ZCT_RX2 (7:0)							

Instant in time at which the last zero-cross event took place, at the end of the last message received in BUF_RX2. It is expressed in 10 µs steps. It is set by hardware and is a read-only register. This register is used by the physical layer for being in accordance with PRIME specification.

Name: TXRXBUF_ZCT_RX3

Address: 0xFD9F - 0xFDA2

Access: Read-only

Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_ZCT_RX3 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_ZCT_RX3 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_ZCT_RX3 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_ZCT_RX3 (7:0)							

Instant in time at which the last zero-cross event took place, at the end of the last message received in BUF_RX3. It is expressed in 10 µs steps. It is set by hardware and is a read-only register. This register is used by the physical layer for being in accordance with PRIME specification.

10.2 Recommended Operating Conditions

Table 10-2. Recommended Operating Conditions

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Supply Voltage	VDDIO	3.00	3.30	3.60	V
	VDDIN AN	3.00	3.30	3.60	
	VDDIN	3.00	3.30	3.60	
	VDDPLL	1.08	-	1.32	
Junction Temperature	T_J	-40	25	125	ºC
Ambient Temperature	T_A	-40	-	85	

Table 10-3. Thermal Data

Parameter	Symbol	Conditions		LQFP80	Unit
		PCB Layers	Air Speed		
Thermal resistance junction-to-ambient steady state	$R_{Theta-ja}$	2	0 m/s	64	ºC/W
			1 m/s	56	
			3 m/s	48	
		4	0 m/s	43	
			1 m/s	40	
			3 m/s	36	

Theta-ja is calculated based on a standard JEDEC defined environment and is not reliable indicator of a device's thermal performance in a non-JEDEC environment. The customer should always perform their own calculations/simulations to ensure that their system's thermal performance is sufficient.