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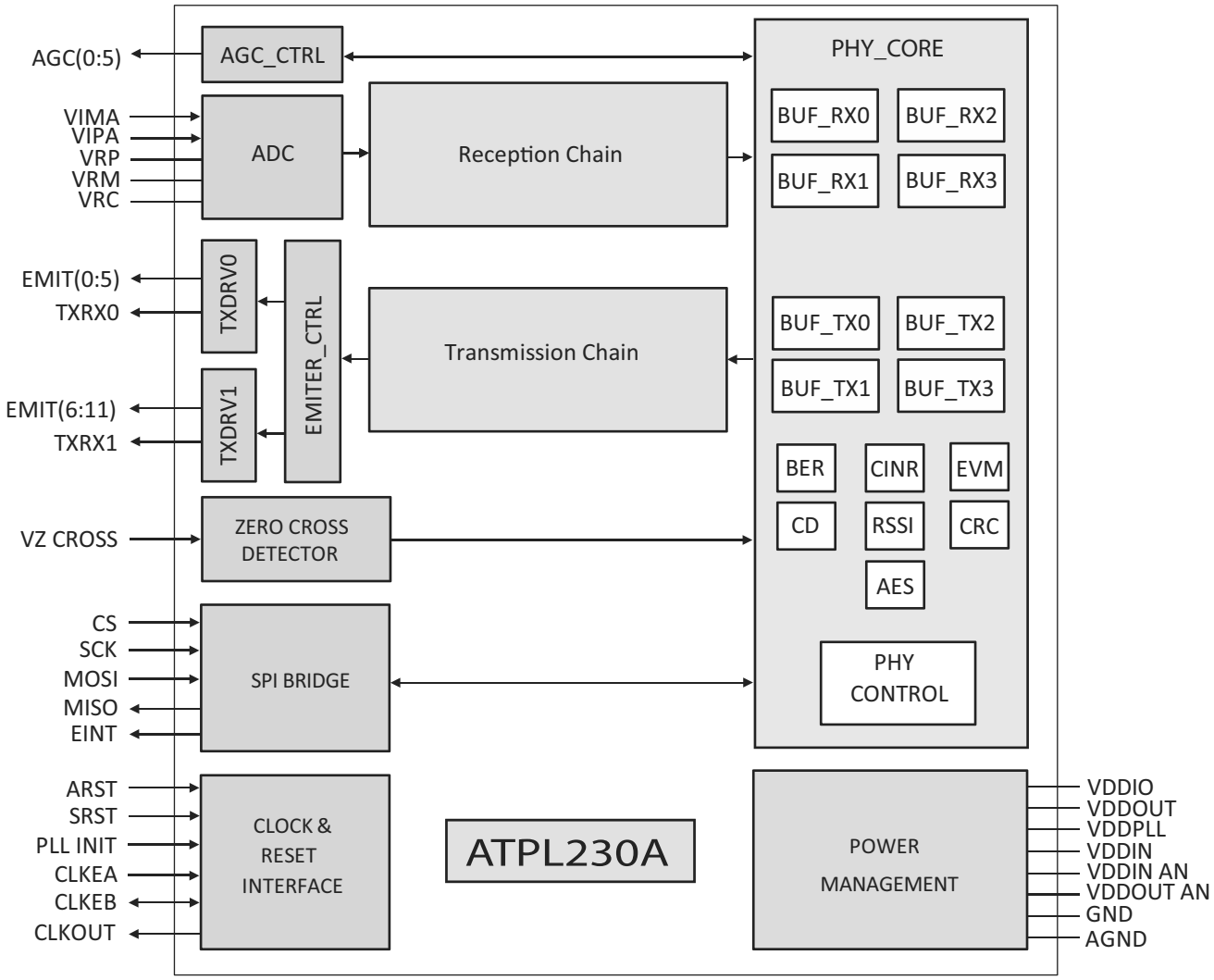
What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Power Line Communications
Core Processor	External
Program Memory Type	-
Controller Series	-
RAM Size	-
Interface	SPI
Number of I/O	-
Voltage - Supply	3V ~ 3.6V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atpl230a-aku-y

2. Block Diagram

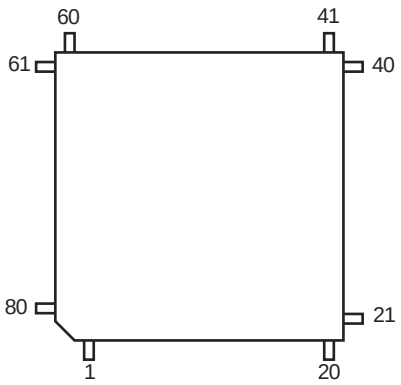
Figure 2-1. ATPL230A Functional Block Diagram



4. Package and Pinout

4.1 80-Lead LQFP Package Outline

Figure 4-1. Orientation of the 80-Lead LQFP Package



4.2 80-Lead LQFP Pinout

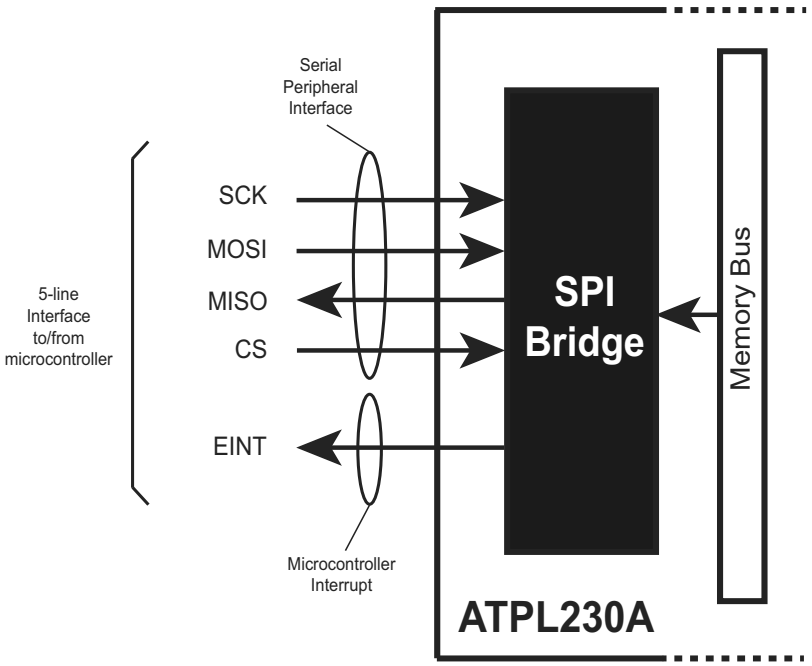
Table 4-1. 80 - Lead LQFP Pinout

1	NC	21	VDDIO	41	GND	61	GND
2	NC	22	NC	42	EMIT8	62	AGND
3	NC	23	CLKOUT	43	EMIT9	63	VDDOUT AN
4	ARST	24	CS	44	EMIT10	64	VIMA
5	PLL INIT	25	SCK	45	EMIT11	65	VIPA
6	GND	26	MOSI	46	VDDIO	66	VDDOUT AN
7	CLKEA	27	MISO	47	GND	67	AGND
8	GND	28	VDDIO	48	VDDOUT	68	VRP
9	CLKEB	29	GND	49	TXRX0	69	VRM
10	VDDIO	30	EMIT0	50	TXRX1	70	VRC
11	GND	31	EMIT1	51	GND	71	VDDIN AN
12	VDDPLL	32	EMIT2	52	AGC2	72	AGND
13	GND	33	EMIT3	53	AGC5	73	AGND
14	VDDIN	34	VDDIO	54	AGC1	74	VDDIN AN
15	VDDIN	35	GND	55	AGC4	75	GND
16	GND	36	EMIT4	56	AGC0	76	VDDIO
17	VDDOUT	37	EMIT5	57	AGC3	77	VZ CROSS
18	GND	38	EMIT6	58	VDDIO	78	NC
19	NC	39	EMIT7	59	GND	79	NC
20	SRST	40	VDDIO	60	EINT	80	NC

6. SPI Controller

ATPL230A has been conceived to be easily managed by an external microcontroller through a 5-line interface. This interface is comprised of a 4-line standard Serial Peripheral Interface (SPI) and an additional line used as interrupt from the ATPL230A to the external microcontroller. A diagram is shown below.

Figure 6-1. SPI Controller Block Diagram



By means of this SPI interface, an external microcontroller can access the ATPL230A and can carry out “write”, “write_rep”, “read” and “mask” operations. All the “Peripheral Registers” in ATPL230A are reachable via the SPI interface, thus the microcontroller can fully manage and control the ATPL230A (PHY layer, MAC co-processing, etc).

6.1 Serial Peripheral Interface

The Serial Peripheral Interface Bus or SPI bus is a synchronous serial data link standard. Devices communicate in master/slave mode where the master device initiates the data frame. Multiple slave devices are allowed with individual slave select (chip select) lines.

Figure 6-2. SPI Communication Example in ATPL230A

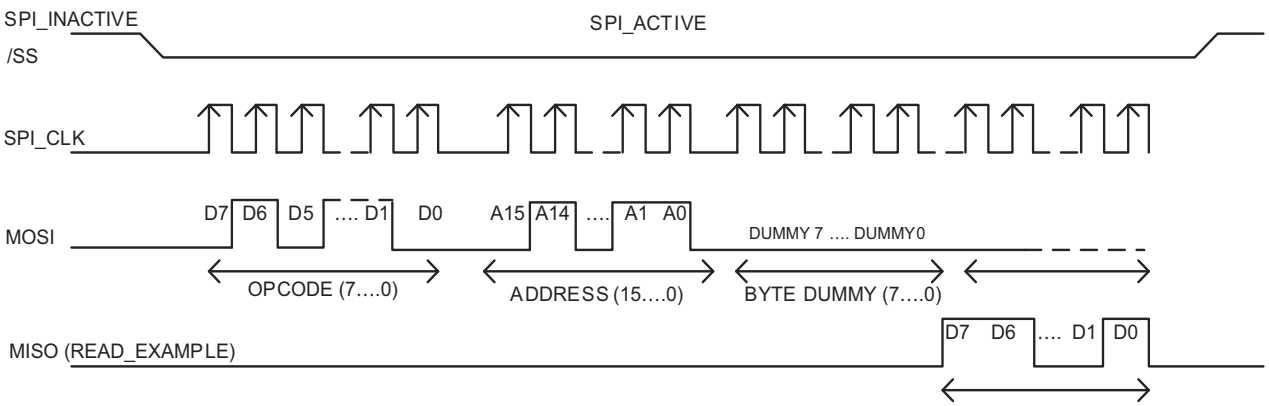


Table 7-1. Register Mapping

Address	Register	Name	Access	Reset
0xFEB7	Reserved	-	-	0x00
0xFEBA - 0xFEBB	CRC32 Errors Counter Register	ERR_CRC32_MAC	Read-only	0x0000
0xFEBC - 0xFEBD	CRC8 Errors Counter Register	ERR_CRC8_MAC	Read-only	0x0000
0xFEC0 - 0xFEC1	CRC8 HD Errors Counter Register	ERR_CRC8_MAC_HD	Read-only	0x0000
0xFEC2 - 0xFEC3	CRC8 PHY Errors Counter Register	ERR_CRC8_PHY	Read-only	0x0000
0xFEC4	False Positive Configuration Register	FALSE_POSITIVE_CONFIG	Read/Write	0x10
0xFEC5 - 0xFEC6	False Positive Counter Register	FALSE_POSITIVE	Read-only	0x0000
0xFEC8	Reserved	-	-	0x3F
0xFEC9	Reserved	-	-	0x3F
0xFECA	Reserved	-	-	0x3F
0xFECB	Reserved	-	-	0x3F
0xFECC	Reserved	-	-	0x3F
0xFECD	Reserved	-	-	0x3F
0xFECE - 0xFECF	Reserved	-	-	0x0000
0xFED3	Reserved	-	-	0x40
0xFED5 - 0xFED6	Reserved	-	-	0x0000
0xFEDB	Reserved	-	-	0x00
0xFEDC - 0xFEDF	Reserved	-	-	0x00..00
0xFEE0	Reserved	-	-	0x02
0xFEE4 - 0xFEE5	Reserved	-	-	0x0000
0xFEE6 - 0xFEE7	Reserved	-	-	0x0000
0xFEE8	Reserved	-	-	0x00
0xFEE9	Reserved	-	-	0xFF
0xFEEA	Reserved	-	-	0x04
0xFEEB	Reserved	-	-	0x08
0xFEEC	Reserved	-	-	0x0C
0xFEED	Reserved	-	-	0x14
0xFEEE	Reserved	-	-	0x00
0xFEEF	Reserved	-	-	0x03
0xFEF0	Reserved	-	-	0x00
0xFEF1	Reserved	-	-	0x17
0xFEF2	Reserved	-	-	0x18
0xFEF3	Reserved	-	-	0x23
0xFEF4	CRC PRIMEPLUS Configuration Register	PRIMEPLUS_CRC_CONFIG	Read/Write	0x14
0xFEF5 - 0xFEF6	CRC PRIMEPLUS Polynomial Register	PRIMEPLUS_CRC_POLY	Read/Write	0x080F
0xFEF7 - 0xFEF8	CRC PRIMEPLUS Reset Value Register	PRIMEPLUS_CRC_RST	Read/Write	0x0000

Table 7-1. Register Mapping

Address	Register	Name	Access	Reset
0xFEFA - 0xFEFD	Channel Selector Register	CTPS	Read/Write	0x000150C7
0xFEFE	Reserved	-	-	0x00
0xFF00 - 0xFF07	Reserved	-	-	0x411A1803 73D6893C
0xFF09 - 0xFF0A	Reserved	-	-	0x0EA5
0xFF0E - 0xFF11	Peripheral CRC Polynomial Register	VCRC_POLY	Read/Write	0x04C11DB7
0xFF12 - 0xFF15	Peripheral CRC Reset Value Register	VCRC_RST	Read/Write	0x00..00
0xFF16	Peripheral CRC Configuration Register	VCRC_CONF	Read/Write	0xC3
0xFF17	Peripheral CRC Input Register	VCRC_INPUT	Read/Write	0x00
0xFF18	Peripheral CRC Control Register	VCRC_CTL	Read/Write	0x00
0xFF19 - 0xFF1C	Peripheral CRC Value Register	VCRC_CRC	Read-only	0x00..00
0xFF1E	Zero Crossing Configuration Register	ZC_CONFIG	Read/Write	0x00
0xFF1F - 0xFF20	Reserved	-	-	0x051E
0xFF21 - 0xFF22	Reserved	-	-	0x8000
0xFF23	Zero Crossing Filter Register	ZC_FILTER	Read/Write	0xB2
0xFF24 - 0xFF27	Reserved	-	-	0x00030D40
0xFF28 - 0xFF2B	Reserved	-	-	0x00..00
0xFF2D	Reserved	-	-	0x01
0xFF33 - 0xFF36	Reserved	-	-	0x00..00
0xFF37 - 0xFF38	Reserved	-	-	0x0000
0xFF39	Reserved	-	-	0x14
0xFF3A	Reserved	-	-	0x80
0xFF3B	Reserved	-	-	0x70
0xFF3C	Reserved	-	-	0xC8
0xFF3D	Reserved	-	-	0x0A
0xFF3E	Reserved	-	-	0x02
0xFF3F	Reserved	-	-	0x04
0xFF40	Reserved	-	-	0x01
0xFF41	Reserved	-	-	0x01
0xFF42	Reserved	-	-	0x27
0xFF43	Reserved	-	-	0x0A
0xFF4C	Reserved	-	-	0xA8
0xFF51	Reserved	-	-	0x99
0xFF52	Reserved	-	-	0xC0
0xFF53	Reserved	-	-	0x00
0xFF54	Reserved	-	-	0x03
0xFF55	Reserved	-	-	0x99
0xFF56	Reserved	-	-	0x99

8. MAC Coprocessor

ATPL230A accelerators can be used to perform PRIME MAC-specific tasks by hardware, decreasing CPU load from the external MCU/MPU. For that purpose, Cyclic Redundance Check (CRC) and AES128 encryption blocks are available in ATPL230A.

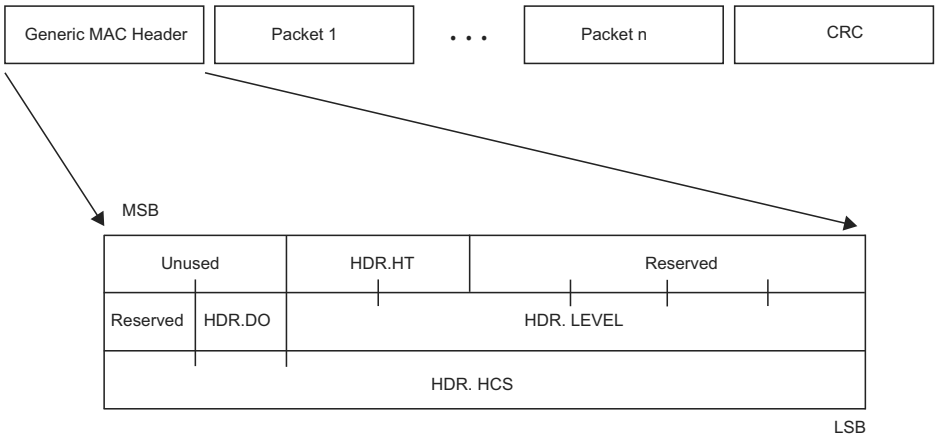
Please refer to Atmel doc43048 “Atmel PRIME Implementation” for Atmel software package detailed description and functionality.

8.1 Cyclic Redundancy Check (CRC)

8.1.1 PRIME v1.3 CRC

There are three types of MAC PDUs (generic, promotion and beacon) for different purposes, and each one has its own specific CRC. There is a hardware implementation of every CRC type calculated by the MAC layer. This CRC hardware-calculation is enabled by default. Note that the CRC included at the physical layer is also a hardware implementation available (enabled by default).

Figure 8-1. Example: Generic MAC PDU format and generic MAC header detail



In transmission all CRC bytes are real-time calculated and the last bytes of the MAC PDU are overwritten with these values, (provided that the field HT in the first byte of the MAC header in transmission data is equal to the corresponding MAC PDU type).

In reception the CRC bytes are also real-time calculated and these bytes are checked with the last bytes of the MAC PDU. If the CRC is not correct, then an error flag is activated, the complete frame is discarded, and the corresponding error counter is increased. These counters allow the MAC layer to take decisions according to error ratio.

For the Generic MAC PDU, there is an 8-bit CRC in the Generic MAC header, which corresponds to PRIME HDR.HCS. In reception, if this CRC doesn’t check successfully, the current frame is discarded and no interruption is generated.

This works in the same way as CRC for the PHY layer (CRC Ctrl, located in the PHY header, see PRIME specification for further information).

There is another CRC for the Generic MAC PDU which is the last field of the GPDU. It is 32 bits long and it is used to detect transmission errors. The CRC shall cover the concatenation of the SNA with the GPDU except for the CRC field itself. In reception, if the CRC is not successful then an internal flag is set and the error counter is increased.

For the Promotion Needed PDU there is an 8-bit CRC, calculated with the first 13 bytes of the header. In reception, if this CRC is not correct, then an internal flag is set and the corresponding error counter is increased.

For the Beacon PDU there is a 32-bit CRC calculated with the same algorithm as the one defined for the CRC of the Generic MAC PDU. This CRC shall be calculated over the complete BPDU except for the CRC field itself. In reception, if this CRC is not successful, then an internal flag is set and the same error counter used for GPDU is increased. The hardware used for this CRC is the same as the one used for GPDU.

8.3.1.9 Peripheral CRC Polynomial Register

Name: VCRC_POLY

Address: 0xFF0E (MSB) – 0xFF11 (LSB)

Access: Read/Write

Reset: 0x04C11DB7

31	30	..	..	..	..	1	0
VCRC_POLY (31:0)							

This is a 32 bits register used to store the CRC polynomial mathematical expression. Each register bit location represents an exponential degree of the polynomial. Meaning that, for a register value of 0x04C11DB7; the corresponding polynomial expression is x^32 + x^26 + x^23 + x^22 + x^16 + x^12 + x^11 + x^10 + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1. Note that, the first exponential degree (x^32) is taken by the feedback of the circuit itself.

To configure the system in CRC mode, the bit VCRC_POLY(0) must be set to ‘1’. Otherwise, if VCRC_POLY(0) is set to ‘0’ the system works in LFSR (Linear Feedback Shift Register) mode.

8.3.1.12 Peripheral CRC Input Register

Name: VCRC_INPUT

Address: 0xFF17

Access: Read/Write

Reset: 0x00

7	6	5	4	3	2	1	0
VCRC_INPUT (7:0)							

This is an 8 bits register used to write the input bytes for CRC calculations. Each time a byte has been written in this register, the VCRC block detects the byte automatically and initiates the operation adding this new byte to previous calculations.

8.3.3.4 BER HARD Maximum Error Registers

Name: TXRXBUF_BERHARD_MAX_RX0
Address: 0xFD67
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERHARD_MAX_RX0							

Used only in PRIME v1.4 mode. After a message is received in BUF_RX0, this register stores the logarithm of the maximum error of the four replicated symbols, regarding the number of received bits, using Viterbi hard* decision. The value is cleared by hardware each time a new message is received in BUF_RX0.

Name: TXRXBUF_BERHARD_MAX_RX1
Address: 0xFD68
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERHARD_MAX_RX1							

Used only in PRIME v1.4 mode. After a message is received in BUF_RX1, this register stores the logarithm of the maximum error of the four replicated symbols, regarding the number of received bits, using Viterbi hard* decision. The value is cleared by hardware each time a new message is received in BUF_RX1.

Name: TXRXBUF_BERHARD_MAX_RX2
Address: 0xFD69
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERHARD_MAX_RX2							

Used only in PRIME v1.4 mode. After a message is received in BUF_RX2, this register stores the logarithm of the maximum error of the four replicated symbols, regarding the number of received bits, using Viterbi hard* decision. The value is cleared by hardware each time a new message is received in BUF_RX2.

Name: TXRXBUF_BERHARD_MAX_RX3
Address: 0xFD6A
Access: Read-only
Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_BERHARD_MAX_RX3							

Used only in PRIME v1.4 mode. After a message is received in BUF_RX3, this register stores the logarithm of the maximum error of the four replicated symbols, regarding the number of received bits, using Viterbi hard* decision. The value is cleared by hardware each time a new message is received in BUF_RX3.

8.3.3.5 False Positive Configuration Register

Name: FALSE_POSITIVE_CONFIG

Address: 0xFEC4

Access: Read/Write

Reset: 0x10

7	6	5	4	3	2	1	0
-	-	ERR_CRC8_MAC_HD	ERR_PROTOCOL	ERR_LEN	ERR_PAD_LEN	ERR_PDU	ERR_SP

Through FALSE_POSITIVE_CONFIG register the user is able to configure FALSE_POSITIVE register behavior. When a flag of this register is set to '1', the correspondent field of the packet is included in the false positive computation algorithm. False positive algorithm is only enabled in PRIME v1.3 mode. See "False Positive Counter Register"

- **ERR_CRC8_MAC_HD:**

  Bad CRC8 MAC value (The one located at the header part of the packet).

- **ERR_PROTOCOL:**

  Unsupported protocol field.

- **ERR_LEN:**

  Invalid LEN field value. LEN field is located in the PRIME PPDU header and it defines the length of the payload (after coding) in OFDM symbols. See PRIME specification for further details about PPDU structure.

- **ERR_PAD_LEN:**

  Invalid PAD_LEN value. PAD_LEN field is located in the PRIME PPDU header and it defines the length of the PAD field (after coding) in bytes. See PRIME specification for further details about PPDU structure.

- **ERR_PDU:**

  Unsupported Header Type.

- **ERR_SP:**

  Unsupported Security Protocol.

Name: TXRXBUF_RECTIME_RX3
Address: 0xFD8F – 0xFD92
Access: Read-only
Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_RECTIME_RX3 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_RECTIME_RX3 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_RECTIME_RX3 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_RECTIME_RX3 (7:0)							

Reception Time in Buffer 3.

When there has been a reception, these registers show when it happened.

9.3.2.2 Buffer Selection Register

Name: TXRXBUF_SELECT_BUFF_RX

Address: 0xFDD3

Access: Read/Write

Reset: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	SB3	SB2	SB1	SB0

Select Reception Buffer: It is used to establish what reception buffers are active.

- **SB0: Select Buffer 0**
  0: Disable Buffer
  1: Enable Buffer
- **SB1: Select Buffer 1**
  0: Disable Buffer
  1: Enable Buffer
- **SB2: Select Buffer 2**
  0: Disable Buffer
  1: Enable Buffer
- **SB3: Select Buffer 3**
  0: Disable Buffer
  1: Enable Buffer

9.3.3.2 Average RSSI Registers

Name: TXRXBUF_RSSIAVG_RX0

Address: 0xFD6F

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIAVG_RX0							

This register stores the average RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX0. The measurement is done at symbol level. The value is stored in dB.

Name: TXRXBUF_RSSIAVG_RX1

Address: 0xFD70

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIAVG_RX1							

This register stores the average RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX1. The measurement is done at symbol level. The value is stored in dB.

Name: TXRXBUF_RSSIAVG_RX2

Address: 0xFD71

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIAVG_RX2							

This register stores the average RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX2. The measurement is done at symbol level. The value is stored in dB.

Name: TXRXBUF_RSSIAVG_RX3

Address: 0xFD72

Access: Read-only

Reset: 0x00

7	6	5	4	3	2	1	0
TXRXBUF_RSSIAVG_RX3							

This register stores the average RSSI (Received Signal Strength Indication) value measured in the last message received in BUF_RX3. The measurement is done at symbol level. The value is stored in dB.

9.3.3.7 Header EVM Registers

Name: TXRXBUF_EVM_HD_RX0

Address: 0xFDA3 - 0xFDA4

Access: Read-only

Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_EVM_HD_RX0 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_EVM_HD_RX0 (7:0)							

This register stores the maximum EVM (Error Vector Magnitude) measured in the reception of the last message header in BUF_RX0. The 7 msb, TXRXBUF_EVM_HD_RX0 (15:9), represent the integer part in %, being the TXRXBUF_EVM_HD_RX0 (8:0) bits the fractional part if more precision were required.

This register is used by the physical layer for being in accordance with PRIME specification.

Name: TXRXBUF_EVM_HD_RX1

Address: 0xFDA5 - 0xFDA6

Access: Read-only

Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_EVM_HD_RX1 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_EVM_HD_RX1 (7:0)							

This register stores the maximum EVM (Error Vector Magnitude) measured in the reception of the last message header in BUF_RX1. The 7 msb, TXRXBUF_EVM_HD_RX1 (15:9), represent the integer part in %, being the TXRXBUF_EVM_HD_RX1 (8:0) bits the fractional part if more precision were required.

This register is used by the physical layer for being in accordance with PRIME specification.

Name: TXRXBUF_EVM_HD_RX2

Address: 0xFDA7 - 0xFDA8

Access: Read-only

Reset: 0x0000

15	14	13	12	11	10	9	8
TXRXBUF_EVM_HD_RX2 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_EVM_HD_RX2 (7:0)							

This register stores the maximum EVM (Error Vector Magnitude) measured in the reception of the last message header in BUF_RX2. The 7 msb, TXRXBUF_EVM_HD_RX2 (15:9), represent the integer part in %, being the TXRXBUF_EVM_HD_RX2 (8:0) bits the fractional part if more precision were required.

This register is used by the physical layer for being in accordance with PRIME specification.

9.3.4 TX Config Registers

9.3.4.1 Global Amplitude Registers

Name: TXRXBUF_GLBL_AMP_TX0
Address: 0xFD20
Access: Read/Write
Reset: 0xFF

7	6	5	4	3	2	1	0
TXRXBUF_GLBL_AMP_TX0							

Being “Amax” the maximum voltage reachable in the external driver MOS couple, this register sets the global amplitude for the transmitted frame (chirp+header+payload), when BUF_TX0 is used, following this formula:

Name: TXRXBUF_GLBL_AMP_TX1
Address: 0xFD21
Access: Read/Write
Reset: 0xFF

7	6	5	4	3	2	1	0
TXRXBUF_GLBL_AMP_TX1							

Being “Amax” the maximum voltage reachable in the external driver MOS couple, this register sets the global amplitude for the transmitted frame (chirp+header+payload), when BUF_TX1 is used, following this formula:

Name: TXRXBUF_GLBL_AMP_TX2
Address: 0xFD22
Access: Read/Write
Reset: 0xFF

7	6	5	4	3	2	1	0
TXRXBUF_GLBL_AMP_TX2							

Being “Amax” the maximum voltage reachable in the external driver MOS couple, this register sets the global amplitude for the transmitted frame (chirp+header+payload), when BUF_TX2 is used, following this formula:

9.3.4.2 Signal Amplitude Registers

Name: TXRXBUF_SGNL_AMP_TX0
Address: 0xFD24
Access: Read/Write
Reset: 0x60

7	6	5	4	3	2	1	0
TXRXBUF_SGNL_AMP_TX0							

This register stores the amplitude value for the transmitted frame (only header+payload; chirp not affected), when BUF_TX0 is used. If this value is equal to 0xFF, the header+payload transmitted are not attenuated. If this register is equal to 0x00, the header+payload are nullified.

Name: TXRXBUF_SGNL_AMP_TX1
Address: 0xFD25
Access: Read/Write
Reset: 0x60

7	6	5	4	3	2	1	0
TXRXBUF_SGNL_AMP_TX1							

This register stores the amplitude value for the transmitted frame (only header+payload; chirp not affected), when BUF_TX1 is used. If this value is equal to 0xFF, the header+payload transmitted are not attenuated. If this register is equal to 0x00, the header+payload are nullified.

Name: TXRXBUF_SGNL_AMP_TX2
Address: 0xFD26
Access: Read/Write
Reset: 0x60

7	6	5	4	3	2	1	0
TXRXBUF_SGNL_AMP_TX2							

This register stores the amplitude value for the transmitted frame (only header+payload; chirp not affected), when BUF_TX2 is used. If this value is equal to 0xFF, the header+payload transmitted are not attenuated. If this register is equal to 0x00, the header+payload are nullified.

Name: TXRXBUF_SGNL_AMP_TX3
Address: 0xFD27
Access: Read/Write
Reset: 0x60

7	6	5	4	3	2	1	0
TXRXBUF_SGNL_AMP_TX3							

This register stores the amplitude value for the transmitted frame (only header+payload; chirp not affected), when BUF_TX3 is used. If this value is equal to 0xFF, the header+payload transmitted are not attenuated. If this register is equal to 0x00, the header+payload are nullified.

Name: TXRXBUF_EMITIME_TX3
Address: 0xFD0C - 0xFD0F
Access: Read/Write
Reset: 0x00000000

31	30	29	28	27	26	25	24
TXRXBUF_EMITIME_TX3 (31:24)							
23	22	21	20	19	18	17	16
TXRXBUF_EMITIME_TX3 (23:16)							
15	14	13	12	11	10	9	8
TXRXBUF_EMITIME_TX3 (15:8)							
7	6	5	4	3	2	1	0
TXRXBUF_EMITIME_TX3 (7:0)							

Transmission time of Buffer 3.

These registers contain the time value (referenced to the 20-bit PHY layer global timer) when a programmed transmission in the corresponding buffer shall begin.

9.3.7.2 Zero Crossing Configuration Register

Name: ZC_CONFIG

Address: 0xFF1E

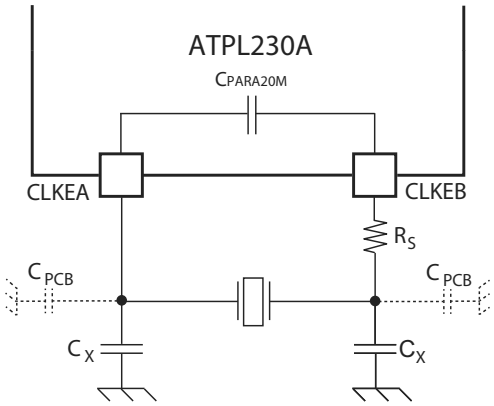
Access: Read/Write

Reset: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	MODE_REP	MODE_INV	MODE_ASC	MODE_MUX

- **MODE_REP: Repetition Mode**
  '0': No effect.
  '1': Zero Crossing Detector Input Signal period is down by half.
- **MODE_INV: Inversion Mode**
  '0': No effect.
  '1': Zero Crossing Detector Input Signal is inverted.
- **MODE_ASC: Ascent-Descent Mode**
  '0': If MODE_MUX is 1, Ascent Zero Crossing.
  '1': If MODE_MUX is 1, Descent Zero Crossing.
- **MODE_MUX: Zero Crossing Mode**
  '0': Selection of both ascent and descent zero-crossing.
  '1': Selection of ascent or descent zero-crossing.

Figure 10-5. 20 MHz Crystal Oscillator Schematic



$$C_X = 2 \times (C_{XTAL} - C_{PARA20M} - C_{PCB} / 2)$$

where C_{PCB} is the ground referenced parasitic capacitance of the printed circuit board (PCB) on CLKEA and CLKEB tracks.

As a practical example, taking the following crystal part number:

Manufacturer: TXC CORPORATION

Part Number: 9C-20.000MAAJ-T

Frequency: 20.000 MHz

Tolerance: 30 ppm (as low as possible to fullfil PRIME specification requirements)

C_{XTAL} = 18 pF

Working in a typical layout / substrate with C_{PCB} = 1 pF

The value of the external capacitors on CLKEA and CLKEB should be C_X = 2 x (18 - 4 - 0.5) = 27 pF

It is strongly recommended to use capacitors with the lowest temperature stability possible. In this practical example, a suitable part number could be:

Manufacturer: MURATA

Part Number: GRM1885C1H270FA01D

Capacitance: 27 pF

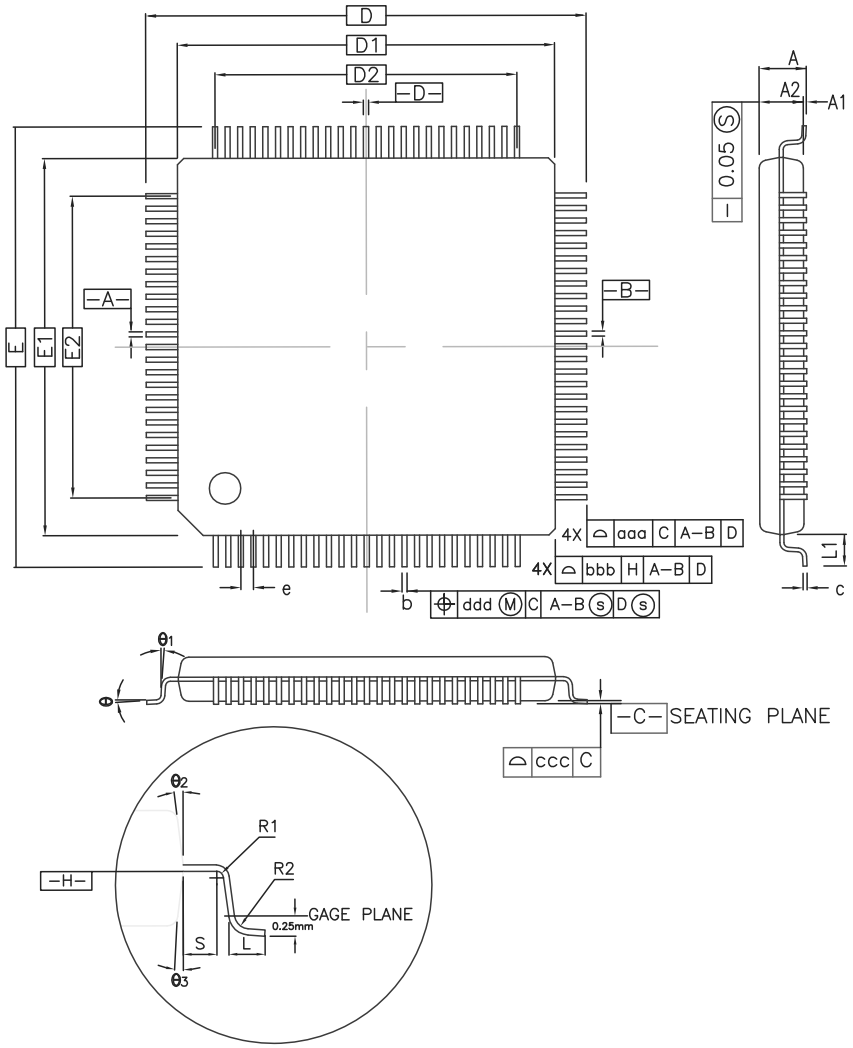
Tolerance: 1 %

Dielectric: C0G / NP0 (0 drift)

11. Mechanical Characteristics

11.1 LQFP80 Mechanical Characteristics

Figure 11-1. 80 LQFP package dimensions



CONTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
D	14.00 BSC.			0.551 BSC.		
D_1	12.00 BSC.			0.472 BSC.		
E	14.00 BSC.			0.551 BSC.		
E_1	12.00 BSC.			0.472 BSC.		
R_2	0.08	—	0.20	0.003	—	0.008
R_1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	80L					
	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D2	9.50			0.374		
E2	9.50			0.374		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		

Table 11-1. LQFP Package Reference

JEDEC Drawing Reference	MS-026

Table 11-2. LQFP Package Characteristics

Moisture Sensitivity Level	3

This package respects the recommendations of the NEMI User Group.