



Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 8x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4124lqi-443

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Figure 2. Block Diagram



The PSoC 4100 devices include extensive support for programming, testing, debugging, and tracing both hardware and firmware.

The ARM Serial\_Wire Debug (SWD) interface supports all programming and debug features of the device.

Complete debug-on-chip functionality enables full device debugging in the final system using the standard production device. It does not require special interfaces, debugging pods, simulators, or emulators. Only the standard programming connections are required to fully support debug.

The PSoC Creator Integrated Development Environment (IDE) provides fully integrated programming and debug support for the PSoC 4100 devices. The SWD interface is fully compatible with industry standard third party tools. With the ability to disable debug features, with very robust flash protection, and by allowing customer-proprietary functionality to be implemented in on-chip programmable blocks, the PSoC 4100 family provides a level of

security not possible with multi-chip application solutions or with microcontrollers.

The debug circuits are enabled by default and can only be disabled in firmware. If not enabled, the only way to re-enable them is to erase the entire device, clear flash protection, and reprogram the device with new firmware that enables debugging.

Additionally, all device interfaces can be permanently disabled (device security) for applications concerned about phishing attacks due to a maliciously reprogrammed device or attempts to defeat security by starting and interrupting flash programming sequences. Because all programming, debug, and test interfaces are disabled when maximum device security is enabled, PSoC 4100 with device security enabled may not be returned for failure analysis. This is a trade-off the PSoC 4100 allows the customer to make.



## **Functional Definition**

### CPU and Memory Subsystem

### CPU

The Cortex-M0 CPU in PSoC 4100 is part of the 32-bit MCU subsystem, which is optimized for low power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from Deep Sleep mode allowing power to be switched off to the main processor when the chip is in Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt input (NMI), which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG; the debug configuration used for PSoC 4100 has four break-point (address) comparators and two watchpoint (data) comparators.

#### Flash

PSoC 4100 has a flash module with a flash accelerator tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 0 wait-state (WS) access time at 24 MHz. Part of the flash module can be used to emulate EEPROM operation if required.

The PSoC 4200 Flash supports the following flash protection modes at the memory subsystem level:

- Open: No Protection. Factory default mode in which the product is shipped.
- Protected: User may change from Open to Protected. This mode disables Debug interface accesses. The mode can be set back to Open but only after completely erasing the Flash.
- Kill: User may change from Open to Kill. This mode disables all Debug accesses. The part cannot be erased externally, thus obviating the possibility of partial erasure by power interruption and potential malfunction and security leaks. This is an irrecvocable mode.

In addition, row-level Read/Write protection is also supported to prevent inadvertent Writes as well as selectively block Reads. Flash Read/Write/Erase operations are always available for internal code using system calls.

### SRAM

SRAM memory is retained during Hibernate.

### SROM

A supervisory ROM that contains boot and configuration routines is provided.

### System Resources

#### Power System

The power system is described in detail in the section Power on page 15. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low-voltage detect (LVD)). The PSoC 4100 operates with a single external supply over the range of 1.71 V to 5.5 V and has five different power modes, transitions between which are managed by the power system. PSoC 4100 provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

#### Clock System

The PSoC 4100 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for PSoC 4100 consists of the internal main oscillator (IMO) and the internal low-power oscillator (ILO) and provision for an external clock.

#### Figure 3. PSoC 4100 MCU Clocking Architecture



The HFCLK signal can be divided down (see PSoC 4100 MCU Clocking Architecture) to generate synchronous clocks for the analog and digital peripherals. There are a total of 12 clock dividers for PSoC 4100, each with 16-bit divide capability. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator.



### IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile latches (NVL). Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 24 MHz and it can be adjusted between 3 MHz to 24 MHz in steps of 1 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2%.

#### ILO Clock Source

The ILO is a very low power oscillator, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

#### Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

#### Reset

PSoC 4100 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration. The XRES pin has an internal pull-up resistor that is always enabled.

#### Voltage Reference

The PSoC 4100 reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal to noise ratios (SNR) and better absolute accuracy, it is possible to bypass the internal reference using a GPIO pin or to use an external reference for the SAR.

### Analog Blocks

#### 12-bit SAR ADC

The 12-bit 806 ksps SAR ADC can operate at a maximum clock rate of 14.5 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to  $\pm$ 1%) and by providing the choice (for the PSoC 4100 case) of three internal voltage references: V<sub>DD</sub>, V<sub>DD</sub>/2, and V<sub>REF</sub> (nominally 1.024 V) as well as an external reference through a GPIO pin. The sample-and-hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision providing appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, aggregate sampling bandwidth is equal to 806 ksps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.



#### Figure 4. SAR ADC System Diagram



### GPIO

PSoC 4100 has 36 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
     Input only
  - Weak pull-up with strong pull-down
  - □ Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - □ Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes).
- Selectable slew rates for dV/dt related noise control to improve EMI.

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves. Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4100 since it has 4.5 ports).

### **Special Function Peripherals**

#### LCD Segment Drive

PSoC 4100 has an LCD controller which can drive up to four commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

#### CapSense

CapSense is supported on all pins in the PSoC 4100 through a CapSense Sigma-Delta (CSD) block that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CapSense function can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another mux bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

The CapSense block has two IDACs which can be used for general purposes if CapSense is not being used.(both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

### WLCSP Package Bootloader

The WLCSP package is supplied with an I<sup>2</sup>C Bootloader installed in flash. The bootloader is compatible with PSoC Creator bootloadable project files and has the following default settings:

- I<sup>2</sup>C SCL and SDA connected to port pins P4.0 and P4.1 respectively (external pull-up resistors required)
- I<sup>2</sup>C Slave mode, address 8, data rate = 100 kbps
- Single application
- Wait two seconds for bootload command
- Other bootloader options are as set by the PSoC Creator Bootloader Component default
- Occupies the bottom 4.5 K of flash

For more information on this bootloader, see the following Cypress application notes:

#### AN73854 - Introduction to Bootloaders

Note that a PSoC Creator bootloadable project must be associated with *.hex* and *.elf* files for a bootloader project that is configured for the target device. Bootloader *.hex* and *.elf* files can be found at http://www.cypress.com/?rID=78805. The factory-installed bootloader can be overwritten using JTAG or SWD programming.



# Pinouts

The following is the pin-list for PSoC 4100 (44-TQFP, 40-QFN, 28-SSOP, and 48-TQFP). Port 2 comprises of the high-speed Analog inputs for the SAR Mux. P1.7 is the optional external input and bypass for the SAR reference. Ports 3 and 4 contain the Digital Communication channels. All pins support CSD CapSense and analog mux bus connections.

4	4-TQFP	40	D-QFN	2	8-SSOP	48	B-TQFP		Alte		Die Deserietien		
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	Pin Description
1	VSS	-	-	-	-	-	-	-	-	-	-	-	Ground
2	P2.0	1	P2.0	-	-	2	P2.0	sarmux.0	-	-	-	-	Port 2 Pin 0: gpio, lcd, csd, sarmux
3	P2.1	2	P2.1	-	-	3	P2.1	sarmux.1	-	-	-	-	Port 2 Pin 1: gpio, lcd, csd, sarmux
4	P2.2	3	P2.2	5	P2.2	4	P2.2	sarmux.2	-	-	-	-	Port 2 Pin 2: gpio, lcd, csd, sarmux
5	P2.3	4	P2.3	6	P2.3	5	P2.3	sarmux.3	-	-	-	-	Port 2 Pin 3: gpio, lcd, csd, sarmux
6	P2.4	5	P2.4	7	P2.4	6	P2.4	sarmux.4	tcpwm0_p[1]	-	-	-	Port 2 Pin 4: gpio, lcd, csd, sarmux, pwm
7	P2.5	6	P2.5	8	P2.5	7	P2.5	sarmux.5	tcpwm0_n[1]	-	-	-	Port 2 Pin 5: gpio, lcd, csd, sarmux, pwm
8	P2.6	7	P2.6	9	P2.6	8	P2.6	sarmux.6	tcpwm1_p[1]	-	-	-	Port 2 Pin 6: gpio, lcd, csd, sarmux, pwm
9	P2.7	8	P2.7	10	P2.7	9	P2.7	sarmux.7	tcpwm1_n[1]	_	_	_	Port 2 Pin 7: gpio, lcd, csd, sarmux, pwm
10	VSS	9	VSS	-	-	-	-	-	-	-	-	-	Ground
-	-	-	-	-	-	10	NC	-	-	-	-	-	No Connect
-	-	-	-	-	-	11	NC	-	-	-	-	-	No Connect
11	P3.0	10	P3.0	11	P3.0	12	P3.0	-	tcpwm0_p[0]	scb1_uart_rx[0]	scb1_i2c_scl[0]	scb1_spi_mosi[0]	Port 3 Pin 0: gpio, lcd, csd, pwm, scb1
12	P3.1	11	P3.1	12	P3.1	13	P3.1	-	tcpwm0_n[0]	scb1_uart_tx[0]	scb1_i2c_sda[0]	scb1_spi_miso[0]	Port 3 Pin 1: gpio, lcd, csd, pwm, scb1
13	P3.2	12	P3.2	13	P3.2	14	P3.2	-	tcpwm1_p[0]	-	swd_io[0]	scb1_spi_clk[0]	Port 3 Pin 2: gpio, lcd, csd, pwm, scb1, swd
-	-	-	-	-	-	15	VSSD	-	-	-	-	-	Ground
14	P3.3	13	P3.3	14	P3.3	16	P3.3	-	tcpwm1_n[0]	-	swd_clk[0]	scb1_spi_ssel_0[0]	Port 3 Pin 3: gpio, lcd, csd, pwm, scb1, swd
15	P3.4	14	P3.4	-	-	17	P3.4	-	tcpwm2_p[0]	-	-	scb1_spi_ssel_1	Port 3 Pin 4: gpio, lcd, csd, pwm, scb1
16	P3.5	15	P3.5	-	-	18	P3.5	-	tcpwm2_n[0]	-	-	scb1_spi_ssel_2	Port 3 Pin 5: gpio, lcd, csd, pwm, scb1
17	P3.6	16	P3.6	-	-	19	P3.6	-	tcpwm3_p[0]	-	swd_io[1]	scb1_spi_ssel_3	Port 3 Pin 6: gpio, lcd, csd, pwm, scb1, swd
18	P3.7	17	P3.7	-	-	20	P3.7	-	tcpwm3_n[0]	-	swd_clk[1]	-	Port 3 Pin 7: gpio, lcd, csd, pwm, swd
19	VDDD	-	-	-	-	21	VDDD	-	-	-	-	-	Digital Supply, 1.8 - 5.5V
20	P4.0	18	P4.0	15	P4.0	22	P4.0	-	-	scb0_uart_rx	scb0_i2c_scl	scb0_spi_mosi	Port 4 Pin 0: gpio, lcd, csd, scb0
21	P4.1	19	P4.1	16	P4.1	23	P4.1	-	-	scb0_uart_tx	scb0_i2c_sda	scb0_spi_miso	Port 4 Pin 1: gpio, lcd, csd, scb0
22	P4.2	20	P4.2	17	P4.2	24	P4.2	csd_c_mod	-	-	-	scb0_spi_clk	Port 4 Pin 2: gpio, lcd, csd, scb0
23	P4.3	21	P4.3	18	P4.3	25	P4.3	csd_c_sh_tank		-	-	scb0_spi_ssel_0	Port 4 Pin 3: gpio, lcd, csd, scb0
-	-	-	-	-	-	26	NC	-		_	_	-	No Connect
-	-	-	-	-	-	27	NC	-	-	-	-	-	No Connect



The following is the pin-list for the PSoC 4100 (35-WLCSP).

35-6	Ball CSP		Alte	ernate Functions	for Pins		<b>Bin Description</b>	
Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4		
D3	P2.2	sarmux.2	_	-	-	-	Port 2 Pin 2: gpio, lcd, csd, sarmux	
E4	P2.3	sarmux.3	_	-	-	-	Port 2 Pin 3: gpio, lcd, csd, sarmux	
E5	P2.4	sarmux.4	tcpwm0_p[1]	-	-	-	Port 2 Pin 4: gpio, lcd, csd, sarmux, pwm	
E6	P2.5	sarmux.5	tcpwm0_n[1]	-	-	-	Port 2 Pin 5: gpio, lcd, csd, sarmux, pwm	
E3	P2.6	sarmux.6	tcpwm1_p[1]	-	-	-	Port 2 Pin 6: gpio, lcd, csd, sarmux, pwm	
E2	P2.7	sarmux.7	tcpwm1_n[1]	-	-	-	Port 2 Pin 7: gpio, lcd, csd, sarmux, pwm	
E1	P3.0	-	tcpwm0_p[0]	scb1_uart_rx[0]	scb1_i2c_scl[0]	scb1_spi_mosi[0]	Port 3 Pin 0: gpio, lcd, csd, pwm, scb1	
D2	P3.1	-	tcpwm0_n[0]	scb1_uart_tx[0]	scb1_i2c_sda[0]	scb1_spi_miso[0]	Port 3 Pin 1: gpio, lcd, csd, pwm, scb1	
D1	P3.2	-	tcpwm1_p[0]	-	swd_io[0]	scb1_spi_clk[0]	Port 3 Pin 2: gpio, lcd, csd, pwm, scb1, swd	
B7	VSS	-	-	-	-	-	Ground	
C1	P3.3	-	tcpwm1_n[0]	-	swd_clk[0]	scb1_spi_ssel_0[0]	Port 3 Pin 3: gpio, lcd, csd, pwm, scb1, swd	
C2	P3.4	-	tcpwm2_p[0]	-	-	scb1_spi_ssel_1	Port 3 Pin 4: gpio, lcd, csd, pwm, scb1	
B1	P4.0	-	_	scb0_uart_rx	scb0_i2c_scl	scb0_spi_mosi	Port 4 Pin 0: gpio, lcd, csd, scb0	
B2	P4.1	-	-	scb0_uart_tx	scb0_i2c_sda	scb0_spi_miso	Port 4 Pin 1: gpio, lcd, csd, scb0	
A2	P4.2	csd_c_mod	_	-	-	scb0_spi_clk	Port 4 Pin 2: gpio, lcd, csd, scb0	
A1	P4.3	csd_c_sh_tank	_	-	-	scb0_spi_ssel_0	Port 4 Pin 3: gpio, lcd, csd, scb0	
C3	P0.0	comp1_inp	-	-	-	scb0_spi_ssel_1	Port 0 Pin 0: gpio, lcd, csd, scb0, comp	
A5	P0.1	comp1_inn	-	-	-	scb0_spi_ssel_2	Port 0 Pin 1: gpio, lcd, csd, scb0, comp	
A4	P0.2	comp2_inp	-	-	-	scb0_spi_ssel_3	Port 0 Pin 2: gpio, lcd, csd, scb0, comp	
A3	P0.3	comp2_inn	-	-	-	-	Port 0 Pin 3: gpio, lcd, csd, comp	
B3	P0.4	-	_	scb1_uart_rx[1]	scb1_i2c_scl[1]	scb1_spi_mosi[1]	Port 0 Pin 4: gpio, lcd, csd, scb1	
A6	P0.5	-	-	scb1_uart_tx[1]	scb1_i2c_sda[1]	scb1_spi_miso[1]	Port 0 Pin 5: gpio, lcd, csd, scb1	
B4	P0.6	-	ext_clk	-	-	scb1_spi_clk[1]	Port 0 Pin 6: gpio, lcd, csd, scb1, ext_clk	
B5	P0.7	-	_	-	wakeup	scb1_spi_ssel_0[1]	Port 0 Pin 7: gpio, lcd, csd, scb1, wakeup	
B6	XRES	-	-	-	-	-	Chip reset, active low	
A7	VCCD	-	-	-	-	-	Regulated supply, connect to 1µF cap or 1.8V	
C7	VDD	-	_	-	-	-	Supply, 1.8 - 5.5V	
C4	P1.0	ctb.oa0.inp	tcpwm2_p[1]	-	-	-	Port 1 Pin 0: gpio, lcd, csd, ctb, pwm	
C5	P1.1	ctb.oa0.inm	tcpwm2_n[1]	-	-	-	Port 1 Pin 1: gpio, lcd, csd, ctb, pwm	



### Figure 5. 48-Pin TQFP Pinout





## Power

The following power system diagrams show the minimum set of power supply pins as implemented for PSoC 4100. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the  $V_{DDA}$  input. There are separate regulators for the Deep Sleep and Hibernate (lowered power supply and retention) modes. There is a separate low-noise regulator for the bandgap. The supply voltage range is 1.71 V to 5.5 V with all functions and circuits operating over that range.





The PSoC 4100 family allows two distinct modes of power supply operation: Unregulated External Supply, and Regulated External Supply modes.

### Unregulated External Supply

In this mode, PSoC 4100 is powered by an external power supply that can be anywhere in the range of 1.8 V to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of PSoC 4100 supplies the internal logic and the V<sub>CCD</sub> output of the PSoC 4100 must be bypassed to ground via an external Capacitor (in the range of 1  $\mu$ F to 1.6  $\mu$ F; X5R ceramic or better).

 $V_{DDA}$  and  $V_{DDD}$  must be shorted together; the grounds, VSSA and  $V_{SS}$  must also be shorted together. Bypass capacitors must be used from  $V_{DDD}$  to ground, typical practice for systems in this frequency range is to use a capacitor in the 1- $\mu F$  range in parallel with a smaller capacitor (0.1  $\mu F$  for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the Bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

### Figure 11. 48-TQFP Package Example



Figure 12. 44-TQFP Package Example



Power Supply	Bypass Capacitors
VDDD-VSS	0.1 $\mu$ F ceramic at each pin (C2, C6) plus bulk capacitor 1 to 10 $\mu$ F (C1). Total capac- itance may be greater than 10 $\mu$ F.
VDDA-VSSA	0.1 $\mu$ F ceramic at pin (C4). Additional 1 $\mu$ F to 10 $\mu$ F (C3) bulk capacitor. Total capacitance may be greater than 10 $\mu$ F.
VCCD-VSS	1 μF ceramic capacitor at the VCCD pin (C5)
VREF–VSSA (optional)	The internal bandgap may be bypassed with a 1 $\mu$ F to 10 $\mu$ F capacitor. Total capacitance may be greater than 10 $\mu$ F.



# **Development Support**

The PSoC 4100 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

### Documentation

A suite of documentation supports the PSoC 4100 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

**Software User Guide**: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

**Component Datasheets**: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

**Application Notes**: PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

**Technical Reference Manual**: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

#### Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

#### Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4100 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.



## **Electrical Specifications**

### **Absolute Maximum Ratings**

### Table 1. Absolute Maximum Ratings<sup>[1]</sup>

Spec ID#	Parameter	Description	Min	Тур	Мах	Units	Details/ Conditions
SID1	V <sub>DDD_ABS</sub>	Digital supply relative to V <sub>SSD</sub>	-0.5	-	6	V	Absolute max
SID2	V <sub>CCD_ABS</sub>	Direct digital core voltage input relative to Vssd	-0.5	-	1.95	V	Absolute max
SID3	V <sub>GPIO_ABS</sub>	GPIO voltage	-0.5	_	V <sub>DD</sub> +0.5	V	Absolute max
SID4	I <sub>GPIO_ABS</sub>	Maximum current per GPIO	-25	-	25	mA	Absolute max
SID5	I <sub>GPIO_injection</sub>	GPIO injection current, Max for V <sub>IH</sub> > V <sub>DDD</sub> , and Min for V <sub>IL</sub> < V <sub>SS</sub>	-0.5	-	0.5	mA	Absolute max, current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	-	-	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	_	_	V	
BID46	LU	Pin current for latch-up	-200	_	200	mA	

### **Device-Level Specifications**

All specifications are valid for -40 °C  $\leq$  TA  $\leq$  105 °C and TJ  $\leq$  125 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

#### Table 2. DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID53	V <sub>DD</sub>	Power Supply Input Voltage (V <sub>DDA</sub> = V <sub>DDD</sub> = V <sub>DD</sub> )	1.8	-	5.5	V	With regulator enabled
SID255	V <sub>DDD</sub>	Power Supply Input Voltage unregu- lated	1.71	1.8	1.89	V	Internally unregulated Supply
SID54	V <sub>CCD</sub>	Output voltage (for core logic)	-	1.8	-	V	
SID55	CEFC	External Regulator voltage bypass	1	1.3	1.6	μF	X5R ceramic or better
SID56	CEXC	Power supply decoupling capacitor	-	1	-	μF	X5R ceramic or better
Active Mo	de, V <sub>DD</sub> = 1.71	V to 5.5 V. Typical Values measured a	t V <sub>DD</sub> = 3.	.3 V			
SID9	IDD4	Execute from Flash; CPU at 6 MHz	-	-	2.8	mA	
SID10	IDD5	Execute from Flash; CPU at 6 MHz	-	2.2	-	mA	T = 25 °C
SID12	IDD7	Execute from Flash; CPU at 12 MHz,	-	-	4.2	mA	
SID13	IDD8	Execute from Flash; CPU at 12 MHz	-	3.7	-	mA	T = 25 °C
SID16	IDD11	Execute from Flash; CPU at 24 MHz	-	6.7	-	mA	T = 25 °C
SID17	IDD12	Execute from Flash; CPU at 24 MHz	-	-	7.2	mA	
Sleep Mod	le, V <sub>DD</sub> = 1.7 V	to 5.5 V					
SID25	IDD20	I <sup>2</sup> C wakeup, WDT, and Comparators on. 6 MHz.	-	1.3	1.8	mA	V <sub>DD</sub> = 1.71 to 5.5 V
SID25A	IDD20A	I <sup>2</sup> C wakeup, WDT, and Comparators on. 12 MHz.	-	1.7	2.2	mA	V <sub>DD</sub> = 1.71 to 5.5 V
Deep Slee	p M <mark>ode, V<sub>DD</sub> =</mark>	1.8 V to 3.6 V (Regulator on)					
SID31	IDD26	I <sup>2</sup> C wakeup and WDT on.	_	1.3	-	μA	T = 25 °C
SID32	IDD27	I <sup>2</sup> C wakeup and WDT on.	-	_	45	μA	T = 85 °C

#### Note

 Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.



### GPIO

### Table 4. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID57	V <sub>IH</sub> [2]	Input voltage high threshold	0.7 × V <sub>DDD</sub>	-	-	V	CMOS Input
SID58	V <sub>IL</sub>	Input voltage low threshold	_	-	0.3 × V <sub>DDD</sub>	V	CMOS Input
SID241	V <sub>IH</sub> [2]	LVTTL input, V <sub>DDD</sub> < 2.7 V	0.7× V <sub>DDD</sub>	-	-	V	
SID242	V <sub>IL</sub>	LVTTL input, V <sub>DDD</sub> < 2.7 V	-	-	0.3 × V <sub>DDD</sub>	V	
SID243	V <sub>IH</sub> <sup>[2]</sup>	LVTTL input, $V_{DDD} \ge 2.7 V$	2.0	-	-	V	
SID244	V <sub>IL</sub>	LVTTL input, $V_{DDD} \ge 2.7 V$	-	-	0.8	V	
SID59	V <sub>OH</sub>	Output voltage high level	V <sub>DDD</sub> -0.6	-	-	V	I <sub>OH</sub> = 4 mA at 3-V V <sub>DDD</sub>
SID60	V <sub>OH</sub>	Output voltage high level	V <sub>DDD</sub> -0.5	-	-	V	I <sub>OH</sub> = 1 mA at 1.8-V V <sub>DDD</sub>
SID61	V <sub>OL</sub>	Output voltage low level	-	-	0.6	V	I <sub>OL</sub> = 4 mA at 1.8-V V <sub>DDD</sub>
SID62	V <sub>OL</sub>	Output voltage low level	-	-	0.6	V	I <sub>OL</sub> = 8 mA at 3-V V <sub>DDD</sub>
SID62A	V <sub>OL</sub>	Output voltage low level	-	-	0.4	V	I <sub>OL</sub> = 3 mA at 3-V V <sub>DDD</sub>
SID63	R <sub>PULLUP</sub>	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	R <sub>PULLDOWN</sub>	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID65	IIL	Input leakage current (absolute value)	-	-	2	nA	25 °C, V <sub>DDD</sub> = 3.0-V
SID65A	I <sub>IL_CTBM</sub>	Input leakage current (absolute value) for CTBM pins	_	-	4	nA	
SID66	C <sub>IN</sub>	Input capacitance	-	_	7	pF	
SID67	V <sub>HYSTTL</sub>	Input hysteresis LVTTL	25	40	-	mV	$V_{DDD} \ge 2.7 V.$ Guaranteed by characterization
SID68	V <sub>HYSCMOS</sub>	Input hysteresis CMOS	0.05 × V <sub>DDD</sub>	_	_	mV	Guaranteed by characterization
SID69	IDIODE	Current through protection diode to $V_{DD}/Vss$	_	_	100	μA	Guaranteed by characterization
SID69A	ITOT_GPIO	Maximum Total Source or Sink Chip Current	-	_	200	mA	Guaranteed by characterization



Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID70	T <sub>RISEF</sub>	Rise time in fast strong mode	2	-	12	ns	3.3-V V <sub>DDD</sub> , Cload = 25 pF
SID71	T <sub>FALLF</sub>	Fall time in fast strong mode	2	-	12	ns	3.3-V V <sub>DDD</sub> , Cload = 25 pF
SID72	T <sub>RISES</sub>	Rise time in slow strong mode	10	-	60	ns	3.3-V V <sub>DDD</sub> , Cload = 25 pF
SID73	T <sub>FALLS</sub>	Fall time in slow strong mode	10	-	60	ns	3.3-V V <sub>DDD</sub> , Cload = 25 pF
SID74	F <sub>GPIOUT1</sub>	GPIO Fout;3.3 V $\leq$ V <sub>DDD</sub> $\leq$ 5.5 V. Fast strong mode.	_	-	24	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID75	F <sub>GPIOUT2</sub>	GPIO Fout;1.7 V $\leq$ V <sub>DDD</sub> $\leq$ 3.3 V. Fast strong mode.	_	-	16.7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID76	F <sub>GPIOUT3</sub>	GPIO Fout;3.3 V $\leq$ V <sub>DDD</sub> $\leq$ 5.5 V. Slow strong mode.	-	-	7	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID245	F <sub>GPIOUT4</sub>	GPIO Fout;1.7 V $\leq$ V <sub>DDD</sub> $\leq$ 3.3 V. Slow strong mode.	_	-	3.5	MHz	90/10%, 25-pF load, 60/40 duty cycle
SID246	F <sub>GPIOIN</sub>	GPIO input operating frequency; 1.71 V $\leq$ V <sub>DDD</sub> $\leq$ 5.5 V	-	-	24	MHz	90/10% V <sub>IO</sub>

### Table 5. GPIO AC Specifications (Guaranteed by Characterization)

XRES

### Table 6. XRES DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Мах	Units	Details/ Conditions
SID77	V <sub>IH</sub>	Input voltage high threshold	0.7 × V <sub>DDD</sub>	-	_	V	CMOS Input
SID78	V <sub>IL</sub>	Input voltage low threshold	-	-	0.3 × V <sub>DDD</sub>	V	CMOS Input
SID79	R <sub>PULLUP</sub>	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID80	C <sub>IN</sub>	Input capacitance	-	3	-	pF	
SID81	V <sub>HYSXRES</sub>	Input voltage hysteresis	_	100	_	mV	Guaranteed by characterization
SID82	IDIODE	Current through protection diode to $V_{\text{DDD}}/V_{\text{SS}}$	_	-	100	μA	Guaranteed by characterization

### Table 7. XRES AC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID83	T <sub>RESETWIDTH</sub>	Reset pulse width	1	-	-	μs	Guaranteed by characterization



### Table 10. Comparator AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID91	T <sub>RESP1</sub>	Response time, normal mode	-	-	110	ns	50-mV overdrive
SID258	T <sub>RESP2</sub>	Response time, low power mode	-	-	200	ns	50-mV overdrive
SID92	T <sub>RESP3</sub>	Response time, ultra low power mode ( $V_{DDD} \ge 2.2 \text{ V}$ for Temp < 0 °C, $V_{DDD} \ge$ 1.8 V for Temp > 0 °C)	-	_	15	μs	200-mV overdrive

#### Temperature Sensor

### Table 11. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID93	T <sub>SENSACC</sub>	Temperature sensor accuracy	-5	±1	+5	°C	–40 to +85 °C

#### SAR ADC

#### Table 12. SAR ADC DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID94	A_RES	Resolution	_	-	12	bits	
SID95	A_CHNIS_S	Number of channels - single ended	-	-	8		8 full speed
SID96	A-CHNKS_D	Number of channels - differential	_	-	4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	_	-	-		Yes. Based on characterization
SID98	A_GAINERR	Gain error	_	_	±0.1	%	With external reference. Guaranteed by characterization
SID99	A_OFFSET	Input offset voltage	_	-	2	mV	Measured with 1-V V <sub>REF.</sub> Guaranteed by characterization
SID100	A_ISAR	Current consumption	-	-	1	mA	
SID101	A_VINS	Input voltage range - single ended	$V_{SS}$	-	V <sub>DDA</sub>	V	Based on device characterization
SID102	A_VIND	Input voltage range - differential	$V_{SS}$	-	V <sub>DDA</sub>	V	Based on device characterization
SID103	A_INRES	Input resistance	_	-	2.2	KΩ	Based on device characterization
SID104	A_INCAP	Input capacitance	_	-	10	pF	Based on device characterization
SID106	A_PSRR	Power supply rejection ratio	70	-	-	dB	
SID107	A_CMRR	Common mode rejection ratio	66	-	Ι	dB	Measured at 1 V
SID111	A_INL	Integral non linearity	-1.7	_	+2	LSB	V <sub>DD</sub> = 1.71 to 5.5, 806 ksps, V <sub>REF</sub> = 1 to 5.5.
SID111A	A_INL	Integral non linearity	-1.5	_	+1.7	LSB	V <sub>DDD</sub> = 1.71 to 3.6, 806 ksps, V <sub>REF</sub> = 1.71 to V <sub>DDD</sub> .



### **Digital Peripherals**

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode.

Timer/Counter/PWM

### Table 15. TCPWM Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	-	-	45	μA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	-	-	155	μA	All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	-	-	650	μA	All modes (TCPWM)
SID.TCPWM.3	TCPWMFREQ	Operating frequency	-	-	Fc	MHz	Fc max = Fcpu. Maximum = 24 MHz
SID.TCPWM.4	TPWMENEXT	Input Trigger Pulse Width for all Trigger Events	2/Fc	-	-	ns	Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID.TCPWM.5	TPWMEXT	Output Trigger Pulse widths	2/Fc	-	_	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	TCRES	Resolution of Counter	1/Fc	-	-	ns	Minimum time between successive counts
SID.TCPWM.5B	PWMRES	PWM Resolution	1/Fc	_	_	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	QRES	Quadrature inputs resolution	1/Fc	_	_	ns	Minimum pulse width between Quadrature phase inputs.

βC

## Table 16. Fixed I<sup>2</sup>C DC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Parameter Description		Тур	Max	Units	<b>Details/Conditions</b>
SID149	I <sub>I2C1</sub>	Block current consumption at 100 kHz	-	-	50	μA	
SID150	I <sub>I2C2</sub>	Block current consumption at 400 kHz	-	-	135	μA	
SID151	I <sub>I2C3</sub>	Block current consumption at 1 Mbps	-	-	310	μA	
SID152	I <sub>I2C4</sub>	I <sup>2</sup> C enabled in Deep Sleep mode	_	-	1.4	μA	

## Table 17. Fixed I<sup>2</sup>C AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Мах	Units	Details/Conditions
SID153	F <sub>I2C1</sub>	Bit rate	-	-	1	Mbps	

#### LCD Direct Drive

### Table 18. LCD Direct Drive DC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	<b>Details/Conditions</b>
SID154	ILCDLOW	Operating current in low power mode	-	5	-	μA	16 × 4 small segment disp. at 50 Hz
SID155	C <sub>LCDCAP</sub>	LCD capacitance per segment/common driver	-	500	5000	pF	Guaranteed by Design
SID156	LCD <sub>OFFSET</sub>	Long-term segment offset	-	20	-	mV	
SID157	I <sub>LCDOP1</sub>	PWM Mode current. 5-V bias. 24-MHz IMO. 25 °C	_	0.6	-	mA	32 × 4 segments. 50 Hz
SID158	I <sub>LCDOP2</sub>	PWM Mode current. 3.3-V bias. 24-MHz IMO. 25 °C	_	0.5	_	mA	32 × 4 segments. 50 Hz



### Internal Main Oscillator

### Table 33. IMO DC Specifications (Guaranteed by Design)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID218	I <sub>IMO1</sub>	IMO operating current at 48 MHz	-	-	1000	μA	
SID219	I <sub>IMO2</sub>	IMO operating current at 24 MHz	-	-	325	μA	
SID220	I <sub>IMO3</sub>	IMO operating current at 12 MHz	-	-	225	μA	
SID221	I <sub>IMO4</sub>	IMO operating current at 6 MHz	-	-	180	μA	
SID222	I <sub>IMO5</sub>	IMO operating current at 3 MHz	-	-	150	μA	

### Table 34. IMO AC Specifications

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID223	F <sub>IMOTOL1</sub>	Frequency variation from 3 to 48 MHz	_	-	±2	%	±3% if T <sub>A</sub> > 85 °C and IMO frequency < 24 MHz
SID226	T <sub>STARTIMO</sub>	IMO startup time	-	-	12	μs	
SID227	T <sub>JITRMSIMO1</sub>	RMS Jitter at 3 MHz	-	156	-	ps	
SID228	T <sub>JITRMSIMO2</sub>	RMS Jitter at 24 MHz	-	145	-	ps	
SID229	T <sub>JITRMSIMO3</sub>	RMS Jitter at 48 MHz	-	139	-	ps	

#### Internal Low-Speed Oscillator

### Table 35. ILO DC Specifications (Guaranteed by Design)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID231	I <sub>ILO1</sub>	ILO operating current at 32 kHz	_	0.3	1.05	μA	Guaranteed by Characterization
SID233	IILOLEAK	ILO leakage current	_	2	15	nA	Guaranteed by Design

#### Table 36. ILO AC Specifications

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID234	T <sub>STARTILO1</sub>	ILO startup time	-	-	2	ms	Guaranteed by charac- terization
SID236	T <sub>ILODUTY</sub>	ILO duty cycle	40	50	60	%	Guaranteed by charac- terization
SID237	F <sub>ILOTRIM1</sub>	32 kHz trimmed frequency	15	32	50	kHz	Max ILO frequency is 70 kHz if T <sub>A</sub> > 85 °C

### Table 37. External Clock Specifications

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID305	ExtClkFreq	External Clock input Frequency	0	-	24	MHz	Guaranteed by characterization
SID306	ExtClkDuty	Duty cycle; Measured at V <sub>DD/2</sub>	45	-	55	%	Guaranteed by characterization



### Part Numbering Conventions

PSoC 4 devices follow the part numbering convention described in the following table. All fields are single-character alphanumeric (0, 1, 2, ..., 9, A,B, ..., Z) unless stated otherwise.

The part numbers are of the form CY8C4ABCDEF-XYZ where the fields are defined as follows.

Example	$\underline{CY8C} 4 \underline{A} \underline{B} \underline{C} \underline{D} \underline{E} \underline{F} - \underline{X} \underline{Y} \underline{Z}$
	Cypress Prefix
4: PSoC 4	Architecture
1: 4100Family	Family within Architecture
2: 24 MHz	Speed Grade
5: 32KB	Flash Capacity
AX: TQFP	Package Code
I: Industrial	Temperature Range
	Attributes Set

The Field Values are listed in the following table.

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
۸	Family within architecture	1	4100 Family
		2	4200 Family
в		2	24 MHz
В	Ci O Speed	4	48 MHz
C	Flash Capacity	4	16 KB
C	Thash Capacity	5	32 KB
		AX, AZ	TQFP
DE	Package Code	LQ	QFN
	1 ackage code	PV	SSOP
		FN	WLCSP
F	Temperature Pange	I	Industrial
		Q	Extended Industrial
XYZ	Attributes Code	000-999	Code of feature set in specific family







NOTES:

1. XXX HATCH AREA IS SOLDERABLE EXPOSED PAD

2. REFERENCE JEDEC # MO-248

3. PACKAGE WEIGHT: 68 ±2 mg

4. ALL DIMENSIONS ARE IN MILLIMETERS

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.

Figure 18. 44-pin TQFP Package Outline



001-80659 \*A







# Acronyms

### Table 43. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus archi- tecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMIPS	Dhrystone million instructions per second
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge

### Table 43. Acronyms Used in this Document (continued)

Acronym	Description
ETM	embedded trace macrocell
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I <sup>2</sup> C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD



Acronym	Description
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration data sheet
POR	power-on reset
PRES	precise power-on reset
PRS	pseudo random sequence
PS	port read data register
PSoC <sup>®</sup>	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I <sup>2</sup> C serial clock
SDA	I <sup>2</sup> C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol

### Table 43. Acronyms Used in this Document (continued)

#### Acronym Description SWV single-wire viewer TD transaction descriptor, see also DMA THD total harmonic distortion TIA transimpedance amplifier TRM technical reference manual TTL transistor-transistor logic ΤХ transmit UART Universal Asynchronous Transmitter Receiver, a communications protocol UDB universal digital block USB Universal Serial Bus USBIO USB input/output, PSoC pins used to connect to a USB port VDAC voltage DAC, see also DAC, IDAC WDT watchdog timer WOL write once latch, see also NVL WRES watchdog timer reset **XRES** external reset I/O pin XTAL crystal

Table 43. Acronyms Used in this Document (continued)