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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I <sup>2</sup> C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	24
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 8x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4124pvi-432

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



## **More Information**

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA86521, How to Design with PSoC 3, PSoC 4, and PSoC 5LP. Following is an abbreviated list for PSoC 4:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: PSoC 1, PSoC 3, PSoC 4, PSoC 5LP In addition, PSoC Creator includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 4 are:
  - □ AN79953: Getting Started With PSoC 4
  - □ AN88619: PSoC 4 Hardware Design Considerations
  - □ AN86439: Using PSoC 4 GPIO Pins
  - □ AN57821: Mixed Signal Circuit Board Layout
  - AN81623: Digital Design Best Practices
  - □ AN73854: Introduction To Bootloaders
  - AN89610: ARM Cortex Code Optimization
  - □ AN90071: CY8CMBRxxx CapSense Design Guide

- Technical Reference Manual (TRM) is in two documents:
- Architecture TRM details each PSoC 4 functional block.
- Registers TRM describes each of the PSoC 4 registers.
- Development Kits:
  - CY8CKIT-042, PSoC 4 Pioneer Kit, is an easy-to-use and inexpensive development platform. This kit includes connectors for Arduino<sup>™</sup> compatible shields and Digilent® Pmod<sup>™</sup> daughter cards.
  - CY8CKIT-049 is a very low-cost prototyping platform. It is a low-cost alternative to sampling PSoC 4 devices.
  - CY8CKIT-001 is a common development platform for any one of the PSoC 1, PSoC 3, PSoC 4, or PSoC 5LP families of devices.

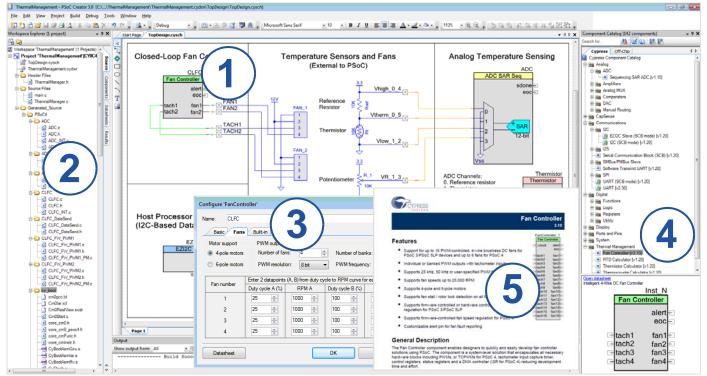
The MiniProg3 device provides an interface for flash programming and debug.

## **PSoC Creator**

PSoC Creator is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of PSoC 3, PSoC 4, and PSoC 5LP based systems. Create designs using classic, familiar schematic capture supported by over 100 pre-verified, production-ready PSoC Components; see the list of component datasheets. With PSoC Creator, you can:

- 1. Drag and drop component icons to build your hardware system design in the main design workspace
- 2. Codesign your application firmware with the PSoC hardware, using the PSoC Creator IDE C compiler
- 3. Configure components using the configuration tools
- 4. Explore the library of 100+ components
- 5. Review component datasheets

#### Figure 1. Multiple-Sensor Example Project in PSoC Creator





#### IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile latches (NVL). Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 24 MHz and it can be adjusted between 3 MHz to 24 MHz in steps of 1 MHz. The IMO tolerance with Cypress-provided calibration settings is ±2%.

#### ILO Clock Source

The ILO is a very low power oscillator, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

#### Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

#### Reset

PSoC 4100 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration. The XRES pin has an internal pull-up resistor that is always enabled.

#### Voltage Reference

The PSoC 4100 reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal to noise ratios (SNR) and better absolute accuracy, it is possible to bypass the internal reference using a GPIO pin or to use an external reference for the SAR.

## Analog Blocks

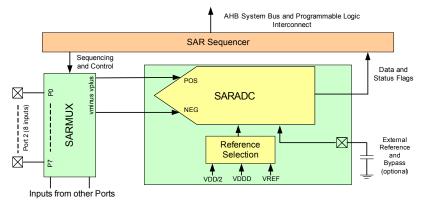
#### 12-bit SAR ADC

The 12-bit 806 ksps SAR ADC can operate at a maximum clock rate of 14.5 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to  $\pm$ 1%) and by providing the choice (for the PSoC 4100 case) of three internal voltage references: V<sub>DD</sub>, V<sub>DD</sub>/2, and V<sub>REF</sub> (nominally 1.024 V) as well as an external reference through a GPIO pin. The sample-and-hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision providing appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, aggregate sampling bandwidth is equal to 806 ksps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.



#### Figure 4. SAR ADC System Diagram



## GPIO

PSoC 4100 has 36 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
  - Analog input mode (input and output buffers disabled)
     Input only
  - Weak pull-up with strong pull-down
  - □ Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - □ Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes).
- Selectable slew rates for dV/dt related noise control to improve EMI.

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves. Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4100 since it has 4.5 ports).

### **Special Function Peripherals**

#### LCD Segment Drive

PSoC 4100 has an LCD controller which can drive up to four commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

#### CapSense

CapSense is supported on all pins in the PSoC 4100 through a CapSense Sigma-Delta (CSD) block that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CapSense function can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another mux bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

The CapSense block has two IDACs which can be used for general purposes if CapSense is not being used.(both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

### WLCSP Package Bootloader

The WLCSP package is supplied with an I<sup>2</sup>C Bootloader installed in flash. The bootloader is compatible with PSoC Creator bootloadable project files and has the following default settings:

- I<sup>2</sup>C SCL and SDA connected to port pins P4.0 and P4.1 respectively (external pull-up resistors required)
- I<sup>2</sup>C Slave mode, address 8, data rate = 100 kbps
- Single application
- Wait two seconds for bootload command
- Other bootloader options are as set by the PSoC Creator Bootloader Component default
- Occupies the bottom 4.5 K of flash

For more information on this bootloader, see the following Cypress application notes:

#### AN73854 - Introduction to Bootloaders

Note that a PSoC Creator bootloadable project must be associated with *.hex* and *.elf* files for a bootloader project that is configured for the target device. Bootloader *.hex* and *.elf* files can be found at http://www.cypress.com/?rID=78805. The factory-installed bootloader can be overwritten using JTAG or SWD programming.

# PSoC<sup>®</sup> 4: PSoC 4100 Family Datasheet



4	4-TQFP	4	0-QFN	N 28-SSOP 48-TQFP Alternate Functions for Pins			Din Description						
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	Pin Description
24	P0.0	22	P0.0	19	P0.0	28	P0.0	comp1_inp	-	-	-	scb0_spi_ssel_1	Port 0 Pin 0: gpio, lcd, csd, scb0, comp
25	P0.1	23	P0.1	20	P0.1	29	P0.1	comp1_inn	-	-	-	scb0_spi_ssel_2	Port 0 Pin 1: gpio, lcd, csd, scb0, comp
26	P0.2	24	P0.2	21	P0.2	30	P0.2	comp2_inp	-	-	-	scb0_spi_ssel_3	Port 0 Pin 2: gpio, lcd, csd, scb0, comp
27	P0.3	25	P0.3	22	P0.3	31	P0.3	comp2_inn	-	-	-	-	Port 0 Pin 3: gpio, lcd, csd, comp
28	P0.4	26	P0.4	-	-	32	P0.4	-	-	scb1_uart_rx[1]	scb1_i2c_scl[1]	scb1_spi_mosi[1]	Port 0 Pin 4: gpio, lcd, csd, scb1
29	P0.5	27	P0.5	Ι	-	33	P0.5	-	-	scb1_uart_tx[1]	scb1_i2c_sda[1]	scb1_spi_miso[1]	Port 0 Pin 5: gpio, lcd, csd, scb1
30	P0.6	28	P0.6	23	P0.6	34	P0.6	-	ext_clk	-	-	scb1_spi_clk[1]	Port 0 Pin 6: gpio, lcd, csd, scb1, ext_clk
31	P0.7	29	P0.7	24	P0.7	35	P0.7	-	-	-	wakeup	scb1_spi_ssel_0[1]	Port 0 Pin 7: gpio, lcd, csd, scb1, wakeup
32	XRES	30	XRES	25	XRES	36	XRES	-	-	-	-	-	Chip reset, active low
33	VCCD	31	VCCD	26	VCCD	37	VCCD	-	-	-	-	-	Regulated supply, connect to 1µF cap or 1.8V
-	-	-	-	-	-	38	VSSD	-	-	-	-	-	Digital Ground
34	VDDD	32	VDDD	27	VDD	39	VDDD	-	-	-	-	-	Digital Supply, 1.8 - 5.5V
35	VDDA	33	VDDA	27	VDD	40	VDDA	-	-	-	-	-	Analog Supply, 1.8 - 5.5V, equal to VDDD
36	VSSA	34	VSSA	28	VSS	41	VSSA	-	-	-	-	-	Analog Ground
37	P1.0	35	P1.0	1	P1.0	42	P1.0	ctb.oa0.inp	tcpwm2_p[1]	-	-	-	Port 1 Pin 0: gpio, lcd, csd, ctb, pwm
38	P1.1	36	P1.1	2	P1.1	43	P1.1	ctb.oa0.inm	tcpwm2_n[1]	-	-	-	Port 1 Pin 1: gpio, lcd, csd, ctb, pwm
39	P1.2	37	P1.2	3	P1.2	44	P1.2	ctb.oa0.out	tcpwm3_p[1]	-	-	-	Port 1 Pin 2: gpio, lcd, csd, ctb, pwm
40	P1.3	38	P1.3	-	-	45	P1.3	ctb.oa1.out	tcpwm3_n[1]	-	-	-	Port 1 Pin 3: gpio, lcd, csd, ctb, pwm
41	P1.4	39	P1.4	Ι	-	46	P1.4	ctb.oa1.inm	-	-	-	-	Port 1 Pin 4: gpio, lcd, csd, ctb
42	P1.5	-	-	-	-	47	P1.5	ctb.oa1.inp	-	-	-	-	Port 1 Pin 5: gpio, lcd, csd, ctb
43	P1.6	Ι	-	-	-	48	P1.6	ctb.oa0.inp_alt	-	-	-	-	Port 1 Pin 6: gpio, lcd, csd
44	P1.7/VREF	40	P1.7/VREF	4	P1.7/VREF	1	P1.7/VREF	ctb.oa1.inp_alt ext_vref	_	-	-	_	Port 1 Pin 7: gpio, lcd, csd, ext_ref

#### Notes:

1. tcpwm\_p and tcpwm\_n refer to tcpwm non-inverted and inverted outputs respectively.

2. P3.2 and P3.3 are SWD pins after boot (reset).



35-	Ball CSP		Alte	rnate Functions	for Pins		Pin Description				
Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4					
C6	P1.2	ctb.oa0.out	tcpwm3_p[1]	_	_	-	Port 1 Pin 2: gpio, lcd, csd, ctb, pwm				
D7	P1.3	ctb.oa1.out	tcpwm3_n[1]	_	-	-	Port 1 Pin 3: gpio, lcd, csd, ctb, pwm				
D4	P1.4	ctb.oa1.inm	_	_	-	-	Port 1 Pin 4: gpio, lcd, csd, ctb				
D5	P1.5	ctb.oa1.inp	_	_	-	-	Port 1 Pin 5: gpio, lcd, csd, ctb				
D6	P1.6	ctb.oa0.inp_alt	_	_	-	-	Port 1 Pin 6: gpio, lcd, csd				
E7	P1.7/VREF	ctb.oa1.inp_alt ext_vref	_	_	_	-	Port 1 Pin 7: gpio, lcd, csd, ext_ref				

#### Descriptions of the Pin functions are as follows:

**VDDD**: Power supply for both analog and digital sections (where there is no V<sub>DDA</sub> pin).

**VDDA**: Analog  $V_{DD}$  pin where package pins allow; shorted to  $V_{DDD}$  otherwise.

VSSA: Analog ground pin where package pins allow; shorted to VSS otherwise

VSS: Ground pin.

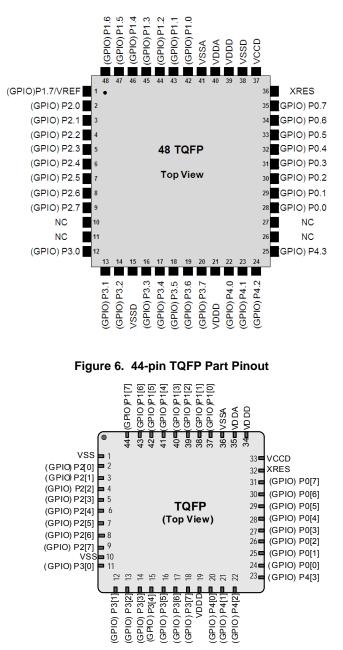
VCCD: Regulated Digital supply (1.8 V ±5%).

Port Pins can all be used as LCD Commons, LCD Segment drivers, or CSD sense and shield pins can be connected to AMUXBUS A or B or can all be used as GPIO pins that can be driven by firmware or DSI signals.

The following packages are supported: 48-pin TQFP, 44-pin TQFP, 40-pin QFN, and 28-pin SSOP.



#### Figure 5. 48-Pin TQFP Pinout





## **Development Support**

The PSoC 4100 family has a rich set of documentation, development tools, and online resources to assist you during your development process. Visit www.cypress.com/go/psoc4 to find out more.

#### Documentation

A suite of documentation supports the PSoC 4100 family to ensure that you can find answers to your questions quickly. This section contains a list of some of the key documents.

**Software User Guide**: A step-by-step guide for using PSoC Creator. The software user guide shows you how the PSoC Creator build process works in detail, how to use source control with PSoC Creator, and much more.

**Component Datasheets**: The flexibility of PSoC allows the creation of new peripherals (components) long after the device has gone into production. Component data sheets provide all of the information needed to select and use a particular component, including a functional description, API documentation, example code, and AC/DC specifications.

**Application Notes:** PSoC application notes discuss a particular application of PSoC in depth; examples include brushless DC motor control and on-chip filtering. Application notes often include example projects in addition to the application note document.

**Technical Reference Manual**: The Technical Reference Manual (TRM) contains all the technical detail you need to use a PSoC device, including a complete description of all PSoC registers. The TRM is available in the Documentation section at www.cypress.com/psoc4.

#### Online

In addition to print documentation, the Cypress PSoC forums connect you with fellow PSoC users and experts in PSoC from around the world, 24 hours a day, 7 days a week.

#### Tools

With industry standard cores, programming, and debugging interfaces, the PSoC 4100 family is part of a development tool ecosystem. Visit us at www.cypress.com/go/psoccreator for the latest information on the revolutionary, easy to use PSoC Creator IDE, supported third party compilers, programmers, debuggers, and development kits.



## **Electrical Specifications**

## **Absolute Maximum Ratings**

## Table 1. Absolute Maximum Ratings<sup>[1]</sup>

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID1	V <sub>DDD_ABS</sub>	Digital supply relative to V <sub>SSD</sub>	-0.5	_	6	V	Absolute max
SID2	V <sub>CCD_ABS</sub>	Direct digital core voltage input relative to Vssd	-0.5	-	1.95	V	Absolute max
SID3	V <sub>GPIO_ABS</sub>	GPIO voltage	-0.5	-	V <sub>DD</sub> +0.5	V	Absolute max
SID4	I <sub>GPIO_ABS</sub>	Maximum current per GPIO	-25	-	25	mA	Absolute max
SID5	I <sub>GPIO_injection</sub>	GPIO injection current, Max for V <sub>IH</sub> > V <sub>DDD</sub> , and Min for V <sub>IL</sub> < V <sub>SS</sub>	-0.5	_	0.5	mA	Absolute max, current injected per pin
BID44	ESD_HBM	Electrostatic discharge human body model	2200	_	_	V	
BID45	ESD_CDM	Electrostatic discharge charged device model	500	-	-	V	
BID46	LU	Pin current for latch-up	-200	_	200	mA	

## **Device-Level Specifications**

All specifications are valid for -40 °C  $\leq$  TA  $\leq$  105 °C and TJ  $\leq$  125 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

#### Table 2. DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID53	V <sub>DD</sub>	Power Supply Input Voltage (V <sub>DDA</sub> = V <sub>DDD</sub> = V <sub>DD</sub> )	1.8	-	5.5	V	With regulator enabled
SID255	V <sub>DDD</sub>	Power Supply Input Voltage unregu- lated	1.71	1.8	1.89	V	Internally unregulated Supply
SID54	V <sub>CCD</sub>	Output voltage (for core logic)	-	1.8	-	V	
SID55	CEFC	External Regulator voltage bypass	1	1.3	1.6	μF	X5R ceramic or better
SID56	CEXC	Power supply decoupling capacitor	-	1	-	μF	X5R ceramic or better
Active Mo	de, V <sub>DD</sub> = 1.71	V to 5.5 V. Typical Values measured a	t V <sub>DD</sub> = 3.	.3 V		•	
SID9	IDD4	Execute from Flash; CPU at 6 MHz	-	_	2.8	mA	
SID10	IDD5	Execute from Flash; CPU at 6 MHz	-	2.2	-	mA	T = 25 °C
SID12	IDD7	Execute from Flash; CPU at 12 MHz,	_	_	4.2	mA	
SID13	IDD8	Execute from Flash; CPU at 12 MHz	-	3.7	-	mA	T = 25 °C
SID16	IDD11	Execute from Flash; CPU at 24 MHz	-	6.7	-	mA	T = 25 °C
SID17	IDD12	Execute from Flash; CPU at 24 MHz	_	_	7.2	mA	
Sleep Mod	le, V <sub>DD</sub> = 1.7 V	to 5.5 V					
SID25	IDD20	I <sup>2</sup> C wakeup, WDT, and Comparators on. 6 MHz.	-	1.3	1.8	mA	V <sub>DD</sub> = 1.71 to 5.5 V
SID25A	IDD20A	I <sup>2</sup> C wakeup, WDT, and Comparators on. 12 MHz.	-	1.7	2.2	mA	V <sub>DD</sub> = 1.71 to 5.5 V
Deep Slee	p Mode, V <sub>DD</sub> =	1.8 V to 3.6 V (Regulator on)					
SID31	IDD26	I <sup>2</sup> C wakeup and WDT on.	-	1.3	-	μA	T = 25 °C
SID32	IDD27	I <sup>2</sup> C wakeup and WDT on.	-	-	45	μA	T = 85 °C

#### Note

 Usage above the absolute maximum conditions listed in Table 1 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.



#### GPIO

## Table 4. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID57	V <sub>IH</sub> <sup>[2]</sup>	Input voltage high threshold	0.7 × V <sub>DDD</sub>	_	-	V	CMOS Input
SID58	V <sub>IL</sub>	Input voltage low threshold	-	-	0.3 × V <sub>DDD</sub>	V	CMOS Input
SID241	V <sub>IH</sub> <sup>[2]</sup>	LVTTL input, V <sub>DDD</sub> < 2.7 V	0.7× V <sub>DDD</sub>	-	-	V	
SID242	V <sub>IL</sub>	LVTTL input, V <sub>DDD</sub> < 2.7 V	-	-	0.3 × V <sub>DDD</sub>	V	
SID243	V <sub>IH</sub> <sup>[2]</sup>	LVTTL input, $V_{DDD} \ge 2.7 V$	2.0	-	-	V	
SID244	V <sub>IL</sub>	LVTTL input, $V_{DDD} \ge 2.7 V$	-	-	0.8	V	
SID59	V <sub>OH</sub>	Output voltage high level	V <sub>DDD</sub> -0.6	_	-	V	I <sub>OH</sub> = 4 mA at 3-V V <sub>DDD</sub>
SID60	V <sub>OH</sub>	Output voltage high level	V <sub>DDD</sub> -0.5	-	-	V	I <sub>OH</sub> = 1 mA at 1.8-V V <sub>DDD</sub>
SID61	V <sub>OL</sub>	Output voltage low level	-	-	0.6	V	I <sub>OL</sub> = 4 mA at 1.8-V V <sub>DDD</sub>
SID62	V <sub>OL</sub>	Output voltage low level	-	-	0.6	V	I <sub>OL</sub> =8 mA at 3-V V <sub>DDD</sub>
SID62A	V <sub>OL</sub>	Output voltage low level	-	-	0.4	V	I <sub>OL</sub> = 3 mA at 3-V V <sub>DDD</sub>
SID63	R <sub>PULLUP</sub>	Pull-up resistor	3.5	5.6	8.5	kΩ	
SID64	R <sub>PULLDOWN</sub>	Pull-down resistor	3.5	5.6	8.5	kΩ	
SID65	IIL	Input leakage current (absolute value)	-	-	2	nA	25 °C, V <sub>DDD</sub> = 3.0-V
SID65A	I <sub>IL_CTBM</sub>	Input leakage current (absolute value) for CTBM pins	-	-	4	nA	
SID66	C <sub>IN</sub>	Input capacitance	-	-	7	pF	
SID67	V <sub>HYSTTL</sub>	Input hysteresis LVTTL	25	40	_	mV	$V_{DDD} \ge 2.7 \text{ V.}$ Guaranteed by characterization
SID68	V <sub>HYSCMOS</sub>	Input hysteresis CMOS	0.05 × V <sub>DDD</sub>	_	-	mV	Guaranteed by characterization
SID69	I <sub>DIODE</sub>	Current through protection diode to V <sub>DD</sub> /Vss	-	-	100	μA	Guaranteed by characterization
SID69A	I <sub>TOT_GPIO</sub>	Maximum Total Source or Sink Chip Current	-	-	200	mA	Guaranteed by characterization



Spec ID#	Parameter	Description	Min	Тур	Max	Units	Details/ Conditions
SID297	Cload	Stable up to maximum load. Perfor- mance specs at 50 pF.	-	-	125	pF	
SID298	Slew_rate	Cload = 50 pF, Power = High, $V_{DDA} \ge 2.7 V$	6	-	-	V/µs	
SID299	T_op_wake	From disable to enable, no external RC dominating	-	300	-	μs	
SID299A	OL_GAIN	Open Loop Gain	-	90	-	dB	Guaranteed by design
	Comp_mode	Comparator mode; 50-mV drive, Trise = Tfall (approx)	-	-	-		
SID300	T <sub>PD1</sub>	Response time; power = high	_	150	_	ns	
SID301	T <sub>PD2</sub>	Response time; power = medium	_	400	-	ns	
SID302	T <sub>PD3</sub>	Response time; power = low	_	2000	_	ns	
SID303	Vhyst_op	Hysteresis	_	10	_	mV	

## Table 8. Opamp Specifications (Guaranteed by Characterization) (continued)

## Comparator

## Table 9. Comparator DC Specifications

Spec ID#	Parameter	Description	Min	Тур	Мах	Units	Details/ Conditions
SID85	V <sub>OFFSET2</sub>	Input offset voltage, Common Mode voltage range from 0 to V <sub>DD</sub> -1	_	-	±4	mV	
SID85A	V <sub>OFFSET3</sub>	Input offset voltage. Ultra low-power mode ( $V_{DDD} \ge 2.2 \text{ V}$ for Temp < 0 °C, $V_{DDD} \ge 1.8 \text{ V}$ for Temp > 0 °C)	_	±12	-	mV	
SID86	V <sub>HYST</sub>	Hysteresis when enabled, Common Mode voltage range from 0 to $V_{DD}$ -1.	_	10	35	mV	Guaranteed by characterization
SID87	V <sub>ICM1</sub>	Input common mode voltage in normal mode	0	-	V <sub>DDD</sub> – 0.1	V	Modes 1 and 2.
SID247	V <sub>ICM2</sub>	Input common mode voltage in low power mode ( $V_{DDD} \ge 2.2 \text{ V}$ for Temp < 0 °C, $V_{DDD} \ge 1.8 \text{ V}$ for Temp > 0 °C)	0	-	V <sub>DDD</sub>	V	
SID247A	V <sub>ICM3</sub>	Input common mode voltage in ultra low power mode	0	-	V <sub>DDD</sub> – 1.15	V	
SID88	CMRR	Common mode rejection ratio	50	-	-	dB	$V_{DDD} \ge 2.7 V.$ Guaranteed by characterization
SID88A	CMRR	Common mode rejection ratio	42	-	-	dB	V <sub>DDD</sub> < 2.7 V. Guaranteed by characterization
SID89	I <sub>CMP1</sub>	Block current, normal mode	-	-	400	μA	Guaranteed by characterization
SID248	I <sub>CMP2</sub>	Block current, low power mode	_	-	100	μA	Guaranteed by characterization
SID259	I <sub>CMP3</sub>	Block current, ultra low power mode $(V_{DDD} \ge 2.2 \text{ V for Temp} < 0 ^{\circ}\text{C}, V_{DDD} \ge 1.8 \text{ V for Temp} > 0 ^{\circ}\text{C})$	_	6	28	μA	Guaranteed by characterization
SID90	Z <sub>CMP</sub>	DC input impedance of comparator	35	-	-	MΩ	Guaranteed by characterization



## **Digital Peripherals**

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode.

Timer/Counter/PWM

## Table 15. TCPWM Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID.TCPWM.1	ITCPWM1	Block current consumption at 3 MHz	-	-	45	μA	All modes (TCPWM)
SID.TCPWM.2	ITCPWM2	Block current consumption at 12 MHz	-	-	155	μA	All modes (TCPWM)
SID.TCPWM.2A	ITCPWM3	Block current consumption at 48 MHz	-	-	650	μA	All modes (TCPWM)
SID.TCPWM.3	TCPWMFREQ	Operating frequency	-	-	Fc	MHz	Fc max = Fcpu. Maximum = 24 MHz
SID.TCPWM.4	TPWMENEXT	Input Trigger Pulse Width for all Trigger Events	2/Fc	_	_	ns	Trigger events can be Stop, Start, Reload, Count, Capture, or Kill depending on which mode of operation is selected.
SID.TCPWM.5	TPWMEXT	Output Trigger Pulse widths	2/Fc	-	_	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) trigger outputs
SID.TCPWM.5A	TCRES	Resolution of Counter	1/Fc	-	-	ns	Minimum time between successive counts
SID.TCPWM.5B	PWMRES	PWM Resolution	1/Fc	-	-	ns	Minimum pulse width of PWM Output
SID.TCPWM.5C	QRES	Quadrature inputs resolution	1/Fc	_	_	ns	Minimum pulse width between Quadrature phase inputs.

βC

## Table 16. Fixed I<sup>2</sup>C DC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	<b>Details/Conditions</b>
SID149	I <sub>I2C1</sub>	Block current consumption at 100 kHz	-	-	50	μA	
SID150	I <sub>I2C2</sub>	Block current consumption at 400 kHz	-	-	135	μA	
SID151	I <sub>I2C3</sub>	Block current consumption at 1 Mbps	_	-	310	μA	
SID152	I <sub>I2C4</sub>	I <sup>2</sup> C enabled in Deep Sleep mode	_	-	1.4	μA	

## Table 17. Fixed I<sup>2</sup>C AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	<b>Details/Conditions</b>
SID153	F <sub>I2C1</sub>	Bit rate	-	-	1	Mbps	

#### LCD Direct Drive

#### Table 18. LCD Direct Drive DC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID154	ILCDLOW	Operating current in low power mode	_	5	-	μA	16 × 4 small segment disp. at 50 Hz
SID155	C <sub>LCDCAP</sub>	LCD capacitance per segment/common driver	-	500	5000	pF	Guaranteed by Design
SID156	LCD <sub>OFFSET</sub>	Long-term segment offset	-	20	-	mV	
SID157	I <sub>LCDOP1</sub>	PWM Mode current. 5-V bias. 24-MHz IMO. 25 °C	-	0.6	-	mA	32 × 4 segments. 50 Hz
SID158	I <sub>LCDOP2</sub>	PWM Mode current. 3.3-V bias. 24-MHz IMO. 25 °C	_	0.5	-	mA	32 × 4 segments. 50 Hz



#### Table 19. LCD Direct Drive AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID159	F <sub>LCD</sub>	LCD frame rate	10	50	150	Hz	

## Table 20. Fixed UART DC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID160	I <sub>UART1</sub>	Block current consumption at 100 Kbps	-	-	55	μA	
SID161	I <sub>UART2</sub>	Block current consumption at 1000 Kbps	-	-	312	μA	

### Table 21. Fixed UART AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID162	F <sub>UART</sub>	Bit rate	-	-	1	Mbps	

#### SPI Specifications

#### Table 22. Fixed SPI DC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID163	I <sub>SPI1</sub>	Block current consumption at 1 Mbps	-	-	360	μA	
SID164	I <sub>SPI2</sub>	Block current consumption at 4 Mbps	-	-	560	μA	
SID165	I <sub>SPI3</sub>	Block current consumption at 8 Mbps	-	-	600	μΑ	

#### Table 23. Fixed SPI AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID166	F <sub>SPI</sub>	SPI operating frequency (master; 6X oversampling)	-	-	4	MHz	

## Table 24. Fixed SPI Master Mode AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID167	T <sub>DMO</sub>	MOSI valid after Sclock driving edge	-	-	15	ns	
SID168	T <sub>DSI</sub>	MISO valid before Sclock capturing edge. Full clock, late MISO Sampling used	20	-	-	ns	
SID169	Т <sub>НМО</sub>	Previous MOSI data hold time with respect to capturing edge at Slave	0	-	Ι	ns	

#### Table 25. Fixed SPI Slave Mode AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID170	Т <sub>DMI</sub>	MOSI valid before Sclock capturing edge	40	-	-	ns	
SID171	T <sub>DSO</sub>	MISO valid after Sclock driving edge	-	-	42+3× Tscbclk	ns	
SID171A	T <sub>DSO_ext</sub>	MISO valid after Sclock driving edge in Ext. Clock mode	-	-	48	ns	
SID172	T <sub>HSO</sub>	Previous MISO data hold time	0	-	-	ns	
SID172A	T <sub>SSELSCK</sub>	SSEL Valid to first SCK Valid edge	100	-	_	ns	



#### Voltage Monitors

## Table 30. Voltage Monitors DC Specifications

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID195	V <sub>LVI1</sub>	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	
SID196	V <sub>LVI2</sub>	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	
SID197	V <sub>LVI3</sub>	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	
SID198	V <sub>LVI4</sub>	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	
SID199	V <sub>LVI5</sub>	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	
SID200	V <sub>LVI6</sub>	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	
SID201	V <sub>LVI7</sub>	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	
SID202	V <sub>LVI8</sub>	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	
SID203	V <sub>LVI9</sub>	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	
SID204	V <sub>LVI10</sub>	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	
SID205	V <sub>LVI11</sub>	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	
SID206	V <sub>LVI12</sub>	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	
SID207	V <sub>LVI13</sub>	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	
SID208	V <sub>LVI14</sub>	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	
SID209	V <sub>LVI15</sub>	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	
SID210	V <sub>LVI16</sub>	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	
SID211	LVI_IDD	Block current	_	-	100	μA	Guaranteed by characterization

## Table 31. Voltage Monitors AC Specifications

Spec ID	Parameter	Description	Min	Тур	Мах	Units	Details/Conditions
SID212	T <sub>MONTRIP</sub>	Voltage monitor trip time	1	1	1	μs	Guaranteed by characterization

## SWD Interface

## Table 32. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID213	F_SWDCLK1	$3.3 \text{ V} \leq \text{V}_{DD} \leq 5.5 \text{ V}$	_	_	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F_SWDCLK2	$1.71 \text{ V} \le \text{V}_{DD} \le 3.3 \text{ V}$	_	_	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID215	T_SWDI_SETUP	T = 1/f SWDCLK	0.25*T	_	_	ns	Guaranteed by characterization
SID216	T_SWDI_HOLD	T = 1/f SWDCLK	0.25*T	_	_	ns	Guaranteed by characterization
SID217	T_SWDO_VALID	T = 1/f SWDCLK	_	_	0.5*T	ns	Guaranteed by characterization
SID217A	T_SWDO_HOLD	T = 1/f SWDCLK	1	-	_	ns	Guaranteed by characterization



#### Internal Main Oscillator

#### Table 33. IMO DC Specifications (Guaranteed by Design)

Spec ID	Parameter	Description	Min	Тур	Max	Units	<b>Details/Conditions</b>
SID218	I <sub>IMO1</sub>	IMO operating current at 48 MHz	-	-	1000	μA	
SID219	I <sub>IMO2</sub>	IMO operating current at 24 MHz	-	_	325	μA	
SID220	I <sub>IMO3</sub>	IMO operating current at 12 MHz	-	_	225	μA	
SID221	I <sub>IMO4</sub>	IMO operating current at 6 MHz	-	_	180	μA	
SID222	I <sub>IMO5</sub>	IMO operating current at 3 MHz	-	_	150	μA	

## Table 34. IMO AC Specifications

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID223	F <sub>IMOTOL1</sub>	Frequency variation from 3 to 48 MHz	-	-	±2		±3% if T <sub>A</sub> > 85 °C and IMO frequency < 24 MHz
SID226	T <sub>STARTIMO</sub>	IMO startup time	-	-	12	μs	
SID227	T <sub>JITRMSIMO1</sub>	RMS Jitter at 3 MHz	-	156	-	ps	
SID228	T <sub>JITRMSIMO2</sub>	RMS Jitter at 24 MHz	-	145	-	ps	
SID229	T <sub>JITRMSIMO3</sub>	RMS Jitter at 48 MHz	_	139	_	ps	

#### Internal Low-Speed Oscillator

## Table 35. ILO DC Specifications (Guaranteed by Design)

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID231	I <sub>ILO1</sub>	ILO operating current at 32 kHz	_	0.3	1.05		Guaranteed by Characterization
SID233	IILOLEAK	ILO leakage current	_	2	15	nA	Guaranteed by Design

#### Table 36. ILO AC Specifications

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID234	T <sub>STARTILO1</sub>	ILO startup time	-	-	2	ms	Guaranteed by charac- terization
SID236	T <sub>ILODUTY</sub>	ILO duty cycle	40	50	60	%	Guaranteed by charac- terization
SID237	F <sub>ILOTRIM1</sub>	32 kHz trimmed frequency	15	32	50	kHz	Max ILO frequency is 70 kHz if T <sub>A</sub> > 85 °C

#### Table 37. External Clock Specifications

Spec ID	Parameter	Description	Min	Тур	Мах	Units	Details/Conditions
SID305	ExtClkFreq	External Clock input Frequency	0	-	24	MHz	Guaranteed by characterization
SID306	ExtClkDuty	Duty cycle; Measured at $V_{DD/2}$	45	1	55	%	Guaranteed by characterization



## Table 38. Block Specs

Spec ID	Parameter	Description	Min	Тур	Max	Units	Details/Conditions
SID257	T <sub>WS24</sub> *	Number of wait states at 24 MHz	0	-	-		CPU execution from Flash. Guaranteed by characterization
SID260	V <sub>REFSAR</sub>	Trimmed internal reference to SAR	–1	-	+1	%	Percentage of Vbg (1.024 V). Guaranteed by characterization
SID262	T <sub>CLKSWITCH</sub>	Clock switching from clk1 to clk2 in clk1 periods	3	-	4	Periods	Guaranteed by design
* Tws24 is gu	aranteed by Design	· · · ·		1		•	•



## Packaging

## Table 40. Package Characteristics

Parameter	Description	Conditions	Min	Тур	Max	Units
T <sub>A</sub>	Operating ambient temperature		-40	25.00	105	°C
TJ	Operating junction temperature		-40	-	125	°C
T <sub>JA</sub>	Package $\theta_{JA}$ (28-pin SSOP)		-	66.58	-	°C/Watt
T <sub>JA</sub>	Package $\theta_{JA}$ (35-ball WLCSP)		-	28.00	-	°C/Watt
T <sub>JA</sub>	Package $\theta_{JA}$ (40-pin QFN)		-	15.34	-	°C/Watt
T <sub>JA</sub>	Package $\theta_{JA}$ (44-pin TQFP)		-	57.16	-	°C/Watt
T <sub>JA</sub>	Package $\theta_{JA}$ (48-pin TQFP)		-	67.30	-	°C/Watt
T <sub>JC</sub>	Package $\theta_{JC}$ (28-pin SSOP)		-	26.28	-	°C/Watt
T <sub>JC</sub>	Package $\theta_{JC}$ (35-ball WLCSP)		-	00.40	-	°C/Watt
T <sub>JC</sub>	Package $\theta_{JC}$ (40-pin QFN)		-	2.50	-	°C/Watt
T <sub>JC</sub>	Package $\theta_{JC}$ (44-pin TQFP)		-	17.47	_	°C/Watt
T <sub>JC</sub>	Package $\theta_{JC}$ (48-pin TQFP)		-	27.60	-	°C/Watt

#### Table 41. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time at Peak Temperature
28-pin SSOP	260 °C	30 seconds
35-ball WLCSP	260 °C	30 seconds
40-pin QFN	260 °C	30 seconds
44-pin TQFP	260 °C	30 seconds
48-pin TQFP	260 °C	30 seconds

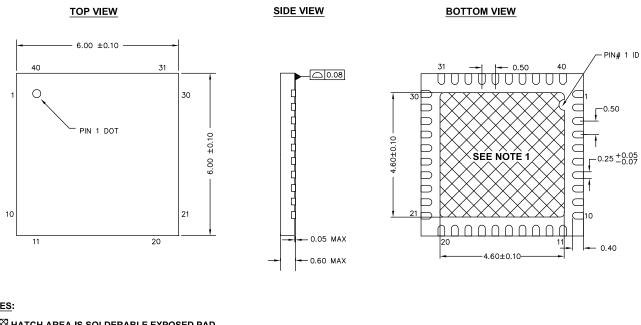
#### Table 42. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
28-pin SSOP	MSL 3
35-ball WLCSP	MSL 3
40-pin QFN	MSL 3
44-pin TQFP	MSL 3
48-pin TQFP	MSL 3

PSoC 4 CAB Libraries with Schematics Symbols and PCB Footprints are on the Cypress web site at http://www.cypress.com/cad-resources/psoc-4-cad-libraries?source=search&cat=technical\_documents.







NOTES:

1. XXX HATCH AREA IS SOLDERABLE EXPOSED PAD

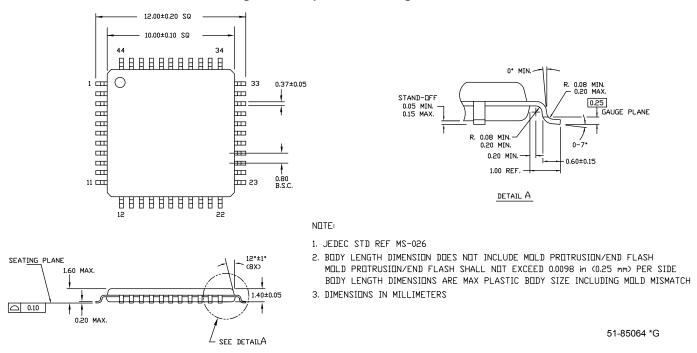
2. REFERENCE JEDEC # MO-248

3. PACKAGE WEIGHT: 68 ±2 mg

4. ALL DIMENSIONS ARE IN MILLIMETERS

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.

Figure 18. 44-pin TQFP Package Outline



001-80659 \*A