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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I ² C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 8x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4125axi-473

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Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in PSoC 4100 is part of the 32-bit MCU subsystem, which is optimized for low power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from Deep Sleep mode allowing power to be switched off to the main processor when the chip is in Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt input (NMI), which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG; the debug configuration used for PSoC 4100 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

PSoC 4100 has a flash module with a flash accelerator tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 0 wait-state (WS) access time at 24 MHz. Part of the flash module can be used to emulate EEPROM operation if required.

The PSoC 4200 Flash supports the following flash protection modes at the memory subsystem level:

- **Open: No Protection.** Factory default mode in which the product is shipped.
- **Protected: User may change from Open to Protected.** This mode disables Debug interface accesses. The mode can be set back to Open but only after completely erasing the Flash.
- **Kill: User may change from Open to Kill.** This mode disables all Debug accesses. The part cannot be erased externally, thus obviating the possibility of partial erasure by power interruption and potential malfunction and security leaks. This is an irrevocable mode.

In addition, row-level Read/Write protection is also supported to prevent inadvertent Writes as well as selectively block Reads. Flash Read/Write/Erase operations are always available for internal code using system calls.

SRAM

SRAM memory is retained during Hibernate.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

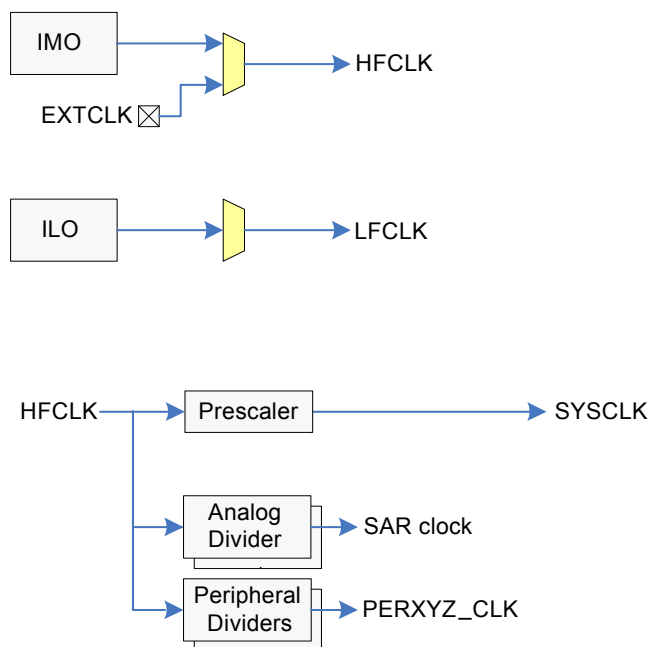
The power system is described in detail in the section [Power on page 15](#). It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low-voltage detect (LVD)). The PSoC 4100 operates with a single external supply over the range of 1.71 V to 5.5 V and has five different power modes, transitions between which are managed by the power system. PSoC 4100 provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

Clock System

The PSoC 4100 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for PSoC 4100 consists of the internal main oscillator (IMO) and the internal low-power oscillator (ILO) and provision for an external clock.

Figure 3. PSoC 4100 MCU Clocking Architecture



The HFCLK signal can be divided down (see [PSoC 4100 MCU Clocking Architecture](#)) to generate synchronous clocks for the analog and digital peripherals. There are a total of 12 clock dividers for PSoC 4100, each with 16-bit divide capability. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator.

GPIO

PSoC 4100 has 36 GPIOs. The GPIO block implements the following:

- Eight drive strength modes:
 - Analog input mode (input and output buffers disabled)
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL).
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes.
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes).
- Selectable slew rates for dV/dt related noise control to improve EMI.

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves. Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (5 for PSoC 4100 since it has 4.5 ports).

Special Function Peripherals

LCD Segment Drive

PSoC 4100 has an LCD controller which can drive up to four commons and up to 32 segments. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD

voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

CapSense

CapSense is supported on all pins in the PSoC 4100 through a CapSense Sigma-Delta (CSD) block that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CapSense function can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CapSense block to make it easy for the user.

Shield voltage can be driven on another mux bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

The CapSense block has two IDACs which can be used for general purposes if CapSense is not being used. (both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available).

WLCSP Package Bootloader

The WLCSP package is supplied with an I²C Bootloader installed in flash. The bootloader is compatible with PSoC Creator bootloadable project files and has the following default settings:

- I²C SCL and SDA connected to port pins P4.0 and P4.1 respectively (external pull-up resistors required)
- I²C Slave mode, address 8, data rate = 100 kbps
- Single application
- Wait two seconds for bootstrap command
- Other bootloader options are as set by the PSoC Creator Bootloader Component default
- Occupies the bottom 4.5 K of flash

For more information on this bootloader, see the following Cypress application notes:

[AN73854](#) - Introduction to Bootloaders

Note that a PSoC Creator bootloadable project must be associated with .hex and .elf files for a bootloader project that is configured for the target device. Bootloader .hex and .elf files can be found at <http://www.cypress.com/?rID=78805>. The factory-installed bootloader can be overwritten using JTAG or SWD programming.

The following is the pin-list for the PSoC 4100 (35-WLCSP).

35-Ball CSP		Alternate Functions for Pins					Pin Description
Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
D3	P2.2	sarmux.2	–	–	–	–	Port 2 Pin 2: gpio, lcd, csd, sarmux
E4	P2.3	sarmux.3	–	–	–	–	Port 2 Pin 3: gpio, lcd, csd, sarmux
E5	P2.4	sarmux.4	tcpwm0_p[1]	–	–	–	Port 2 Pin 4: gpio, lcd, csd, sarmux, pwm
E6	P2.5	sarmux.5	tcpwm0_n[1]	–	–	–	Port 2 Pin 5: gpio, lcd, csd, sarmux, pwm
E3	P2.6	sarmux.6	tcpwm1_p[1]	–	–	–	Port 2 Pin 6: gpio, lcd, csd, sarmux, pwm
E2	P2.7	sarmux.7	tcpwm1_n[1]	–	–	–	Port 2 Pin 7: gpio, lcd, csd, sarmux, pwm
E1	P3.0	–	tcpwm0_p[0]	scb1_uart_rx[0]	scb1_i2c_scl[0]	scb1_spi_mosi[0]	Port 3 Pin 0: gpio, lcd, csd, pwm, scb1
D2	P3.1	–	tcpwm0_n[0]	scb1_uart_tx[0]	scb1_i2c_sda[0]	scb1_spi_miso[0]	Port 3 Pin 1: gpio, lcd, csd, pwm, scb1
D1	P3.2	–	tcpwm1_p[0]	–	swd_io[0]	scb1_spi_clk[0]	Port 3 Pin 2: gpio, lcd, csd, pwm, scb1, swd
B7	VSS	–	–	–	–	–	Ground
C1	P3.3	–	tcpwm1_n[0]	–	swd_clk[0]	scb1_spi_ssel_0[0]	Port 3 Pin 3: gpio, lcd, csd, pwm, scb1, swd
C2	P3.4	–	tcpwm2_p[0]	–	–	scb1_spi_ssel_1	Port 3 Pin 4: gpio, lcd, csd, pwm, scb1
B1	P4.0	–	–	scb0_uart_rx	scb0_i2c_scl	scb0_spi_mosi	Port 4 Pin 0: gpio, lcd, csd, scb0
B2	P4.1	–	–	scb0_uart_tx	scb0_i2c_sda	scb0_spi_miso	Port 4 Pin 1: gpio, lcd, csd, scb0
A2	P4.2	csd_c_mod	–	–	–	scb0_spi_clk	Port 4 Pin 2: gpio, lcd, csd, scb0
A1	P4.3	csd_c_sh_tank	–	–	–	scb0_spi_ssel_0	Port 4 Pin 3: gpio, lcd, csd, scb0
C3	P0.0	comp1_inp	–	–	–	scb0_spi_ssel_1	Port 0 Pin 0: gpio, lcd, csd, scb0, comp
A5	P0.1	comp1_inn	–	–	–	scb0_spi_ssel_2	Port 0 Pin 1: gpio, lcd, csd, scb0, comp
A4	P0.2	comp2_inp	–	–	–	scb0_spi_ssel_3	Port 0 Pin 2: gpio, lcd, csd, scb0, comp
A3	P0.3	comp2_inn	–	–	–	–	Port 0 Pin 3: gpio, lcd, csd, comp
B3	P0.4	–	–	scb1_uart_rx[1]	scb1_i2c_scl[1]	scb1_spi_mosi[1]	Port 0 Pin 4: gpio, lcd, csd, scb1
A6	P0.5	–	–	scb1_uart_tx[1]	scb1_i2c_sda[1]	scb1_spi_miso[1]	Port 0 Pin 5: gpio, lcd, csd, scb1
B4	P0.6	–	ext_clk	–	–	scb1_spi_clk[1]	Port 0 Pin 6: gpio, lcd, csd, scb1, ext_clk
B5	P0.7	–	–	–	wakeup	scb1_spi_ssel_0[1]	Port 0 Pin 7: gpio, lcd, csd, scb1, wakeup
B6	XRES	–	–	–	–	–	Chip reset, active low
A7	VCCD	–	–	–	–	–	Regulated supply, connect to 1µF cap or 1.8V
C7	VDD	–	–	–	–	–	Supply, 1.8 - 5.5V
C4	P1.0	ctb.oa0.inp	tcpwm2_p[1]	–	–	–	Port 1 Pin 0: gpio, lcd, csd, ctb, pwm
C5	P1.1	ctb.oa0.inm	tcpwm2_n[1]	–	–	–	Port 1 Pin 1: gpio, lcd, csd, ctb, pwm

35-Ball CSP		Alternate Functions for Pins					Pin Description
Pin	Name	Analog	Alt 1	Alt 2	Alt 3	Alt 4	
C6	P1.2	ctb.0a0.out	tcpwm3_p[1]	–	–	–	Port 1 Pin 2: gpio, lcd, csd, ctb, pwm
D7	P1.3	ctb.0a1.out	tcpwm3_n[1]	–	–	–	Port 1 Pin 3: gpio, lcd, csd, ctb, pwm
D4	P1.4	ctb.0a1.inm	–	–	–	–	Port 1 Pin 4: gpio, lcd, csd, ctb
D5	P1.5	ctb.0a1.inp	–	–	–	–	Port 1 Pin 5: gpio, lcd, csd, ctb
D6	P1.6	ctb.0a0.inp_alt	–	–	–	–	Port 1 Pin 6: gpio, lcd, csd
E7	P1.7/VREF	ctb.0a1.inp_alt ext_vref	–	–	–	–	Port 1 Pin 7: gpio, lcd, csd, ext_ref

Descriptions of the Pin functions are as follows:

VDDD: Power supply for both analog and digital sections (where there is no V_{DDA} pin).

VDDA: Analog V_{DD} pin where package pins allow; shorted to V_{DDD} otherwise.

VSSA: Analog ground pin where package pins allow; shorted to VSS otherwise

VSS: Ground pin.

VCCD: Regulated Digital supply (1.8 V $\pm$ 5%).

Port Pins can all be used as LCD Commons, LCD Segment drivers, or CSD sense and shield pins can be connected to AMUXBUS A or B or can all be used as GPIO pins that can be driven by firmware or DSI signals.

The following packages are supported: 48-pin TQFP, 44-pin TQFP, 40-pin QFN, and 28-pin SSOP.

Figure 5. 48-Pin TQFP Pinout

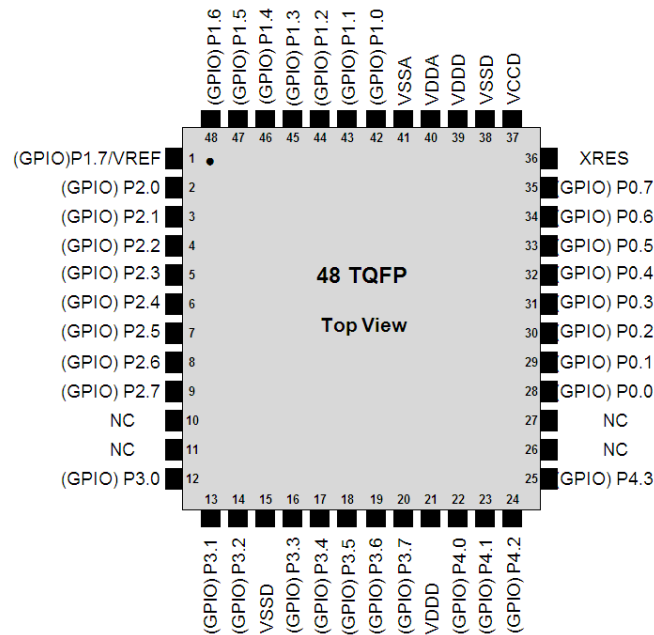
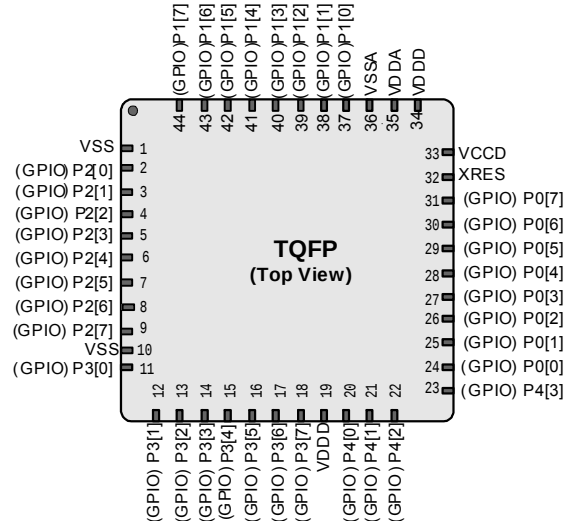


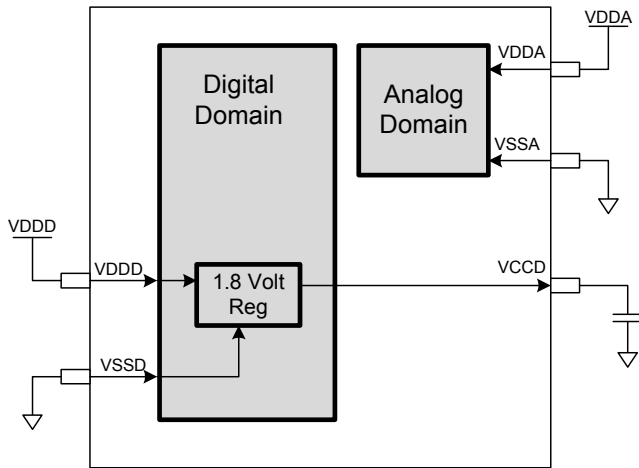
Figure 6. 44-pin TQFP Part Pinout



Power

The following power system diagrams show the minimum set of power supply pins as implemented for PSoC 4100. The system has one regulator in Active mode for the digital circuitry. There is no analog regulator; the analog circuits run directly from the V_{DDA} input. There are separate regulators for the Deep Sleep and Hibernate (lowered power supply and retention) modes. There is a separate low-noise regulator for the bandgap. The supply voltage range is 1.71 V to 5.5 V with all functions and circuits operating over that range.

Figure 10. PSoC 4 Power Supply



The PSoC 4100 family allows two distinct modes of power supply operation: Unregulated External Supply, and Regulated External Supply modes.

Unregulated External Supply

In this mode, PSoC 4100 is powered by an external power supply that can be anywhere in the range of 1.8 V to 5.5 V. This range is also designed for battery-powered operation, for instance, the chip can be powered from a battery system that starts at 3.5 V and works down to 1.8 V. In this mode, the internal regulator of PSoC 4100 supplies the internal logic and the V_{CCD} output of the PSoC 4100 must be bypassed to ground via an external Capacitor (in the range of 1 μF to 1.6 μF ; X5R ceramic or better).

V_{DDA} and V_{DDDD} must be shorted together; the grounds, V_{SSA} and V_{SS} must also be shorted together. Bypass capacitors must be used from V_{DDDD} to ground, typical practice for systems in this frequency range is to use a capacitor in the 1- μF range in parallel with a smaller capacitor (0.1 μF for example). Note that these are simply rules of thumb and that, for critical applications, the PCB layout, lead inductance, and the Bypass capacitor parasitic should be simulated to design and obtain optimal bypassing.

Figure 11. 48-TQFP Package Example

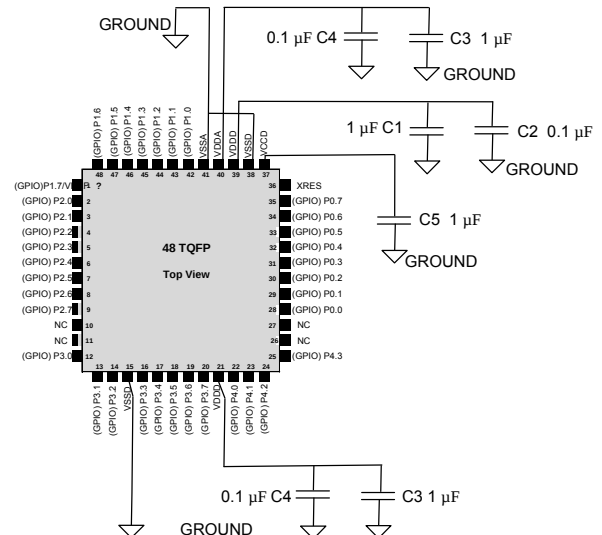
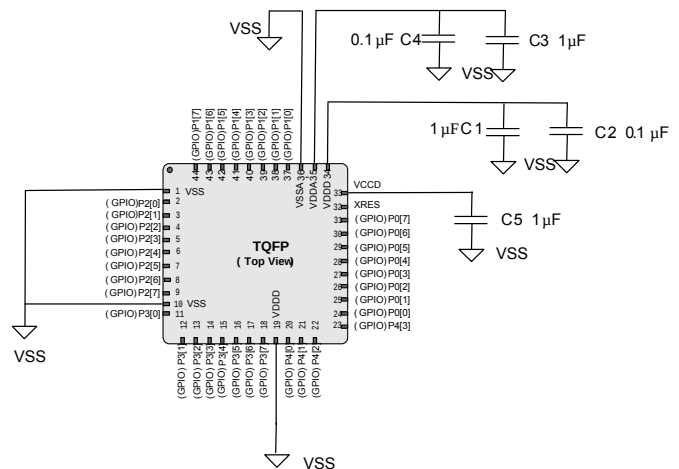


Figure 12. 44-TQFP Package Example



Power Supply	Bypass Capacitors
VDDDD–VSS	0.1 μF ceramic at each pin (C2, C6) plus bulk capacitor 1 to 10 μF (C1). Total capacitance may be greater than 10 μF .
VDDA–VSSA	0.1 μF ceramic at pin (C4). Additional 1 μF to 10 μF (C3) bulk capacitor. Total capacitance may be greater than 10 μF .
VCCD–VSS	1 μF ceramic capacitor at the VCCD pin (C5)
VREF–VSSA (optional)	The internal bandgap may be bypassed with a 1 μF to 10 μF capacitor. Total capacitance may be greater than 10 μF .

GPIO
Table 4. GPIO DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID57	$V_{IH}^{[2]}$	Input voltage high threshold	$0.7 \times V_{DD}$	–	–	V	CMOS Input
SID58	V_{IL}	Input voltage low threshold	–	–	$0.3 \times V_{DD}$	V	CMOS Input
SID241	$V_{IH}^{[2]}$	LVTTL input, $V_{DD} < 2.7$ V	$0.7 \times V_{DD}$	–	–	V	
SID242	V_{IL}	LVTTL input, $V_{DD} < 2.7$ V	–	–	$0.3 \times V_{DD}$	V	
SID243	$V_{IH}^{[2]}$	LVTTL input, $V_{DD} \geq 2.7$ V	2.0	–	–	V	
SID244	V_{IL}	LVTTL input, $V_{DD} \geq 2.7$ V	–	–	0.8	V	
SID59	V_{OH}	Output voltage high level	$V_{DD} - 0.6$	–	–	V	$I_{OH} = 4$ mA at 3-V V_{DD}
SID60	V_{OH}	Output voltage high level	$V_{DD} - 0.5$	–	–	V	$I_{OH} = 1$ mA at 1.8-V V_{DD}
SID61	V_{OL}	Output voltage low level	–	–	0.6	V	$I_{OL} = 4$ mA at 1.8-V V_{DD}
SID62	V_{OL}	Output voltage low level	–	–	0.6	V	$I_{OL} = 8$ mA at 3-V V_{DD}
SID62A	V_{OL}	Output voltage low level	–	–	0.4	V	$I_{OL} = 3$ mA at 3-V V_{DD}
SID63	R_{PULLUP}	Pull-up resistor	3.5	5.6	8.5	k Ω	
SID64	$R_{PULLDOWN}$	Pull-down resistor	3.5	5.6	8.5	k Ω	
SID65	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	25 °C, $V_{DD} = 3.0$ -V
SID65A	I_{IL_CTBM}	Input leakage current (absolute value) for CTBM pins	–	–	4	nA	
SID66	C_{IN}	Input capacitance	–	–	7	pF	
SID67	V_{HYSTTL}	Input hysteresis LVTTL	25	40	–	mV	$V_{DD} \geq 2.7$ V. Guaranteed by characterization
SID68	$V_{HYSCMOS}$	Input hysteresis CMOS	$0.05 \times V_{DD}$	–	–	mV	Guaranteed by characterization
SID69	I_{DIODE}	Current through protection diode to V_{DD}/V_{SS}	–	–	100	μ A	Guaranteed by characterization
SID69A	I_{TOT_GPIO}	Maximum Total Source or Sink Chip Current	–	–	200	mA	Guaranteed by characterization

Note

 2. V_{IH} must not exceed $V_{DD} + 0.2$ V.

Table 10. Comparator AC Specifications

(Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID91	T _{RESP1}	Response time, normal mode	–	–	110	ns	50-mV overdrive
SID258	T _{RESP2}	Response time, low power mode	–	–	200	ns	50-mV overdrive
SID92	T _{RESP3}	Response time, ultra low power mode (V _{DD} ≥ 2.2 V for Temp < 0 °C, V _{DD} ≥ 1.8 V for Temp > 0 °C)	–	–	15	µs	200-mV overdrive

Temperature Sensor

Table 11. Temperature Sensor Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID93	T _{SENSACC}	Temperature sensor accuracy	–5	±1	+5	°C	–40 to +85 °C

SAR ADC

Table 12. SAR ADC DC Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID94	A_RES	Resolution	–	–	12	bits	
SID95	A_CHNIS_S	Number of channels - single ended	–	–	8		8 full speed
SID96	A-CHNKS_D	Number of channels - differential	–	–	4		Diff inputs use neighboring I/O
SID97	A-MONO	Monotonicity	–	–	–		Yes. Based on characterization
SID98	A_GAINERR	Gain error	–	–	±0.1	%	With external reference. Guaranteed by characterization
SID99	A_OFFSET	Input offset voltage	–	–	2	mV	Measured with 1-V V _{REF} . Guaranteed by characterization
SID100	A_ISAR	Current consumption	–	–	1	mA	
SID101	A_VINS	Input voltage range - single ended	V _{SS}	–	V _{DDA}	V	Based on device characterization
SID102	A_VIND	Input voltage range - differential	V _{SS}	–	V _{DDA}	V	Based on device characterization
SID103	A_INRES	Input resistance	–	–	2.2	KΩ	Based on device characterization
SID104	A_INCAP	Input capacitance	–	–	10	pF	Based on device characterization
SID106	A_PSR	Power supply rejection ratio	70	–	–	dB	
SID107	A_CMRR	Common mode rejection ratio	66	–	–	dB	Measured at 1 V
SID111	A_INL	Integral non linearity	–1.7	–	+2	LSB	V _{DD} = 1.71 to 5.5, 806 ksp, V _{REF} = 1 to 5.5.
SID111A	A_INL	Integral non linearity	–1.5	–	+1.7	LSB	V _{DD} = 1.71 to 3.6, 806 ksp, V _{REF} = 1.71 to V _{DD} .

Table 12. SAR ADC DC Specifications *(continued)*

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID111B	A_INL	Integral non linearity	-1.5	–	+1.7	LSB	$V_{DD} = 1.71$ to 5.5, 500 ksp/s, $V_{REF} = 1$ to 5.5.
SID112	A_DNL	Differential non linearity	-1	–	+2.2	LSB	$V_{DD} = 1.71$ to 5.5, 806 ksp/s, $V_{REF} = 1$ to 5.5.
SID112A	A_DNL	Differential non linearity	-1	–	+2	LSB	$V_{DD} = 1.71$ to 3.6, 806 ksp/s, $V_{REF} = 1.71$ to V_{DD} .
SID112B	A_DNL	Differential non linearity	-1	–	+2.2	LSB	$V_{DD} = 1.71$ to 5.5, 500 ksp/s, $V_{REF} = 1$ to 5.5.

Table 13. SAR ADC AC Specifications (Guaranteed by Characterization)

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID108	A_SAMP_1	Sample rate with external reference bypass cap	–	–	806	ksp/s	
SID108A	A_SAMP_2	Sample rate with no bypass cap. Reference = V_{DD}	–	–	500	ksp/s	
SID108B	A_SAMP_3	Sample rate with no bypass cap. Internal reference	–	–	100	ksp/s	
SID109	A_SNDR	Signal-to-noise and distortion ratio (SINAD)	65	–	–	dB	$F_{IN} = 10$ kHz
SID113	A_THD	Total harmonic distortion	–	–	-65	dB	$F_{IN} = 10$ kHz.

CSD
Table 14. CSD Specifications

Spec ID#	Parameter	Description	Min	Typ	Max	Units	Details/ Conditions
SID.CSD#16	IDAC1IDD	IDAC1 (8 bits) block current	–	–	1125	μA	
SID.CSD#17	IDAC2IDD	IDAC2 (7 bits) block current	–	–	1125	μA	
SID308	VCSD	Voltage range of operation	1.71	–	5.5	V	
SID308A	VCOMPIDAC	Voltage compliance range of IDAC for S0	0.8	–	V _{DD} -0.8	V	
SID309	IDAC1	DNL for 8-bit resolution	–1	–	1	LSB	
SID310	IDAC1	INL for 8-bit resolution	–3	–	3	LSB	
SID311	IDAC2	DNL for 7-bit resolution	–1	–	1	LSB	
SID312	IDAC2	INL for 7-bit resolution	–3	–	3	LSB	
SID313	SNR	Ratio of counts of finger to noise, 0.1-pF sensitivity	5	–	–	Ratio	Capacitance range of 9 to 35 pF, 0.1-pF sensitivity
SID314	IDAC1_CRT1	Output current of IDAC1 (8 bits) in High range	–	612	–	uA	
SID314A	IDAC1_CRT2	Output current of IDAC1 (8 bits) in Low range	–	306	–	uA	
SID315	IDAC2_CRT1	Output current of IDAC2 (7 bits) in High range	–	304.8	–	uA	
SID315A	IDAC2_CRT2	Output current of IDAC2 (7 bits) in Low range	–	152.4	–	uA	
SID320	IDACOFFSET	All zeroes input	–	–	±1	LSB	
SID321	IDACGAIN	Full-scale error less offset	–	–	±10	%	
SID322	IDACMISMATCH	Mismatch between IDACs	–	–	7	LSB	
SID323	IDACSET8	Settling time to 0.5 LSB for 8-bit IDAC	–	–	10	μs	Full-scale transition. No external load.
SID324	IDACSET7	Settling time to 0.5 LSB for 7-bit IDAC	–	–	10	μs	Full-scale transition. No external load.
SID325	CMOD	External modulator capacitor	–	2.2	–	nF	5-V rating, X7R or NP0 cap.

Voltage Monitors

Table 30. Voltage Monitors DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID195	V _{LVI1}	LVI_A/D_SEL[3:0] = 0000b	1.71	1.75	1.79	V	
SID196	V _{LVI2}	LVI_A/D_SEL[3:0] = 0001b	1.76	1.80	1.85	V	
SID197	V _{LVI3}	LVI_A/D_SEL[3:0] = 0010b	1.85	1.90	1.95	V	
SID198	V _{LVI4}	LVI_A/D_SEL[3:0] = 0011b	1.95	2.00	2.05	V	
SID199	V _{LVI5}	LVI_A/D_SEL[3:0] = 0100b	2.05	2.10	2.15	V	
SID200	V _{LVI6}	LVI_A/D_SEL[3:0] = 0101b	2.15	2.20	2.26	V	
SID201	V _{LVI7}	LVI_A/D_SEL[3:0] = 0110b	2.24	2.30	2.36	V	
SID202	V _{LVI8}	LVI_A/D_SEL[3:0] = 0111b	2.34	2.40	2.46	V	
SID203	V _{LVI9}	LVI_A/D_SEL[3:0] = 1000b	2.44	2.50	2.56	V	
SID204	V _{LVI10}	LVI_A/D_SEL[3:0] = 1001b	2.54	2.60	2.67	V	
SID205	V _{LVI11}	LVI_A/D_SEL[3:0] = 1010b	2.63	2.70	2.77	V	
SID206	V _{LVI12}	LVI_A/D_SEL[3:0] = 1011b	2.73	2.80	2.87	V	
SID207	V _{LVI13}	LVI_A/D_SEL[3:0] = 1100b	2.83	2.90	2.97	V	
SID208	V _{LVI14}	LVI_A/D_SEL[3:0] = 1101b	2.93	3.00	3.08	V	
SID209	V _{LVI15}	LVI_A/D_SEL[3:0] = 1110b	3.12	3.20	3.28	V	
SID210	V _{LVI16}	LVI_A/D_SEL[3:0] = 1111b	4.39	4.50	4.61	V	
SID211	LVI_IDD	Block current	–	–	100	μA	Guaranteed by characterization

Table 31. Voltage Monitors AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID212	T _{MONTRIP}	Voltage monitor trip time	–	–	1	μs	Guaranteed by characterization

SWD Interface

Table 32. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID213	F _{SWDCLK1}	$3.3\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID214	F _{SWDCLK2}	$1.71\text{ V} \leq V_{DD} \leq 3.3\text{ V}$	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID215	T _{SWDI_SETUP}	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID216	T _{SWDI_HOLD}	T = 1/f SWDCLK	0.25*T	–	–	ns	Guaranteed by characterization
SID217	T _{SWDO_VALID}	T = 1/f SWDCLK	–	–	0.5*T	ns	Guaranteed by characterization
SID217A	T _{SWDO_HOLD}	T = 1/f SWDCLK	1	–	–	ns	Guaranteed by characterization

Internal Main Oscillator
Table 33. IMO DC Specifications (Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID218	I _{IMO1}	IMO operating current at 48 MHz	–	–	1000	μA	
SID219	I _{IMO2}	IMO operating current at 24 MHz	–	–	325	μA	
SID220	I _{IMO3}	IMO operating current at 12 MHz	–	–	225	μA	
SID221	I _{IMO4}	IMO operating current at 6 MHz	–	–	180	μA	
SID222	I _{IMO5}	IMO operating current at 3 MHz	–	–	150	μA	

Table 34. IMO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID223	F _{IMOTOL1}	Frequency variation from 3 to 48 MHz	–	–	±2	%	±3% if T _A > 85 °C and IMO frequency < 24 MHz
SID226	T _{STARTIMO}	IMO startup time	–	–	12	μs	
SID227	T _{JITRMSIMO1}	RMS Jitter at 3 MHz	–	156	–	ps	
SID228	T _{JITRMSIMO2}	RMS Jitter at 24 MHz	–	145	–	ps	
SID229	T _{JITRMSIMO3}	RMS Jitter at 48 MHz	–	139	–	ps	

Internal Low-Speed Oscillator
Table 35. ILO DC Specifications (Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID231	I _{ILO1}	ILO operating current at 32 kHz	–	0.3	1.05	μA	Guaranteed by Characterization
SID233	I _{ILOLEAK}	ILO leakage current	–	2	15	nA	Guaranteed by Design

Table 36. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID234	T _{STARTILO1}	ILO startup time	–	–	2	ms	Guaranteed by characterization
SID236	T _{ILODUTY}	ILO duty cycle	40	50	60	%	Guaranteed by characterization
SID237	F _{ILOTRIM1}	32 kHz trimmed frequency	15	32	50	kHz	Max ILO frequency is 70 kHz if T _A > 85 °C

Table 37. External Clock Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID305	ExtClkFreq	External Clock input Frequency	0	–	24	MHz	Guaranteed by characterization
SID306	ExtClkDuty	Duty cycle; Measured at V _{DD/2}	45	–	55	%	Guaranteed by characterization

Table 38. Block Specs

Spec ID	Parameter	Description	Min	Typ	Max	Units	Details/Conditions
SID257	T _{WS24} *	Number of wait states at 24 MHz	0	–	–		CPU execution from Flash. Guaranteed by characterization
SID260	V _{REFSAR}	Trimmed internal reference to SAR	–1	–	+1	%	Percentage of V _{bg} (1.024 V). Guaranteed by characterization
SID262	T _{CLKSWITCH}	Clock switching from clk1 to clk2 in clk1 periods	3	–	4	Periods	Guaranteed by design

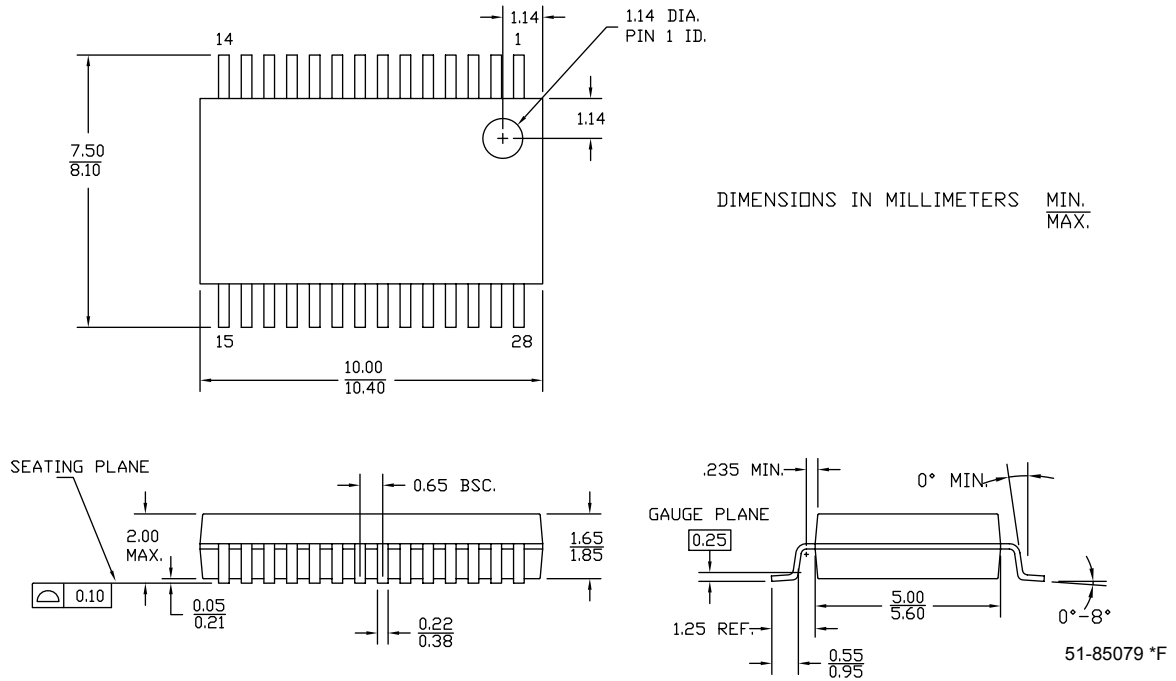
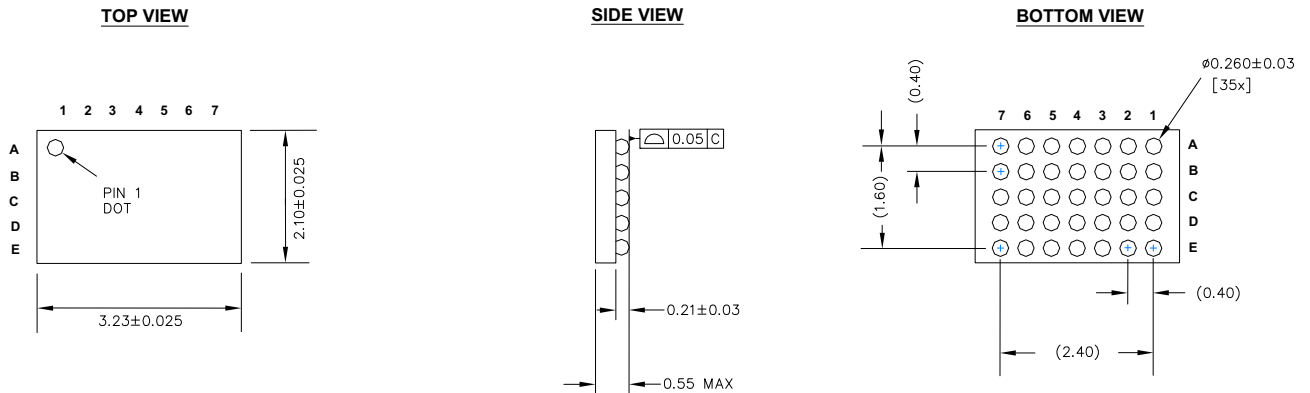
* T_{WS24} is guaranteed by Design

Ordering Information

The PSoC 4100 part numbers and features are listed in the following table.

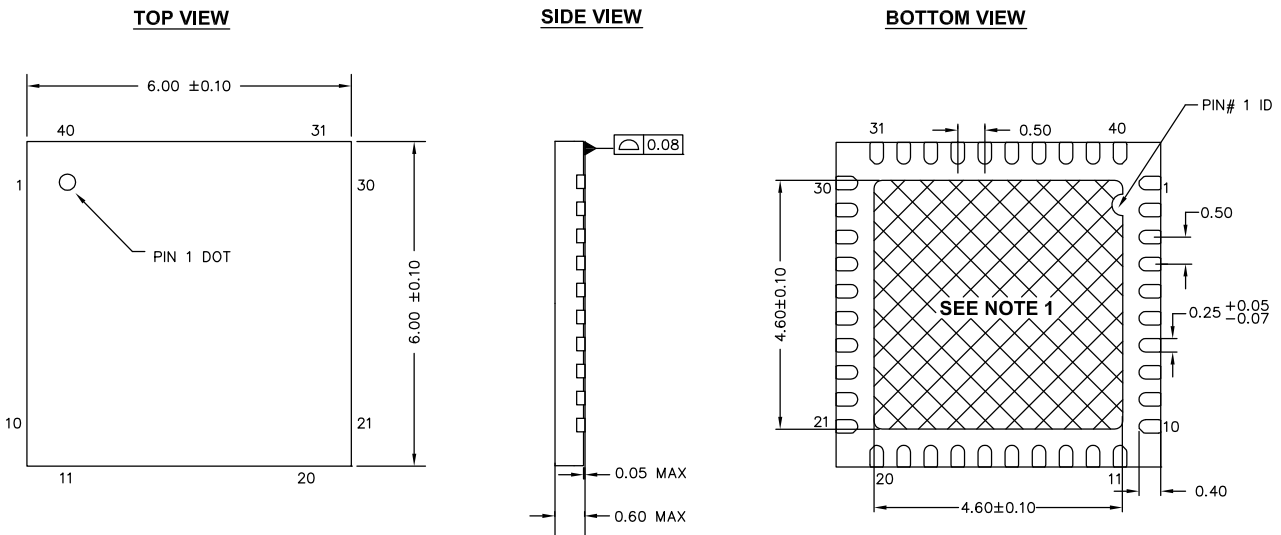
Table 39. PSoC 4100 Family Ordering Information

Family	MPN	Features												Package				
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	UDB	Op-amp (CTBm)	CapSense	Direct LCD Drive	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	GPIO	28-SSOP	35-WLCSP	40-QFN	44-TQFP	48-TQFP
4100	CY8C4124PVI-432	24	16	4	-	1	-	-	806 ksps	2	4	2	24	√				
	CY8C4124PVI-442	24	16	4	-	1	√	√	806 ksps	2	4	2	24	√				
	CY8C4124PVQ-432	24	16	4	-	1	-	-	806 ksps	2	4	2	24	√				
	CY8C4124PVQ-442	24	16	4	-	1	√	√	806 ksps	2	4	2	24	√				
	CY8C4124FNI-443	24	16	4	-	2	√	√	806 ksps	2	4	2	31		√			
	CY8C4124LQI-443	24	16	4	-	2	√	√	806 ksps	2	4	2	34			√		
	CY8C4124AXI-443	24	16	4	-	2	√	√	806 ksps	2	4	2	36				√	
	CY8C4124LQQ-443	24	16	4	-	2	√	√	806 ksps	2	4	2	34			√		
	CY8C4124AXQ-443	24	16	4	-	2	√	√	806 ksps	2	4	2	36				√	
	CY8C4124AZI-443	24	16	4	-	2	√	√	806 ksps	2	4	2	36					√
	CY8C4125AXI-473	24	32	4	-	2	-	-	806 ksps	2	4	2	36				√	
	CY8C4125AXQ-473	24	32	4	-	2	-	-	806 ksps	2	4	2	36				√	
	CY8C4125AZI-473	24	32	4	-	2	-	-	806 ksps	2	4	2	36					√
	CY8C4125PVI-482	24	32	4	-	1	√	√	806 ksps	2	4	2	24	√				
	CY8C4125PVQ-482	24	32	4	-	1	√	√	806 ksps	2	4	2	24	√				
	CY8C4125FNI-483(T)	24	32	4	-	2	√	√	806 ksps	2	4	2	31		√			
	CY8C4125LQI-483	24	32	4	-	2	√	√	806 ksps	2	4	2	34			√		
	CY8C4125AXI-483	24	32	4	-	2	√	√	806 ksps	2	4	2	36				√	
	CY8C4125LQQ-483	24	32	4	-	2	√	√	806 ksps	2	4	2	34			√		
	CY8C4125AXQ-483	24	32	4	-	2	√	√	806 ksps	2	4	2	36				√	
	CY8C4125AZI-483	24	32	4	-	2	√	√	806 ksps	2	4	2	36					√

Figure 15. 28-pin (210-mil) SSOP Package Outline

Figure 16. 35-ball WLCSP Package Outline

NOTES:

1. REFERENCE JEDEC PUBLICATION 95, DESIGN GUIDE 4.18
2. ALL DIMENSIONS ARE IN MILLIMETERS

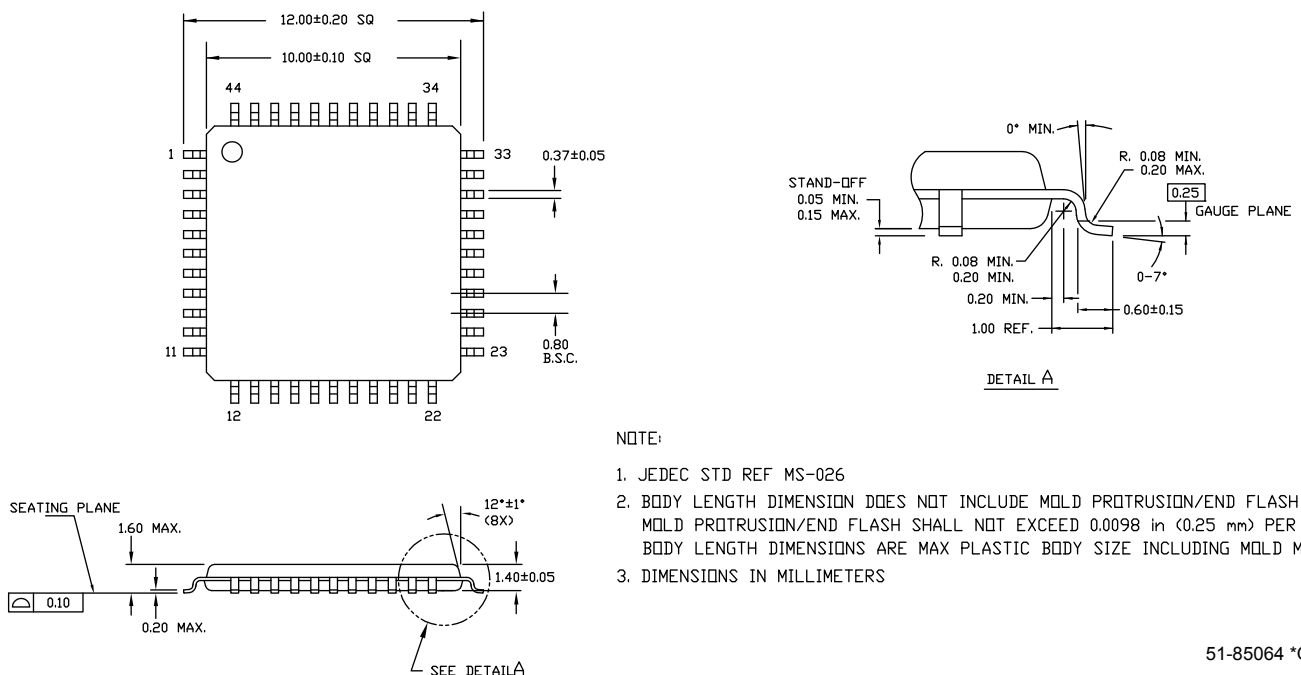
001-93741 **

Figure 17. 40-pin QFN Package Outline

NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

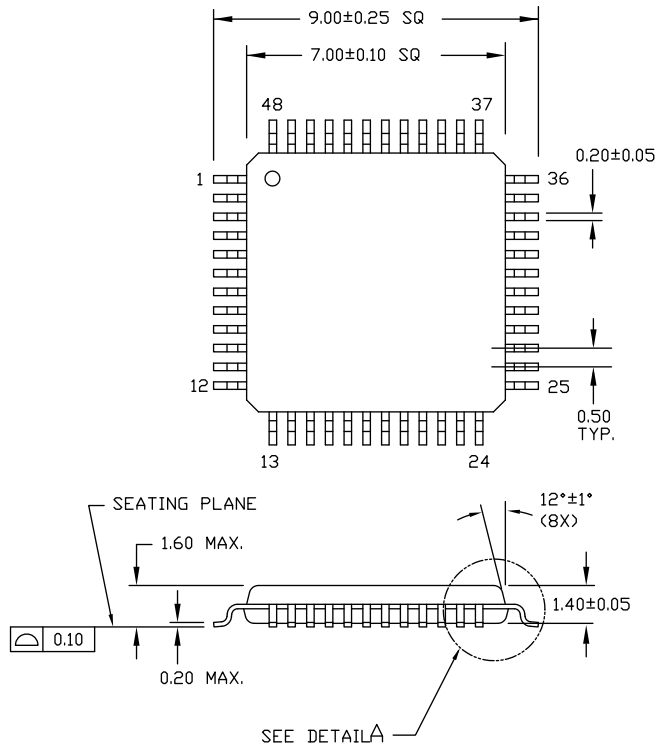
001-80659 *A

The center pad on the QFN package should be connected to ground (VSS) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floating and not connected to any other signal.

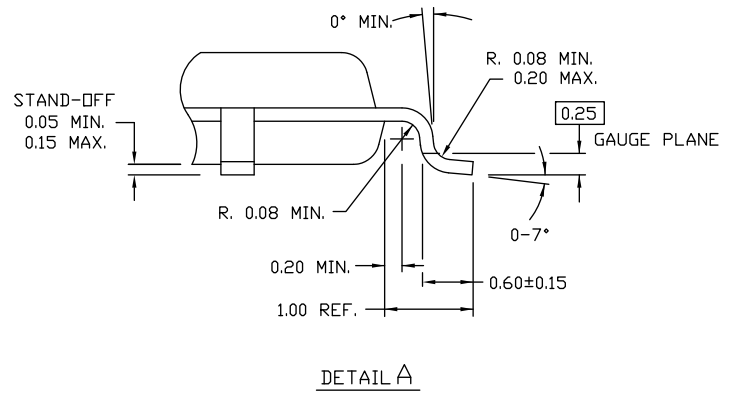
Figure 18. 44-pin TQFP Package Outline

NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS

51-85064 *G

Figure 19. 48-Pin TQFP Package Outline


DIMENSIONS ARE IN MILLIMETERS



51-85135 °C

Revision History

Description Title: PSoC® 4: PSoC 4100 Family Datasheet Programmable System-on-Chip (PSoC®) Document Number:001-87220				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*B	4108562	WKA	08/29/2013	Added clarifying note about the XRES pin in the Reset section. Added a link reference to the PSoC 4 TRM. Updated the footnote in Absolute Maximum Ratings . Updated Sleep Mode IDD specs in DC Specifications . Updated Comparator DC Specifications Updated SAR ADC AC Specifications (Guaranteed by Characterization) Updated LCD Direct Drive DC Specifications (Guaranteed by Characterization) Updated the number of GPIOs in Ordering Information .
*C	4568937	WKA	11/19/2014	Added 48-pin TQFP pin and package details. Added SID308A spec details. Updated Ordering Information .
*D	4617283	WKA	01/08/2015	Corrected typo in the ordering information table. Updated 28-pin SSOP package diagram.
*E	4643655	WKA	04/29/2015	Added 35 WLCSP pinout and package detail information. Updated CSD specifications.
*F	5287114	WKA	06/09/2016	Corrected typo in the Features section. Added reference to AN90071 in the More Information section. Updated Flash section with details of flash protection modes. Added notes in the Pinouts section. Updated 40-pin QFN and 28-pin SSOP pin diagrams. Added PSoC 4 Power Supply diagram. Updated the Bypass Capacitors column in the Power Supply table. Updated values for SID32, SID34, SID38, SID269, SID270, SID271. Added SID299A. Updated Comparator Specifications. Updated TCPWM Specifications. Updated values for SID149, SID160, SID171. Updated Conditions for SID190. Added BID55. Removed Conditions for SID237. Added reference to PSoC 4 CAB Libraries with Schematics Symbols and PCB Footprints in the Packaging section.
*G	5327384	WKA	06/28/2016	Removed the capacitor connection for Pin 15 in Figure 11.
*H	5704046	GNKK	04/26/2017	Updated the Cypress logo and copyright information.

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