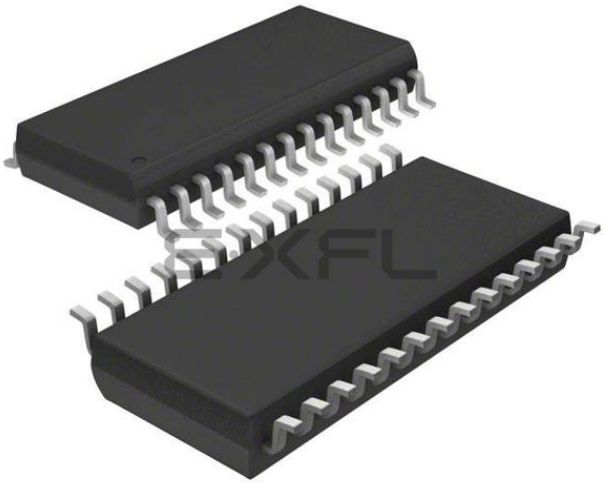

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	24MHz
Connectivity	I²C, IrDA, LINbus, Microwire, SmartCard, SPI, SSP, UART/USART
Peripherals	Brown-out Detect/Reset, CapSense, LCD, LVD, POR, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 8x12b SAR; D/A 2xIDAC
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c4125pvi-482t

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Functional Definition

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in PSoC 4100 is part of the 32-bit MCU subsystem, which is optimized for low power operation with extensive clock gating. It mostly uses 16-bit instructions and executes a subset of the Thumb-2 instruction set. This enables fully compatible binary upward migration of the code to higher performance processors such as the Cortex-M3 and M4, thus enabling upward compatibility. The Cypress implementation includes a hardware multiplier that provides a 32-bit result in one cycle. It includes a nested vectored interrupt controller (NVIC) block with 32 interrupt inputs and also includes a Wakeup Interrupt Controller (WIC), which can wake the processor up from Deep Sleep mode allowing power to be switched off to the main processor when the chip is in Deep Sleep mode. The Cortex-M0 CPU provides a Non-Maskable Interrupt input (NMI), which is made available to the user when it is not in use for system functions requested by the user.

The CPU also includes a debug interface, the serial wire debug (SWD) interface, which is a two-wire form of JTAG; the debug configuration used for PSoC 4100 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

PSoC 4100 has a flash module with a flash accelerator tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver 0 wait-state (WS) access time at 24 MHz. Part of the flash module can be used to emulate EEPROM operation if required.

The PSoC 4200 Flash supports the following flash protection modes at the memory subsystem level:

Open: No Protection. Factory default mode in which the product is shipped.

Protected: User may change from Open to Protected. This mode disables Debug interface accesses. The mode can be set back to Open but only after completely erasing the Flash.

Kill: User may change from Open to Kill. This mode disables all Debug accesses. The part cannot be erased externally, thus obviating the possibility of partial erasure by power interruption and potential malfunction and security leaks. This is an irrecvocable mode.

In addition, row-level Read/Write protection is also supported to prevent inadvertent Writes as well as selectively block Reads. Flash Read/Write/Erase operations are always available for internal code using system calls.

SRAM

SRAM memory is retained during Hibernate.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

System Resources

Power System

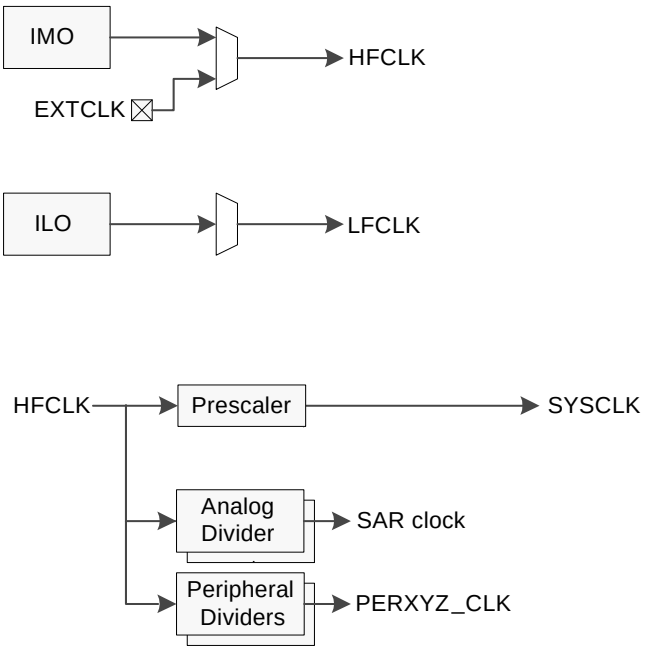
The power system is described in detail in the section Power on page 15. It provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets (brown-out detect (BOD)) or interrupts (low-voltage detect (LVD)). The PSoC 4100 operates with a single external supply over the range of 1.71 V to 5.5 V and has five different power modes, transitions between which are managed by the power system. PSoC 4100 provides Sleep, Deep Sleep, Hibernate, and Stop low-power modes.

Clock System

The PSoC 4100 clock system is responsible for providing clocks to all subsystems that require clocks and for switching between different clock sources without glitching. In addition, the clock system ensures that no metastable conditions occur.

The clock system for PSoC 4100 consists of the internal main oscillator (IMO) and the internal low-power oscillator (ILO) and provision for an external clock.

Figure 3. PSoC 4100 MCU Clocking Architecture



The HFCLK signal can be divided down (see PSoC 4100 MCU Clocking Architecture) to generate synchronous clocks for the analog and digital peripherals. There are a total of 12 clock dividers for PSoC 4100, each with 16-bit divide capability. The analog clock leads the digital clocks to allow analog events to occur before digital clock-related noise is generated. The 16-bit capability allows a lot of flexibility in generating fine-grained frequency values and is fully supported in PSoC Creator.

IMO Clock Source

The IMO is the primary source of internal clocking in the PSoC 4100. It is trimmed during testing to achieve the specified accuracy. Trim values are stored in nonvolatile latches (NVL). Additional trim settings from flash can be used to compensate for changes. The IMO default frequency is 24 MHz and it can be adjusted between 3 MHz to 24 MHz in steps of 1 MHz. The IMO tolerance with Cypress-provided calibration settings is –2%.

ILO Clock Source

The ILO is a very low power oscillator, which is primarily used to generate clocks for peripheral operation in Deep Sleep mode. ILO-driven counters can be calibrated to the IMO to improve accuracy. Cypress provides a software component, which does the calibration.

Watchdog Timer

A watchdog timer is implemented in the clock block running from the ILO; this allows watchdog operation during Deep Sleep and generates a watchdog reset if not serviced before the timeout occurs. The watchdog reset is recorded in the Reset Cause register.

Reset

PSoC 4100 can be reset from a variety of sources including a software reset. Reset events are asynchronous and guarantee reversion to a known state. The reset cause is recorded in a register, which is sticky through reset and allows software to determine the cause of the reset. An XRES pin is reserved for external reset to avoid complications with configuration and multiple pin functions during power-on or reconfiguration. The XRES pin has an internal pull-up resistor that is always enabled.

Voltage Reference

The PSoC 4100 reference system generates all internally required references. A 1% voltage reference spec is provided for the 12-bit ADC. To allow better signal to noise ratios (SNR) and better absolute accuracy, it is possible to bypass the internal reference using a GPIO pin or to use an external reference for the SAR.

Analog Blocks

12-bit SAR ADC

The 12-bit 806 ksps SAR ADC can operate at a maximum clock rate of 14.5 MHz and requires a minimum of 18 clocks at that frequency to do a 12-bit conversion.

The block functionality is augmented for the user by adding a reference buffer to it (trimmable to –1%) and by providing the choice (for the PSoC 4100 case) of three internal voltage references: V_{DD}, $V_{DD}/2$, and V_{REF} (nominally 1.024 V) as well as an external reference through a GPIO pin. The sample-and-hold (S/H) aperture is programmable allowing the gain bandwidth requirements of the amplifier driving the SAR inputs, which determine its settling time, to be relaxed if required. System performance will be 65 dB for true 12-bit precision providing appropriate references are used and system noise levels permit. To improve performance in noisy conditions, it is possible to provide an external bypass (through a fixed pin location) for the internal reference amplifier.

The SAR is connected to a fixed set of pins through an 8-input sequencer. The sequencer cycles through selected channels autonomously (sequencer scan) and does so with zero switching overhead (that is, aggregate sampling bandwidth is equal to 806 ksps whether it is for a single channel or distributed over several channels). The sequencer switching is effected through a state machine or through firmware driven switching. A feature provided by the sequencer is buffering of each channel to reduce CPU interrupt service requirements. To accommodate signals with varying source impedance and frequency, it is possible to have different sample times programmable for each channel. Also, signal range specification through a pair of range registers (low and high range values) is implemented with a corresponding out-of-range interrupt if the digitized value exceeds the programmed range; this allows fast detection of out-of-range values without the necessity of having to wait for a sequencer scan to be completed and the CPU to read the values and check for out-of-range values in software.

The SAR is able to digitize the output of the on-board temperature sensor for calibration and other temperature-dependent functions. The SAR is not available in Deep Sleep and Hibernate modes as it requires a high-speed clock (up to 18 MHz). The SAR operating range is 1.71 V to 5.5 V.

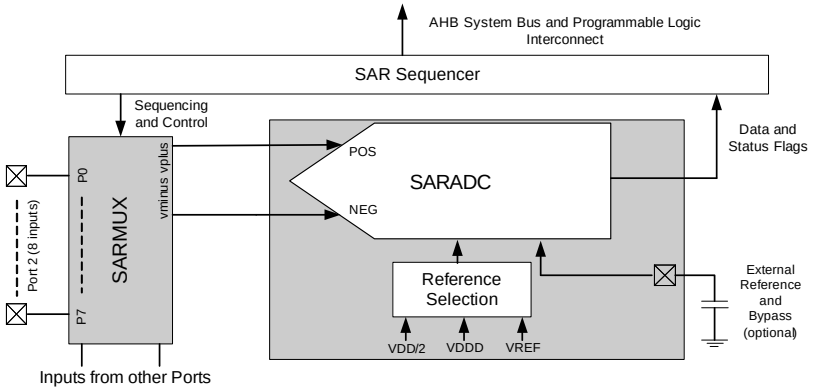



Figure 4. SAR ADC System Diagram