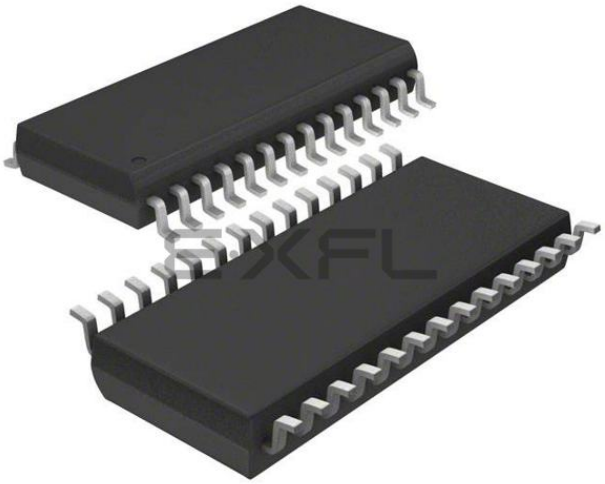

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	M8C
Core Size	8-Bit
Speed	12MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	24
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.25V
Data Converters	A/D 12x14b; D/A 4x9b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c29466-12pvxe

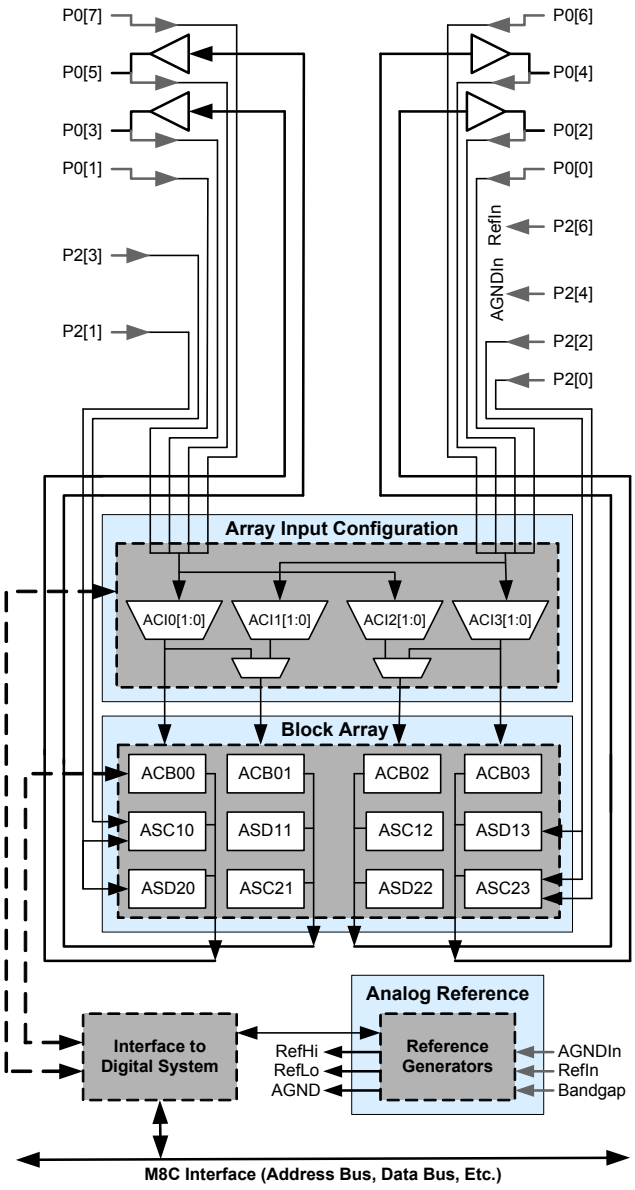
The Analog System

The Analog System is composed of 12 configurable blocks, each comprised of an opamp circuit allowing the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the common PSoC analog functions for this device (most available as user modules) are as follows:

- ADCs (up to 4, with 6- to 14-bit resolution, selectable as Incremental, Delta-Sigma, and SAR)
- Filters (2, 4, 6, or 8 pole band-pass, low-pass, and notch)
- Amplifiers (up to 4, with selectable gain up to 48x)
- Instrumentation amplifiers (up to 2, with selectable gain up to 93x)
- Comparators (up to 4, with 16 selectable thresholds)
- DACs (up to 4, with 6- to 9-bit resolution)
- Multiplying DACs (up to 4, with 6- to 9-bit resolution)
- High current output drivers (four with 30 mA drive as a PSoC Core resource)
- 1.3 V reference (as a System Resource)
- DTMF Dialer
- Correlators
- Peak Detectors
- Many other topologies possible

Analog blocks are provided in columns of three, which includes one Continuous Time (CT) and two Switched Capacitor (SC) blocks, as shown in Figure 2.

Figure 2. Analog System Block Diagram



Additional System Resources

System Resources, some of which have been previously listed, provide additional capability useful for complete systems. Additional resources include a multiplier, decimator, low voltage detection, and power on reset. Brief statements describing the merits of each system resource are given below:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- Two multiply accumulates (MACs) provide fast 8-bit multiplier with 32-bit accumulate to assist in both general math as well as digital filters.
- The decimator provides a custom hardware filter for digital signal processing applications including the creation of Delta Sigma ADCs.
- The I^2C module provides 0 to 400 kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced POR (Power On Reset) circuit eliminates the need for a system supervisor.
- An internal 1.3 V voltage reference provides an absolute reference for the analog system, including ADCs and DACs.

PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have a varying number of digital and analog blocks. The following table lists the resources available for specific PSoC device groups. The PSoC device covered by this data sheet is highlighted in Table 1.

Table 1. PSoC Device Characteristics

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size
CY8C29x66[2]	up to 64	4	16	12	4	4	12	2K	32K
CY8C27x43	up to 44	2	8	12	4	4	12	256 Bytes	16K
CY8C24x94	64	1	4	48	2	2	6	1K	16K
CY8C24x23A[2]	up to 24	1	4	12	2	2	6	256 Bytes	4K
CY8C23x33	up to	1	4	12	2	2	4	256 Bytes	8K
CY8C21x34[2]	up to 28	1	4	28	0	2	4[3]	512 Bytes	8K
CY8C21x23	16	1	4	8	0	2	4[3]	256 Bytes	4K
CY8C20x34	up to 28	0	0	28	0	0	3[3, 4]	512 Bytes	8K

Notes
2. Automotive qualified devices available in this group.
3. Limited analog functionality.
4. Two analog blocks and one CapSense.

Getting Started

For in-depth information, along with detailed programming details, see the *PSoC® Technical Reference Manual*.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These user module datasheets explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations, and external signals.

Pinouts

The automotive CY8C29x66 PSoC device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, Vss, Vdd, and XRES are not capable of Digital I/O.

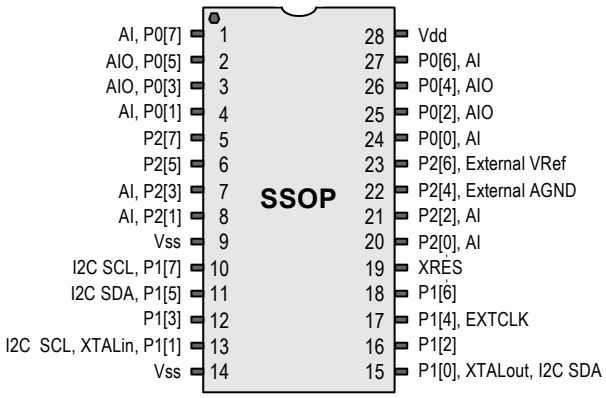
28-pin Part Pinout

Table 2. 28-Pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input.
2	I/O	I/O	P0[5]	Analog column mux input and column output.
3	I/O	I/O	P0[3]	Analog column mux input and column output.
4	I/O	I	P0[1]	Analog column mux input.
5	I/O		P2[7]	
6	I/O		P2[5]	
7	I/O	I	P2[3]	Direct switched capacitor block input.
8	I/O	I	P2[1]	Direct switched capacitor block input.
9	Power		Vss	Ground connection.
10	I/O		P1[7]	I^2C Serial Clock (SCL).
11	I/O		P1[5]	I^2C Serial Data (SDA).
12	I/O		P1[3]	
13	I/O		P1[1]	Crystal Input (XTALin), I^2C Serial Clock (SCL), ISSP-SCLK[5].
14	Power		Vss	Ground connection.
15	I/O		P1[0]	Crystal Output (XTALout), I^2C Serial Data (SDA), ISSP-SDATA[5].
16	I/O		P1[2]	
17	I/O		P1[4]	Optional External Clock Input (EXTCLK).
18	I/O		P1[6]	
19	Input		XRES	Active high external reset with internal pull down.
20	I/O	I	P2[0]	Direct switched capacitor block input.
21	I/O	I	P2[2]	Direct switched capacitor block input.
22	I/O		P2[4]	External Analog Ground (AGND).
23	I/O		P2[6]	External Voltage Reference (VRef).
24	I/O	I	P0[0]	Analog column mux input.
25	I/O	I/O	P0[2]	Analog column mux input and column output.
26	I/O	I/O	P0[4]	Analog column mux input and column output.
27	I/O	I	P0[6]	Analog column mux input.
28	Power		Vdd	Supply voltage.

LEGEND: A = Analog, I = Input, and O = Output.

Figure 3. CY8C29466 28-pin PSoC Device



Note
5. These are the ISSP pins, which are not High Z when coming out of POR (Power On Reset). See the *PSoC Technical Reference Manual* for details.

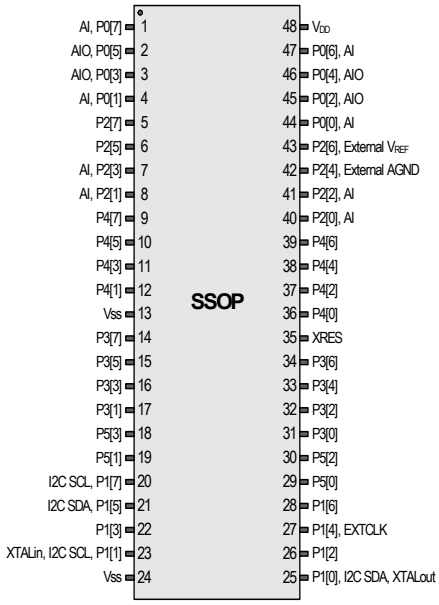
48-pin Part Pinout

Table 3. 48-pin Part Pinout (SSOP)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input
2	I/O	I/O	P0[5]	Analog column mux input and column output
3	I/O	I/O	P0[3]	Analog column mux input and column output
4	I/O	I	P0[1]	Analog column mux input
5	I/O		P2[7]	
6	I/O		P2[5]	
7	I/O	I	P2[3]	Direct switched capacitor block input
8	I/O	I	P2[1]	Direct switched capacitor block input
9	I/O		P4[7]	
10	I/O		P4[5]	
11	I/O		P4[3]	
12	I/O		P4[1]	
13	Power		V_{SS}	Ground connection
14	I/O		P3[7]	
15	I/O		P3[5]	
16	I/O		P3[3]	
17	I/O		P3[1]	
18	I/O		P5[3]	
19	I/O		P5[1]	
20	I/O		P1[7]	I^2C serial clock (SCL)
21	I/O		P1[5]	I^2C serial data (SDA)
22	I/O		P1[3]	
23	I/O		P1[1]	Crystal input (XTALin), I^2C serial clock (SCL), ISSP-SCLK[6]
24	Power		V_{SS}	Ground connection
25	I/O		P1[0]	Crystal output (XTALout), I^2C Serial Data (SDA), ISSP-SDATA[6]
26	I/O		P1[2]	
27	I/O		P1[4]	Optional external clock (EXTCLK) input
28	I/O		P1[6]	
29	I/O		P5[0]	
30	I/O		P5[2]	
31	I/O		P3[0]	
32	I/O		P3[2]	
33	I/O		P3[4]	
34	I/O		P3[6]	
35	Input		XRES	Active high external reset with internal pull-down
36	I/O		P4[0]	
37	I/O		P4[2]	
38	I/O		P4[4]	
39	I/O		P4[6]	
40	I/O	I	P2[0]	Direct switched capacitor block input
41	I/O	I	P2[2]	Direct switched capacitor block input
42	I/O		P2[4]	External analog ground (AGND)
43	I/O		P2[6]	External voltage reference (V_{REF})
44	I/O	I	P0[0]	Analog column mux input
45	I/O	I/O	P0[2]	Analog column mux input and column output
46	I/O	I/O	P0[4]	Analog column mux input and column output
47	I/O	I	P0[6]	Analog column mux input
48	Power		V_{DD}	Supply voltage

LEGEND: A = Analog, I = Input, and O = Output.

Figure 4. CY8C29666 48-pin PSoC Device



Note
6. These are the ISSP pins, which are not high Z when coming out of POR. See the *PSoC Technical Reference Manual* for details.

Registers

Register Conventions

This section lists the the registers of the automotive CY8C29x66 PSoC device. For detailed register information, reference the *PSoC Technical Reference Manual.*

The register conventions specific to this section are listed in the following table.

Table 4. Abbreviations

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks. The XIO bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XIO bit is set the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and should not be accessed.

Table 6. Register Map Bank 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW	DBB20FN	40	RW	ASC10CR0	80	RW	RDI2RI	C0	RW
PRT0DM1	01	RW	DBB20IN	41	RW	ASC10CR1	81	RW	RDI2SYN	C1	RW
PRT0IC0	02	RW	DBB20OU	42	RW	ASC10CR2	82	RW	RDI2IS	C2	RW
PRT0IC1	03	RW		43		ASC10CR3	83	RW	RDI2LT0	C3	RW
PRT1DM0	04	RW	DBB21FN	44	RW	ASD11CR0	84	RW	RDI2LT1	C4	RW
PRT1DM1	05	RW	DBB21IN	45	RW	ASD11CR1	85	RW	RDI2RO0	C5	RW
PRT1IC0	06	RW	DBB21OU	46	RW	ASD11CR2	86	RW	RDI2RO1	C6	RW
PRT1IC1	07	RW		47		ASD11CR3	87	RW		C7	
PRT2DM0	08	RW	DCB22FN	48	RW	ASC12CR0	88	RW	RDI3RI	C8	RW
PRT2DM1	09	RW	DCB22IN	49	RW	ASC12CR1	89	RW	RDI3SYN	C9	RW
PRT2IC0	0A	RW	DCB22OU	4A	RW	ASC12CR2	8A	RW	RDI3IS	CA	RW
PRT2IC1	0B	RW		4B		ASC12CR3	8B	RW	RDI3LT0	CB	RW
PRT3DM0	0C	RW	DCB23FN	4C	RW	ASD13CR0	8C	RW	RDI3LT1	CC	RW
PRT3DM1	0D	RW	DCB23IN	4D	RW	ASD13CR1	8D	RW	RDI3RO0	CD	RW
PRT3IC0	0E	RW	DCB23OU	4E	RW	ASD13CR2	8E	RW	RDI3RO1	CE	RW
PRT3IC1	0F	RW		4F		ASD13CR3	8F	RW		CF	
PRT4DM0	10	RW	DBB30FN	50	RW	ASD20CR0	90	RW	GDI_O_IN	D0	RW
PRT4DM1	11	RW	DBB30IN	51	RW	ASD20CR1	91	RW	GDI_E_IN	D1	RW
PRT4IC0	12	RW	DBB30OU	52	RW	ASD20CR2	92	RW	GDI_O_OU	D2	RW
PRT4IC1	13	RW		53		ASD20CR3	93	RW	GDI_E_OU	D3	RW
PRT5DM0	14	RW	DBB31FN	54	RW	ASC21CR0	94	RW		D4	
PRT5DM1	15	RW	DBB31IN	55	RW	ASC21CR1	95	RW		D5	
PRT5IC0	16	RW	DBB31OU	56	RW	ASC21CR2	96	RW		D6	
PRT5IC1	17	RW		57		ASC21CR3	97	RW		D7	
	18		DCB32FN	58	RW	ASD22CR0	98	RW		D8	
	19		DCB32IN	59	RW	ASD22CR1	99	RW		D9	
	1A		DCB32OU	5A	RW	ASD22CR2	9A	RW		DA	
	1B			5B		ASD22CR3	9B	RW		DB	
	1C		DCB33FN	5C	RW	ASC23CR0	9C	RW		DC	
	1D		DCB33IN	5D	RW	ASC23CR1	9D	RW	OSC_GO_EN	DD	RW
	1E		DCB33OU	5E	RW	ASC23CR2	9E	RW	OSC_CR4	DE	RW
	1F			5F		ASC23CR3	9F	RW	OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW		64			A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5			E5	
DBB01OU	26	RW	AMD_CR1	66	RW		A6			E6	
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW	ALT_CR1	68	RW		A8		IMO_TR	E8	W
DCB02IN	29	RW	CLK_CR2	69	RW		A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B			6B			AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
DBB10FN	30	RW	ACB00CR3	70	RW	RDI0RI	B0	RW		F0	
DBB10IN	31	RW	ACB00CR0	71	RW	RDI0SYN	B1	RW		F1	
DBB10OU	32	RW	ACB00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACB00CR2	73	RW	RDI0LT0	B3	RW		F3	
DBB11FN	34	RW	ACB01CR3	74	RW	RDI0LT1	B4	RW		F4	
DBB11IN	35	RW	ACB01CR0	75	RW	RDI0RO0	B5	RW		F5	
DBB11OU	36	RW	ACB01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACB01CR2	77	RW		B7		CPU_F	F7	RL
DCB12FN	38	RW	ACB02CR3	78	RW	RDI1RI	B8	RW		F8	
DCB12IN	39	RW	ACB02CR0	79	RW	RDI1SYN	B9	RW		F9	
DCB12OU	3A	RW	ACB02CR1	7A	RW	RDI1IS	BA	RW	FLS_PR1	FA	RW
	3B		ACB02CR2	7B	RW	RDI1LT0	BB	RW		FB	
DCB13FN	3C	RW	ACB03CR3	7C	RW	RDI1LT1	BC	RW		FC	
DCB13IN	3D	RW	ACB03CR0	7D	RW	RDI1RO0	BD	RW		FD	
DCB13OU	3E	RW	ACB03CR1	7E	RW	RDI1RO1	BE	RW	CPU_SCR1	FE	#
	3F		ACB03CR2	7F	RW		BF		CPU_SCR0	FF	#

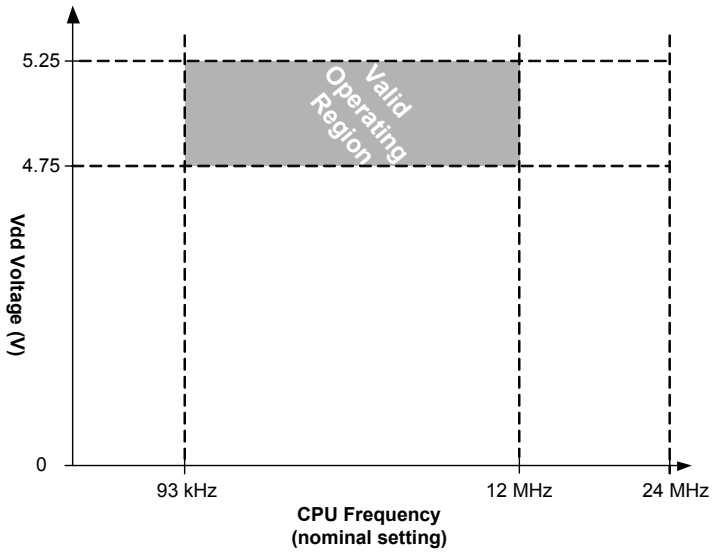
Blank fields are Reserved and should not be accessed. # Access is bit specific.

Electrical Specifications

This section presents the DC and AC electrical specifications of the automotive CY8C29x66 PSoC device. For the most up to date electrical specifications, confirm that you have the most recent data sheet by visiting http://www.cypress.com.

Specifications are valid for –40 °C ≤ T_A ≤ 125 °C and T_J ≤ 135 °C, except where noted.

Figure 5. Voltage versus CPU Frequency



DC Electrical Characteristics

DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 125 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 9. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
Vdd	Supply Voltage	4.75	–	5.25	V	
I_{DD}	Supply Current	–	8	15	mA	Conditions are –40 °C ≤ T_A ≤ 125 °C, CPU=3 MHz, 48 MHz disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz. Analog power = off.
I_{SB}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT.[7]	–	6	16	µA	Conditions are with internal low speed oscillator active, –40 °C ≤ T_A ≤ 55 °C. Analog power = off.
I_{SBH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, and WDT at high temperature[7]	–	6	100	µA	Conditions are with internal low speed oscillator active, 55 °C < T_A ≤ 125 °C. Analog power = off.
I_{SBXTL}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal.[7]	–	8	18	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. –40 °C ≤ T_A ≤ 55 °C. Analog power = off.
I_{SBXTLH}	Sleep (Mode) Current with POR, LVD, Sleep Timer, WDT, and external crystal at high temperature.[7]	–	8	100	µA	Conditions are with properly loaded, 1 µW max, 32.768 kHz crystal. 55 °C < T_A ≤ 125 °C. Analog power = off.
V_{REF}	Reference Voltage (Bandgap)	1.25	1.3	1.35	V	

Note
7. Standby current includes all functions (POR, LVD, WDT, Sleep Timer) needed for reliable system operation. This must be compared with devices that have similar functions enabled.

DC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 125 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 10. DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull up Resistor	4	5.6	8	kΩ	
R_{PD}	Pull down Resistor	4	5.6	8	kΩ	
V_{OH}	High Output Level	3.5	–	–	V	I_{OH} = 10 mA, Vdd = 4.75 to 5.25 V (maximum 40 mA on even port pins (for example, P0[2], P1[4]), maximum 40 mA on odd port pins (for example, P0[3], P1[5])). 80 mA maximum combined I_{OH} budget.
V_{OL}	Low Output Level	–	–	0.75	V	I_{OL} = 25 mA, Vdd = 4.75 to 5.25 V (maximum 100 mA on even port pins (for example, P0[2], P1[4]), maximum 100 mA on odd port pins (for example, P0[3], P1[5])). 150 mA maximum combined I_{OL} budget.
I_{OH}	High Level Source Current	10	–	–	mA	V_{OH} ≥ Vdd–1.0 V, see the limitations of the total current in the note for V_{OH}
I_{OL}	Low Level Sink Current	25	–	–	mA	V_{OL} ≤ 0.75 V, see the limitations of the total current in the note for V_{OL}
V_{IL}	Input Low Level	–	–	0.8	V	
V_{IH}	Input High Level	2.1	–		V	
V_H	Input Hysterisis	–	60	–	mV	
I_{IL}	Input Leakage (Absolute Value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive Load on Pins as Input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.
C_{OUT}	Capacitive Load on Pins as Output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.

DC Low Power Comparator Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 125 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 12. DC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{REFLPC}	Low power comparator (LPC) reference voltage range	0.2	–	Vdd – 1	V	
I_{SLPC}	LPC supply current	–	10	40	µA	
V_{OSLPC}	LPC voltage offset	–	2.5	30	mV	

DC Analog Output Buffer Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 125 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 13. DC Analog Output Buffer Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOB}	Input Offset Voltage (Absolute Value)	–	3	18	mV	
TCV_{OSOB}	Input Offset Voltage Drift	–	+6	–	µV/°C	
V_{CMOB}	Common-Mode Input Voltage Range	0.5	–	Vdd – 1.0	V	
R_{OUTOB}	Output Resistance	–	1	–	W	
$V_{OHIGHOB}$	High Output Voltage Swing (Load = 32Ω to Vdd/2)	0.5 x Vdd + 1.1	–	–	V	
V_{OLOWOB}	Low Output Voltage Swing (Load = 32Ω to Vdd/2)	–	–	0.5 x Vdd – 1.3	V	
I_{SOB}	Supply Current Including Bias Cell (No Load) Power = Low Power = High	 – –	 1.1 2.6	 5.1 8.8	 mA mA	
$PSRR_{OB}$	Supply Voltage Rejection Ratio	–	64	–	dB	

DC Analog Reference Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 125 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

The guaranteed specifications for RefHI and RefLO are measured through the analog continuous time PSoC blocks. The power levels for RefHI and RefLO refer to the analog reference control register. AGND is measured at P2[4] in AGND bypass mode. Each analog continuous time PSoC block adds a maximum of 10 mV additional offset error to guaranteed AGND specifications from the local AGND buffer. Reference control power can be set to medium or high unless otherwise noted.

Note Avoid using P2[4] for digital signaling when using an analog resource that depends on the Analog Reference. Some coupling of the digital signal may appear on the AGND.

Table 14. DC Analog Reference Specifications

Symbol	Description	Min	Typ	Max	Units
V_{BG}	Bandgap Voltage Reference	1.25	1.30	1.35	V
–	AGND = Vdd/2[8]	Vdd/2 – 0.02	Vdd/2	Vdd/2 + 0.02	V
–	AGND = 2 x BandGap[8]	2.4	2.6	2.8	V
–	AGND = P2[4] (P2[4] = Vdd/2)[8]	P2[4] – 0.02	P2[4]	P2[4] + 0.02	V
–	AGND = BandGap[8]	1.23	1.3	1.37	V
–	AGND = 1.6 x BandGap[8]	1.98	2.08	2.14	V
–	AGND Column to Column Variation (AGND=Vdd/2)[8]	0.035	0.000	0.035	V
–	RefHi = Vdd/2 + BandGap[9]	Vdd/2 + 1.15	Vdd/2 + 1.30	Vdd/2 + 1.45	V
–	RefHi = 3 x BandGap[9]	3.65	3.9	4.15	V
–	RefHi = 2 x BandGap + P2[6] (P2[6] = 1.3 V)[9]	P2[6] + 2.4	P2[6] + 2.6	P2[6] + 2.8	V
–	RefHi = P2[4] + BandGap (P2[4] = Vdd/2)[9]	P2[4] + 1.24	P2[4] + 1.30	P2[4] + 1.36	V
–	RefHi = P2[4] + P2[6] (P2[4] = Vdd/2, P2[6] = 1.3 V)[9]	P2[4] + P2[6] – 0.1	P2[4] + P2[6]	P2[4] + P2[6] + 0.1	V
–	RefHi = 2 x BandGap[9]	2.4	2.6	2.8	V
–	RefHi = 3.2 x BandGap[9]	3.9	4.16	4.42	V
–	RefLo = Vdd/2 - BandGap[9]	Vdd/2 – 1.45	Vdd/2 – 1.3	Vdd/2 – 1.15	V
–	RefLo = BandGap[9]	1.15	1.30	1.45	V
–	RefLo = 2 x BandGap – P2[6] (P2[6] = 1.3 V)[9]	2.4 – P2[6]	2.6 – P2[6]	2.8 – P2[6]	V
–	RefLo = P2[4] - BandGap (P2[4] = Vdd/2)[9]	P2[4] – 1.45	P2[4] – 1.3	P2[4] – 1.15	V
–	RefLo = P2[4] – P2[6] (P2[4] = Vdd/2, P2[6] = 1.3 V)[9]	P2[4] – P2[6] – 0.1	P2[4] – P2[6]	P2[4] – P2[6] + 0.1	V

DC Analog PSoC Block Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 125 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 15. DC Analog PSoC Block Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{CT}	Resistor Unit Value (Continuous Time)	–	12.24	–	kΩ	
C_{SC}	Capacitor Unit Value (Switch Cap)	–	80	–	fF	

Notes
8. This specification is only valid when CT Block Power = High. AGND tolerance includes the offsets of the local buffer in the PSoC block.
9. This specification is only valid when Ref Control Power = High.

AC Electrical Characteristics

AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 125 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

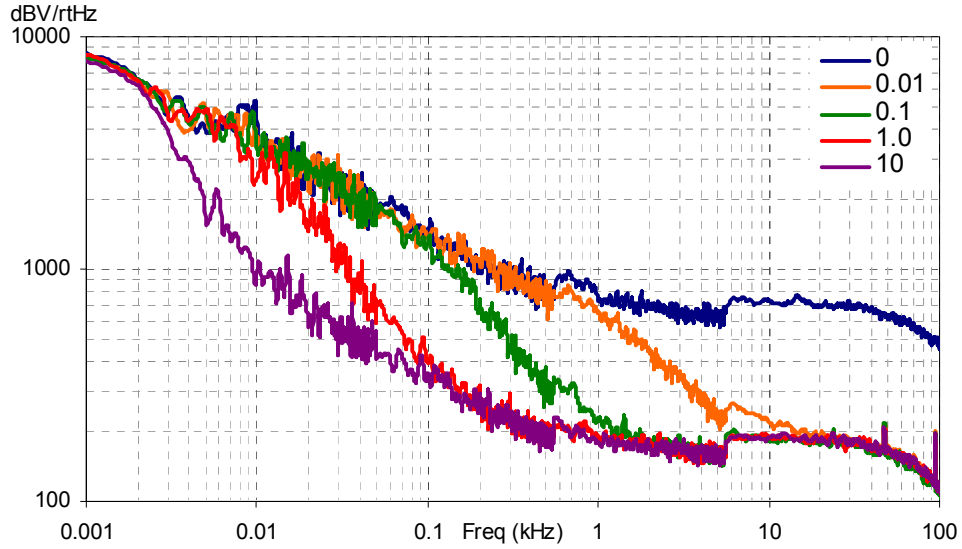
Table 18. AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO24}	Internal Main Oscillator Frequency for 24 MHz	23.04[13]	24	24.96[13]	MHz	Trimmed. Utilizing factory trim values.
F_{CPU1}	CPU Frequency (5 V Vdd Nominal)	0.09[13]	12	12.48[13]	MHz	
F_{24M}	Digital PSoC Block Frequency	0	24	24.96[14, 13]	MHz	
F_{32K1}	Internal Low Speed Oscillator Frequency	15	32	64	kHz	This specification applies when the ILO has been trimmed.
F_{32KU}	Internal Low Speed Oscillator (ILO) Untrimmed Frequency	5	–	–	kHz	After a reset and before the M8C processor starts to execute, the ILO is not trimmed.
F_{32K2}	External Crystal Oscillator	–	32.768	–	kHz	Accuracy is capacitor and crystal dependent. 50% duty cycle.
F_{PLL}	PLL Frequency	–	23.986	–	MHz	Is a multiple (x732) of crystal frequency.
Jitter24M2	24 MHz Period Jitter (PLL)	–	–	800	ps	
$T_{PLLSLEW}$	PLL Lock Time	0.5	–	10	ms	Refer to Figure 6 on page 23.
$T_{PLLSLEWSLOW}$	PLL Lock Time for Low Gain Setting	0.5	–	50	ms	Refer to Figure 7 on page 23.
T_{OS}	External Crystal Oscillator Startup to 1%	–	1700	2620	ms	Refer to Figure 8 on page 23.
T_{OSACC}	External Crystal Oscillator Startup to 200 ppm	–	2800	3800	ms	
Jitter32k	32 kHz Period Jitter	–	100	–	ns	Refer to Figure 10 on page 23.
T_{XRST}	External Reset Pulse Width	10	–	–	µs	
DC24M	24 MHz Duty Cycle	40	50	60	%	
DC_{ILO}	Internal Low Speed Oscillator (ILO) Duty Cycle	20	50	80	%	
Step24M	24 MHz Trim Step Size	–	50	–	kHz	
Jitter24M1P	24 MHz Period Jitter (IMO) Peak-to-Peak	–	600	–	ps	Refer to Figure 9 on page 23.
Jitter24M1R	24 MHz Period Jitter (IMO) Root Mean Squared	–	–	600	ps	Refer to Figure 9 on page 23.
F_{MAX}	Maximum frequency of signal on row input or row output.	–	–	12.48[13]	MHz	
$SR_{POWERUP}$	Power Supply Slew Rate	–	–	250	V/ms	Vdd slew rate during power up.
$T_{POWERUP}$	Time between end of POR state and CPU code execution	–	16	100	ms	Power up from 0 V.

Notes
13. Accuracy derived from Internal Main Oscillator with appropriate trim for Vdd range.
14. See the individual user module data sheets for information on maximum frequencies for user modules.

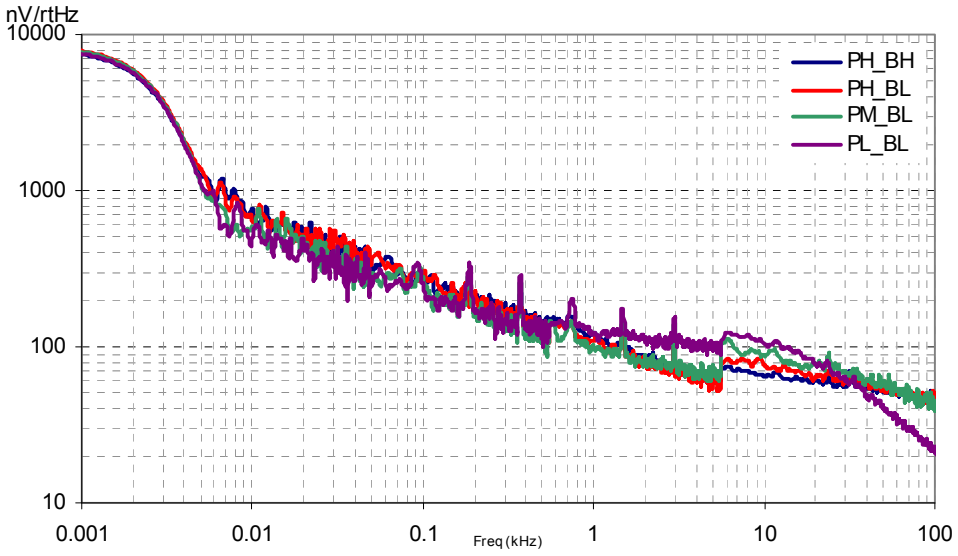
When bypassed by a capacitor on P2[4], the noise of the analog ground signal distributed to each block is reduced by a factor of up to 5 (14 dB). This is at frequencies above the corner frequency defined by the on-chip 8.1 kΩ resistance and the external capacitor.

Figure 12. Typical AGND Noise with P2[4] Bypass



At low frequencies, the opamp noise is proportional to 1/f, power independent, and determined by device geometry. At high frequencies, increased power level reduces the noise spectrum level.

Figure 13. Typical Opamp Noise



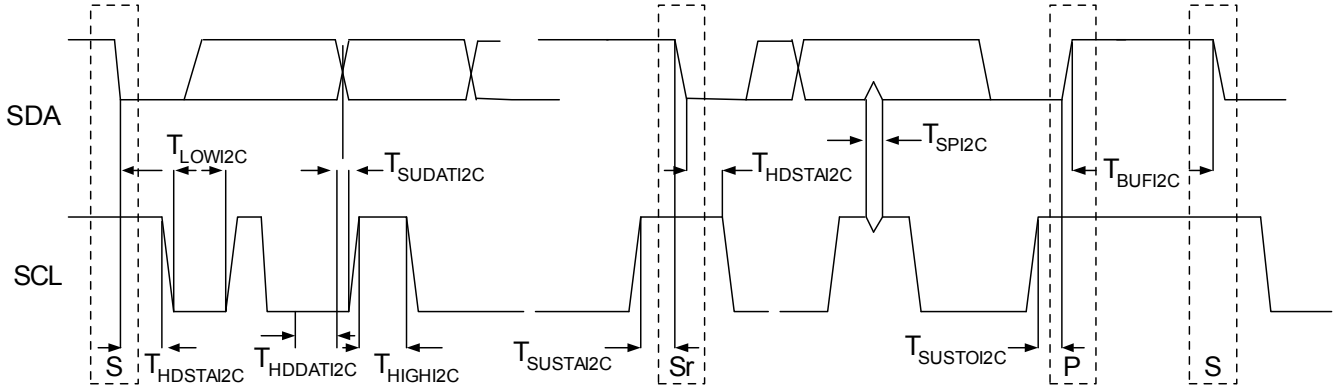
AC I²C Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 125 °C. Typical parameters apply to 5 V at 25 °C and are for design guidance only.

Table 26. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL Clock Frequency	0	100[16]	0	400[16]	kHz	
$T_{HDSTAI2C}$	Hold Time (repeated) START Condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW Period of the SCL Clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH Period of the SCL Clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Set Up Time for a Repeated START Condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data Set Up Time	250	–	100[17]	–	ns	
$T_{SUSTOI2C}$	Set-up Time for STOP Condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	Bus Free Time Between a STOP and START Condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse Width of spikes are suppressed by the input filter.	–	–	0	50	ns	

Figure 14. Definition for Timing for Fast/Standard Mode on the I²C Bus



Notes

16. F_{SCLI2C} is derived from SysClk of the PSoC. This specification assumes that SysClk is operating at 24 MHz, nominal. If SysClk is at a lower frequency, then the F_{SCLI2C} specification adjusts accordingly.
17. A Fast-Mode I²C-bus device can be used in a Standard-Mode I²C-bus system, but the requirement $T_{SUDATI2C} \geq 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + T_{SUDATI2C} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

Development Tool Selection

This section presents the development tools available for the CY8C29x66 family.

Software

PSoC Designer

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for years. PSoC Designer is available free of charge at http://www.cypress.com. PSoC Designer comes with a free C compiler.

PSoC Programmer

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at http://www.cypress.com.

Development Kits

All development kits can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

CY3215-DK Basic Development Kit

The CY3215-DK is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface allows users to run, halt, and single step the processor and view the contents of specific memory locations. Advanced emulation features are also supported through PSoC Designer. The kit includes:

- ICE-Cube Unit
- 28-pin PDIP Emulation Pod for CY8C29466-24PXI
- 28-pin CY8C29466-24PXI PDIP PSoC Device Samples (two)
- PSoC Designer Software CD
- ISSP Cable
- MiniEval Socket Programming and Evaluation board
- Backward Compatibility Cable (for connecting to legacy Pods)
- Universal 110/220 Power Supply (12 V)
- European Plug Adapter
- USB 2.0 Cable
- Getting Started Guide
- Development Kit Registration form

Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store. The online store also has the most up to date information on kit contents, descriptions, and availability.

CY3210-PSoCEval1

The CY3210-PSoCEval1 kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, an RS-232 port, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-pin CY8C29466-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

CY3210-29X66 Evaluation Pod (EvalPod)

PSoC EvalPods are pods that connect to the ICE In-Circuit Emulator (CY3215-DK kit) to allow debugging capability. They can also function as a standalone device without debugging capability. The EvalPod has a 28-pin DIP footprint on the bottom for easy connection to development kits or other hardware. The top of the EvalPod has prototyping headers for easy connection to the device's pins. CY3210-29X66 provides evaluation of the CY8C29x66 PSoC device family.

Device Programmers

All device programmers can be purchased from the Cypress Online Store.

CY3210-MiniProg1

The CY3210-MiniProg1 kit allows a user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-pin CY8C29466-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

Reference Information

Acronyms Used

The following table lists the acronyms that are used in this document.

Table 32. Acronyms

Acronym	Description	Acronym	Description
AC	alternating current	IMO	internal main oscillator
ADC	analog-to-digital converter	I/O	input/output
API	application programming interface	IPOR	imprecise power on reset
CPU	central processing unit	LSb	least-significant bit
CT	continuous time	LVD	low voltage detect
DAC	digital-to-analog converter	MSb	most-significant bit
DC	direct current	PC	program counter
ECO	external crystal oscillator	PLL	phase-locked loop
EEPROM	electrically erasable programmable read-only memory	POR	power on reset
FSR	full scale range	PPOR	precision power on reset
GPIO	general purpose IO	PSoC	Programmable System-on-Chip
GUI	graphical user interface	PWM	pulse width modulator
HBM	human body model	SC	switched capacitor
ICE	in-circuit emulator	SRAM	static random access memory
ILO	internal low speed oscillator		

Units of Measure

The following table lists the units of measure that are used in this section.

Table 33. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µVrms	microvolts root-mean-square
dB	decibels	µW	microwatt
fF	femto farad	mA	milliampere
Hz	hertz	ms	millisecond
KB	1024 bytes	mV	millivolt
Kbit	1024 bits	nA	nanoampere
kHz	kilohertz	ns	nanosecond
kΩ	kilohm	nV	nanovolt
Mbaud	megabaud	Ω	ohm
Mbps	megabits per second	pA	picoampere
MHz	megahertz	pF	picofarad
MΩ	megaohm	pp	peak-to-peak
µA	microampere	ppm	parts per million
µF	microfarad	ps	picosecond
µH	microhenry	sps	samples per second
µs	microsecond	σ	sigma: one standard deviation
µV	microvolt	V	volt

Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, ‘01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’, ‘b’, or ‘0x’ are decimal.

Document History Page

Document Title: CY8C29466, CY8C29666, Automotive – Extended Temperature PSoC® Programmable System-on-Chip Document Number: 38-12026				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	228771	06/01/2004	SFV	First release of the CY8C29x66 automotive PSoC device data sheet.
*A	271452	See ECN	HMT	Update per SFV memo. Input changes from MWR, including removing SMP.
*B	288029	See ECN	HMT	Add Reflow Peak Temp. table. Update PSoC Characteristics table. Update characterization data.
*C	473829	See ECN	HMT	Update PSoC Characteristics table. Update characterization data. Update Storage Temperature for extended temperature devices. Fix error in Register Bank 0/1. Update CY color, logo and copyright.
*D	602219	See ECN	HMT	Add Low Power Comparator (LPC) AC/DC electrical spec. tables. Add CY8C20x34 to PSoC Device Characteristics table. Update Technical Training Modules paragraph. Add ISSP note to pinout tables.
*E	2101387	See ECN	AESA	Post to www.cypress.com
*F	2545030	07/29/08	YARA	Added note to DC Analog Reference Specification table and Ordering Information
*G	2663861	02/24/09	PRKA / AESA	Updated template Removed CY8C29666-12PVXE and CY8C29666-12PVXET and related package information Updated PSoC Designer and Getting Started sections
*H	2756235	08/26/09	BTK/AESA	Changed title. Updated Features section. Updated text of PSoC Functional Overview section. Updated Getting Started section. Made corrections and minor text edits to Pinouts section. Changed the name of some sections for added clarity. Improved formatting of the register tables. Added clarifying comments to some electrical specifications. Changed T_{RAMP} specification per MASJ input. Fixed all AC specifications to conform to a ±4% IMO accuracy. Made other miscellaneous minor text edits. Deleted some non-applicable or redundant information. Added a footnote to clarify that 8 of the 12 analog inputs are regular and the other 4 are direct SC block connections. Added Development Tool Selection section. Improved the bookmark structure. Changed the T_{ROB}, T_{SOB}, V_{IHP}, $V_{OHIGHOB}$, V_{OSOB}, V_{OSOA}, C_{INOA}, $V_{OHIGHOA}$, V_{OLOWOA}, I_{SOA}, Jitter24M1P, TRiseF, and DC POR and LVD specifications according to MASJ directives.
*I	2822792	12/07/2009	BTK/AESA	Added T_{PRGH}, T_{PRGC}, I_{OL}, I_{OH}, F_{32KU}, DC_{ILO}, and $T_{POWERUP}$ electrical specifications. Updated the text of footnote 10. Added maximum values and updated typical values for T_{ERASEB} and T_{WRITE} electrical specifications. Replaced T_{RAMP} electrical specification with $SR_{POWERUP}$ electrical specification. Added "Contents" on page 2. This revision fixes CDT 63984.
*J	2888007	03/30/2010	NJF	Updated Cypress website links. Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters in Absolute Maximum Ratings Updated Packaging Information. Updated Development Kits and Evaluation Tools. Removed Third Party Tools and Build a PSoC Emulator into your Board. Updated Ordering Code Definitions. Updated links in Sales, Solutions, and Legal Information.
*K	3440253	11/16/2011	MYKT_UKR	Added part number CY8C29666-12PVXE to the Ordering Information table. Added 48-pin part information to Pinouts, Thermal Impedances, and Capacitance on Crystal Pins sections. Updated Accessories (Emulation and Programming) section. Updated Solder Reflow Specifications section. Included 48-Pin (300-Mil) SSOP spec to Packaging Information section.
*L	3537225	02/28/2011	VIVG	No technical updates.

Document Title: CY8C29466, CY8C29666, Automotive – Extended Temperature PSoC® Programmable System-on-Chip Document Number: 38-12026				
*M	3726340	08/28/2012	tess_ukr/ LURE	Updated the following sections: Getting Started, Development Tools, and Designing with PSoC Designer as all the System level designs have been de-emphasized. Changed the PWM description string from “8- to 32-bit” to “8- and 16-bit”.
*N	4689330	03/16/2015	KUK	Updated Electrical Specifications: Updated DC Electrical Characteristics: Updated DC Analog Reference Specifications: Updated description. Updated Packaging Information: spec 51-85079 – Changed revision from *E to *F. spec 51-85061 – Changed revision from *E to *F. Updated to new template. Completing Sunset Review.

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