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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	4MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at90s8515-4ac

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	one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.
	The AT90S8515 provides the following features: 8K bytes of In-System Programmable Flash, 512 bytes EEPROM, 512 bytes SRAM, 32 general-purpose I/O lines, 32 general-purpose working registers, flexible timer/counters with compare modes, internal and external interrupts, a programmable serial UART, programmable Watchdog Timer with internal oscillator, an SPI serial port and two software-selectable power-saving modes. The Idle Mode stops the CPU while allowing the SRAM, timer/counters, SPI port and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.
	The device is manufactured using Atmel's high-density nonvolatile memory technology. The On-chip In-System Programmable Flash allows the program memory to be repro- grammed In-System through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining an enhanced RISC 8-bit CPU with In-System Pro- grammable Flash on a monolithic chip, the Atmel AT90S8515 is a powerful microcontroller that provides a highly flexible and cost-effective solution to many embed- ded control applications.
	The AT90S8515 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators and evaluation kits.
Pin Descriptions	
vcc	Supply voltage.
GND	Ground.
Port A (PA7PA0)	Port A is an 8-bit bi-directional I/O port. Port pins can provide internal pull-up resistors (selected for each bit). The Port A output buffers can sink 20 mA and can drive LED displays directly. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not active.
	Port A serves as multiplexed address/data input/output when using external SRAM.
Port B (PB7PB0)	Port B is an 8-bit bi-directional I/O port with internal pull-up resistors. The Port B output buffers can sink 20 mA. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not active.
	Port B also serves the functions of various special features of the AT90S8515 as listed on page 66.
Port C (PC7PC0)	Port C is an 8-bit bi-directional I/O port with internal pull-up resistors. The Port C output buffers can sink 20 mA. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not active.
	Port C also serves as address output when using external SRAM.
Port D (PD7PD0)	Port D is an 8-bit bi-directional I/O port with internal pull-up resistors. The Port D output

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Architectural Overview

The fast-access register file concept contains 32×8 -bit general-purpose working registers with a single clock cycle access time. This means that during one single clock cycle, one ALU (Arithmetic Logic Unit) operation is executed. Two operands are output from the register file, the operation is executed and the result is stored back in the register file – in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing, enabling efficient address calculations. One of the three address pointers is also used as the address pointer for the constant table look-up function. These added function registers are the 16-bit X-, Y-, and Z-register.

The ALU supports arithmetic and logic functions between registers or between a constant and a register. Single register operations are also executed in the ALU. Figure 4 shows the AT90S8515 AVR RISC microcontroller architecture.

In addition to the register operation, the conventional memory addressing modes can be used on the register file as well. This is enabled by the fact that the register file is assigned the 32 lowermost Data Space addresses (\$00 - \$1F), allowing them to be accessed as though they were ordinary memory locations.

The I/O memory space contains 64 addresses for CPU peripheral functions such as Control Registers, Timer/Counters, A/D converters and other I/O functions. The I/O memory can be accessed directly or as the Data Space locations following those of the register file, \$20 - \$5F.

The AVR uses a Harvard architecture concept – with separate memories and buses for program and data. The program memory is executed with a two-stage pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is In-System Programmable Flash memory.

With the relative jump and call instructions, the whole 4K address space is directly accessed. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

During interrupts and subroutine calls, the return address Program Counter (PC) is stored on the stack. The stack is effectively allocated in the general data SRAM and consequently, the stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the reset routine (before subroutines or interrupts are executed). The 16-bit Stack Pointer (SP) is read/write-accessible in the I/O space.

The 512-byte data SRAM can be easily accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.









A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the status register. All the different interrupts have a separate interrupt vector in the interrupt vector table at the beginning of the program memory. The different interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.

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In the different addressing modes these address registers have functions as fixed dis-
placement, automatic increment and decrement (see the descriptions for the different
instructions).

ALU – Arithmetic Logic Unit The high-performance AVR ALU operates in direct connection with all the 32 generalpurpose working registers. Within a single clock cycle, ALU operations between registers in the register file are executed. The ALU operations are divided into three main categories: arithmetic, logical and bit functions.

In-System Programmable Flash Program Memory Flash Program Memory i The AT90S8515 contains 8K bytes On-chip In-System Programmable Flash memory for program storage. Since all instructions are 16- or 32-bit words, the Flash is organized as 4K x 16. The Flash memory has an endurance of at least 1000 write/erase cycles. The AT90S8515 Program Counter (PC) is 12 bits wide, thus addressing the 4096 program memory addresses.

See page 86 for a detailed description of Flash data downloading.

See page 13 for the different program memory addressing modes.



• Bit 6 – INTF0: External Interrupt Flag0

When an edge on the INT0 pin triggers an interrupt request, the corresponding interrupt flag, INTF0, becomes set (one). If the I-bit in SREG and the corresponding interrupt enable bit, INT0 in GIMSK are set (one), the MCU will jump to the interrupt vector. The flag is cleared when the interrupt routine is executed. Alternatively, the flag is cleared by writing a logical "1" to it. This flag is always cleared when INT0 is configured as level interrupt.

Bits 5..0 – Res: Reserved Bits

These bits are reserved bits in the AT90S8515 and always read as zero.

Timer/Counter Interrupt Mask Register – TIMSK

Bit	7	6	5	4	3	2	1	0	
\$39 (\$59)	TOIE1	OCIE1A	OCIE1B	-	TICIE1	-	TOIE0	-	TIMSK
Read/Write	R/W	R/W	R/W	R	R/W	R	R/W	R	-
Initial Value	0	0	0	0	0	0	0	0	

Bit 7 – TOIE1: Timer/Counter1 Overflow Interrupt Enable

When the TOIE1 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 Overflow interrupt is enabled. The corresponding interrupt (at vector \$006) is executed if an overflow in Timer/Counter1 occurs, i.e., when the TOV1 bit is set in the Timer/Counter Interrupt Flag Register (TIFR).

• Bit 6 – OCE1A: Timer/Counter1 Output CompareA Match Interrupt Enable

When the OCIE1A bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 CompareA Match interrupt is enabled. The corresponding interrupt (at vector \$004) is executed if a CompareA match in Timer/Counter1 occurs, i.e., when the OCF1A bit is set in the Timer/Counter Interrupt Flag Register (TIFR).

• Bit 5 – OCIE1B: Timer/Counter1 Output CompareB Match Interrupt Enable

When the OCIE1B bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 CompareB Match interrupt is enabled. The corresponding interrupt (at vector \$005) is executed if a CompareB match in Timer/Counter1 occurs, i.e., when the OCF1B bit is set in the Timer/Counter Interrupt Flag Register (TIFR).

• Bit 4 – Res: Reserved Bit

This bit is a reserved bit in the AT90S8515 and always reads zero.

• Bit 3 – TICIE1: Timer/Counter1 Input Capture Interrupt Enable

When the TICIE1 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter1 Input Capture Event interrupt is enabled. The corresponding interrupt (at vector \$003) is executed if a capture-triggering event occurs on pin 31, ICP, i.e., when the ICF1 bit is set in the Timer/Counter Interrupt Flag Register (TIFR).

• Bit 2 - Res: Reserved Bit

This bit is a reserved bit in the AT90S8515 and always reads zero.

• Bit 1 – TOIE0: Timer/Counter0 Overflow Interrupt Enable

When the TOIE0 bit is set (one) and the I-bit in the Status Register is set (one), the Timer/Counter0 Overflow interrupt is enabled. The corresponding interrupt (at vector \$007) is executed if an overflow in Timer/Counter0 occurs, i.e., when the TOV0 bit is set in the Timer/Counter Interrupt Flag Register (TIFR).

• Bit 0 - Res: Reserved Bit

This bit is a reserved bit in the AT90S8515 and always reads zero.





• Bit 5 – SE: Sleep Enable

The SE bit must be set (one) to make the MCU enter the Sleep Mode when the SLEEP instruction is executed. To avoid the MCU entering the Sleep Mode, unless it is the programmer's purpose, it is recommended to set the Sleep Enable (SE) bit just before the execution of the SLEEP instruction.

• Bit 4 – SM: Sleep Mode

This bit selects between the two available sleep modes. When SM is cleared (zero), Idle Mode is selected as Sleep Mode. When SM is set (one), Power-down mode is selected as Sleep Mode. For details, refer to the section "Sleep Modes".

• Bits 3, 2 – ISC11, ISC10: Interrupt Sense Control 1, Bit 1 and Bit 0

The External Interrupt 1 is activated by the external pin INT1 if the SREG I-flag and the corresponding interrupt mask in the GIMSK are set. The level and edges on the external INT1 pin that activate the interrupt are defined in Table 5.

Table 5. Interrupt 1 Sense Control

ISC11	ISC10	Description
0	0	The low level of INT1 generates an interrupt request.
0	1	Reserved
1	0	The falling edge of INT1 generates an interrupt request.
1	1	The rising edge of INT1 generates an interrupt request.

• Bits 1, 0 – ISC01, ISC00: Interrupt Sense Control 0, Bit 1 and Bit 0

The External Interrupt 0 is activated by the external pin INT0 if the SREG I-flag and the corresponding interrupt mask are set. The level and edges on the external INT0 pin that activate the interrupt are defined in Table 6.

Table 6. Interrupt 0 Sense Control

ISC01	ISC00	Description
0	0	The low level of INT0 generates an interrupt request.
0	1	Reserved
1	0	The falling edge of INT0 generates an interrupt request.
1	1	The rising edge of INT0 generates an interrupt request.

The value on the INTn pin is sampled before detecting edges. If edge interrupt is selected, pulses with a duration longer than one CPU clock period will generate an interrupt. Shorter pulses are not guaranteed to generate an interrupt. If low-level interrupt is selected, the low level must be held until the completion of the currently executing instruction to generate an interrupt. If enabled, a level-triggered interrupt will generate an interrupt request as long as the pin is held low.

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The Stop condition provides a Timer Enable/Disable function. The CK down divided modes are scaled directly from the CK oscillator clock. If the external pin modes are used for Timer/Counter0, transitions on PB0/(T0) will clock the counter even if the pin is configured as an output. This feature can give the user software control of the counting.

Timer Counter0 – TCNT0



The Timer/Counter0 is realized as an up-counter with read and write access. If the Timer/Counter0 is written and a clock source is present, the Timer/Counter0 continues counting in the clock cycle following the write operation.

16-bit Timer/Counter1

Figure 30 shows the block diagram for Timer/Counter1.

Figure 30. Timer/Counter1 Block Diagram



The 16-bit Timer/Counter1 can select clock source from CK, prescaled CK or an external pin. In addition, it can be stopped as described in the specification for the Timer/Counter1 Control Registers (TCCR1A and TCCR1B). The different status flags (overflow, compare match and capture event) are found in the Timer/Counter Interrupt Flag Register (TIFR). Control signals are found in the Timer/Counter1 Control Registers

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Prevent EEPROM Corruption

During periods of low V_{CC}, the EEPROM data can be corrupted because the supply voltage is too low for the CPU and the EEPROM to operate properly. These issues are the same as for board level systems using the EEPROM and the same design solutions should be applied.

An EEPROM data corruption can be caused by two situations when the voltage is too low. First, a regular write sequence to the EEPROM requires a minimum voltage to operate correctly. Second, the CPU itself can execute instructions incorrectly if the supply voltage for executing instructions is too low.

EEPROM data corruption can easily be avoided by following these design recommendations (one is sufficient):

- Keep the AVR RESET active (low) during periods of insufficient power supply voltage. This is best done by an external low V_{CC} Reset Protection circuit, often referred to as a Brown-out Detector (BOD). Please refer to application note AVR 180 for design considerations regarding power-on reset and low-voltage detection.
- Keep the AVR core in Power-down Sleep mode during periods of low V_{CC}. This will prevent the CPU from attempting to decode and execute instructions, effectively protecting the EEPROM registers from unintentional writes.
- 3. Store constants in Flash memory if the ability to change memory contents from software is not required. Flash memory cannot be updated by the CPU and will not be subject to corruption.

Serial Peripheral Interface – SPI

The Serial Peripheral Interface (SPI) allows high-speed synchronous data transfer between the AT90S8515 and peripheral devices or between several AVR devices. The AT90S8515 SPI features include the following:

- Full-duplex, 3-wire Synchronous Data Transfer
- Master or Slave Operation
- LSB First or MSB First Data Transfer
- Four Programmable Bit Rates
- End-of-Transmission Interrupt Flag
- Write Collision Flag Protection
- Wake-up from Idle Mode (Slave Mode Only)

Figure 34. SPI Block Diagram



The interconnection between master and slave CPUs with SPI is shown in Figure 35. The PB7(SCK) pin is the clock output in the Master Mode and is the clock input in the Slave Mode. Writing to the SPI Data Register of the master CPU starts the SPI clock generator and the data written shifts out of the PB5(MOSI) pin and into the PB5(MOSI) pin of the slave CPU. After shifting one byte, the SPI clock generator stops, setting the end-of-transmission flag (SPIF). If the SPI interrupt enable bit (SPIE) in the SPCR register is set, an interrupt is requested. The Slave Select input, PB4(SS), is set low to select an individual slave SPI device. The two shift registers in the master and the slave can be considered as one distributed 16-bit circular shift register. This is shown in Figure 35. When data is shifted from the master to the slave, data is also shifted in the opposite direction, simultaneously. This means that during one shift cycle, data in the master and the slave are interchanged.



pins are inputs. When \overline{SS} is driven high, all pins are inputs and the SPI is passive, which means that it will not receive incoming data. Note that the SPI logic will be reset once the \overline{SS} pin is brought high. If the \overline{SS} pin is brought high during a transmission, the SPI will stop sending and receiving immediately and both data received and data sent must be considered as lost.

Data Modes

There are four combinations of SCK phase and polarity with respect to serial data, which are determined by control bits CPHA and CPOL. The SPI data transfer formats are shown in Figure 36 and Figure 37.





* Not defined but normally MSB of character just received





* Not defined but normally LSB of previously transmitted character

SPI Control Register – SPCR

Bit	7	6	5	4	3	2	1	0	_
\$0D (\$2D)	SPIE	SPE	DORD	MSTR	CPOL	CPHA	SPR1	SPR0	SPCR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	-
Initial Value	0	0	0	0	0	0	0	0	

• Bit 7 – SPIE: SPI Interrupt Enable

This bit causes the SPI interrupt to be executed if SPIF bit in the SPSR register is set and the global interrupts are enabled.

Bit 6 – SPE: SPI Enable

When the SPE bit is set (one), the SPI is enabled. This bit must be set to enable any SPI operations.





The FE bit is cleared when the stop bit of received data is one.

Bit 3 – OR: Overrun

This bit is set if an Overrun condition is detected, i.e., when a character already present in the UDR register is not read before the next character has been shifted into the Receiver Shift register. The OR bit is buffered, which means that it will be set once the valid data still in UDRE is read.

The OR bit is cleared (zero) when data is received and transferred to UDR.

• Bits 2..0 – Res: Reserved Bits

These bits are reserved bits in the AT90S8515 and will always read as zero.

UART Control Register – UCR

Bit	7	6	5	4	3	2	1	0	
\$0A (\$2A)	RXCIE	TXCIE	UDRIE	RXEN	TXEN	CHR9	RXB8	TXB8	UCR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R	W	•
Initial Value	0	0	0	0	0	0	1	0	

Bit 7 – RXCIE: RX Complete Interrupt Enable

When this bit is set (one), a setting of the RXC bit in USR will cause the Receive Complete Interrupt routine to be executed provided that global interrupts are enabled.

• Bit 6 – TXCIE: TX Complete Interrupt Enable

When this bit is set (one), a setting of the TXC bit in USR will cause the Transmit Complete Interrupt routine to be executed provided that global interrupts are enabled.

• Bit 5 – UDRIE: UART Data Register Empty Interrupt Enable

When this bit is set (one), a setting of the UDRE bit in USR will cause the UART Data Register Empty Interrupt routine to be executed provided that global interrupts are enabled.

Bit 4 – RXEN: Receiver Enable

This bit enables the UART receiver when set (one). When the receiver is disabled, the RXC, OR and FE status flags cannot become set. If these flags are set, turning off RXEN does not cause them to be cleared.

• Bit 3 – TXEN: Transmitter Enable

This bit enables the UART transmitter when set (one). When disabling the transmitter while transmitting a character, the transmitter is not disabled before the character in the shift register plus any following character in UDR has been completely transmitted.

• Bit 2 – CHR9: 9-bit Characters

When this bit is set (one) transmitted and received characters are 9 bits long plus start and stop bits. The ninth bit is read and written by using the RXB8 and TXB8 bits in UCR, respectively. The ninth data bit can be used as an extra stop bit or a parity bit.

• Bit 1 – RXB8: Receive Data Bit 8

When CHR9 is set (one), RXB8 is the ninth data bit of the received character.

• Bit 0 – TXB8: Transmit Data Bit 8

When CHR9 is set (one), TXB8 is the ninth data bit in the character to be transmitted.



Baud Rate	1	MHz	%Error	1.8432	MHz	%Error	2	MHz	%Error	2.4576	MHz	%Error
2400	UBRR=	25	0.2	UBRR=	47	0.0	UBRR=	51	0.2	UBRR=	63	0.0
4800	UBRR=	12	0.2	UBRR=	23	0.0	UBRR=	25	0.2	UBRR=	31	0.0
9600	UBRR=	6	7.5	UBRR=	11	0.0	UBRR=	12	0.2	UBRR=	15	0.0
14400	UBRR=	3	7.8	UBRR=	7	0.0	UBRR=	8	3.7	UBRR=	10	3.1
19200	UBRR=	2	7.8	UBRR=	5	0.0	UBRR=	6	7.5	UBRR=	7	0.0
28800	UBRR=	1	7.8	UBRR=	3	0.0	UBRR=	3	7.8	UBRR=	4	6.3
38400	UBRR=	1	22.9	UBRR=	2	0.0	UBRR=	2	7.8	UBRR=	3	0.0
57600	UBRR=	0	7.8	UBRR=	1	0.0	UBRR=	1	7.8	UBRR=	2	12.5
76800	UBRR=	0	22.9	UBRR=	1	33.3	UBRR=	1	22.9	UBRR=	1	0.0
115200	UBRR=	0	84.3	UBRR=	0	0.0	UBRR=	0	7.8	UBRR=	0	25.0
Baud Rate	3.2768	MHz	%Error	3.6864	MHz	%Error	4	MHz	%Error	4.608	MHz	%Error
2400	UBRR=	84	0.4	UBRR=	95	0.0	UBRR=	103	0.2	UBRR=	119	0.0
4800	UBRR=	42	0.8	UBRR=	47	0.0	UBRR=	51	0.2	UBRR=	59	0.0
9600	UBRR=	20	1.6	UBRR=	23	0.0	UBRR=	25	0.2	UBRR=	29	0.0
14400	UBRR=	13	1.6	UBRR=	15	0.0	UBRR=	16	2.1	UBRR=	19	0.0
19200	UBRR=	10	3.1	UBRR=	11	0.0	UBRR=	12	0.2	UBRR=	14	0.0
28800	UBRR=	6	1.6	UBRR=	7	0.0	UBRR=	8	3.7	UBRR=	9	0.0
38400	UBRR=	4	6.3	UBRR=	5	0.0	UBRR=	6	7.5	UBRR=	7	6.7
57600	UBRR=	3	12.5	UBRR=	3	0.0	UBRR=	3	7.8	UBRR=	4	0.0
76800	UBRR=	2	12.5	UBRR=	2	0.0	UBRR=	2	7.8	UBRR=	3	6.7
115200	UBRR=	1	12.5	UBRR=	1	0.0	UBRR=	1	7.8	UBRR=	2	20.0
												•
Baud Rate	7.3728	MHz	%Error	8	MHz	%Error	9.216	MHz	%Error	11.059	MHz	%Error
2400	UBRR=	191	0.0	UBRR=	207	0.2	UBRR=	239	0.0	UBRR=	287	-
4800	UBRR=	95	0.0	UBRR=	103	0.2	UBRR=	119	0.0	UBRR=	143	0.0
9600	UBRR=	47	0.0	UBRR=	51	0.2	UBRR=	59	0.0	UBRR=	71	0.0
14400	UBRR=	31	0.0	UBRR=	34	0.8	UBRR=	39	0.0	UBRR=	47	0.0
19200	UBRR=	23	0.0	UBRR=	25	0.2	UBRR=	29	0.0	UBRR=	35	0.0
28800	UBRR=	15	0.0	UBRR=	16	2.1	UBRR=	19	0.0	UBRR=	23	0.0
38400	UBRR=	11	0.0	UBRR=	12	0.2	UBRR=	14	0.0	UBRR=	17	0.0
57600	UBRR=	7	0.0	UBRR=	8	3.7	UBRR=	9	0.0	UBRR=	11	0.0
76800	UBRR=	5	0.0	UBRR=	6	7.5	UBRR=	7	6.7	UBRR=	8	0.0
115200	UBRR=	3	0.0	UBRR=	3	7.8	UBRR=	4	0.0	UBRR=	5	0.0

Table 17. UBRR Settings at Various Crystal Frequencies

UART BAUD Rate Register – UBRR



The UBRR register is an 8-bit read/write register that specifies the UART Baud Rate according to the equation on the previous page.



- 1. Set BS to "1". This selects high data.
- 2. Give WR a negative pulse. This starts programming of the data byte. RDY/BSY goes low.
- 3. Wait until RDY/BSY goes high to program the next byte.

(See Figure 62 for signal waveforms.)

The loaded command and address are retained in the device during programming. For efficient programming, the following should be considered:

- The command needs only be loaded once when writing or reading multiple memory locations.
- Address high byte needs only be loaded before programming a new 256-word page in the Flash.
- Skip writing the data value \$FF, that is, the contents of the entire Flash and EEPROM after a Chip Erase.

These considerations also apply to EEPROM programming and Flash, EEPROM and signature byte reading.



Figure 61. Programming the Flash Waveforms

AT90S8515







External Data Memory Timing

			8 MHz Os	scillator	Variable	Oscillator	
	Symbol	Parameter	Min	Max	Min	Max	Unit
0	1/t _{CLCL}	Oscillator Frequency			0.0	8.0	MHz
1	t _{LHLL}	ALE Pulse Width	32.5		0.5 t _{CLCL} - 30.0 ⁽¹⁾		ns
2	t _{AVLL}	Address Valid A to ALE Low	22.5		0.5 t _{CLCL} - 40.0 ⁽¹⁾		ns
3a	t _{LLAX_ST}	Address Hold after ALE Low, ST/STD/STS Instructions	67.5		0.5 t _{CLCL} + 5.0 ⁽²⁾		ns
Зb	t _{LLAX_LD}	Address Hold after ALE Low, LD/LDD/LDS Instructions	15.0		15.0		ns
4	t _{AVLLC}	Address Valid C to ALE Low	22.5		0.5 t _{CLCL} - 40.0 ⁽¹⁾		ns
5	t _{AVRL}	Address Valid to RD Low	95.0		1.0 t _{CLCL} - 30.0		ns
6	t _{AVWL}	Address Valid to WR Low	157.5		1.5 t _{CLCL} - 30.0 ⁽¹⁾		ns
7	t _{LLWL}	ALE Low to WR Low	105.0	145.0	1.0 t _{CLCL} - 20.0	1.0 t _{CLCL} + 20.0	ns
8	t _{LLRL}	ALE Low to RD Low	42.5	82.5	0.5 t _{CLCL} - 20.0 ⁽²⁾	$0.5 t_{CLCL} + 20.0^{(2)}$	ns
9	t _{DVRH}	Data Setup to RD High	60.0		60.0		ns
10	t _{RLDV}	Read Low to Data Valid		70.0		1.0 t _{CLCL} - 55.0	ns
11	t _{RHDX}	Data Hold after RD High	0.0		0.0		ns
12	t _{RLRH}	RD Pulse Width	105.0		1.0 t _{CLCL} - 20.0		ns
13	t _{DVWL}	Data Setup to WR Low	27.5		0.5 t _{CLCL} - 35.0 ⁽²⁾		ns
14	t _{WHDX}	Data Hold after WR High	0.0		0.0		ns
15	t _{DVWH}	Data Valid to WR High	95.0		1.0 t _{CLCL} - 30.0		ns
16	t _{wLWH}	WR Pulse Width	42.5		0.5 t _{CLCL} - 20.0 ⁽¹⁾		ns

	Table 37.	External	Data Memor	v Characteristics.	4.0V -	6.0V. N	lo Wait 🗄	State
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Table 38. External Data Memory Characteristics, 4.0V - 6.0V, One Cycle Wait State

			8 MHz Os	scillator	Variable		
	Symbol	Parameter	Min	Max	Min	Max	Unit
0	1/t _{CLCL}	Oscillator Frequency			0.0	8.0	MHz
10	t _{RLDV}	Read Low to Data Valid		195.0		2.0 t _{CLCL} - 55.0	ns
12	t _{RLRH}	RD Pulse Width	230.0		2.0 t _{CLCL} - 20.0		ns
15	t _{DVWH}	Data Valid to WR High	220.0		2.0 t _{CLCL} - 30.0		ns
16	t _{wLWH}	WR Pulse Width	167.5		1.5 t _{CLCL} - 20.0 ⁽²⁾		ns

Notes: 1. This assumes 50% clock duty cycle. The half-period is actually the high time of the external clock, XTAL1.

2. This assumes 50% clock duty cycle. The half-period is actually the low time of the external clock, XTAL1.



Sink and source capabilities of I/O ports are measured on one pin at a time.













Figure 84. I/O Pin Source Current vs. Output Voltage









AT90S8515 Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
4	2.7V - 6.0V	AT90S8515-4AC	44A	Commercial
		AT90S8515-4JC	44J	(0°C to 70°C)
		AT90S8515-4PC	40P6	
		AT90S8515-4AI	44A	Industrial
		AT90S8515-4JI	44J	(-40°C to 85°C)
		AT90S8515-4PI	40P6	
8	4.0V - 6.0V	AT90S8515-8AC	44A	Commercial
		AT90S8515-8JC	44J	(0°C to 70°C)
		AT90S8515-8PC	40P6	
		AT90S8515-8AI	44A	Industrial
		AT90S8515-8JI	44J	(-40°C to 85°C)
		AT90S8515-8PI	40P6	

Note: Order AT90S8515A-XXX for devices with the FSTRT Fuse programmed.

Package Type			
44 A	44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flat Package (TQFP)		
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)		
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)		

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40P6

40-lead, Plastic Dual Inline Parkage (PDIP), 0.600" wide Demension in Millimeters and (Inches)* JEDEC STANDARD MS-011 AC



*Controlling dimension: Inches







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