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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	AVR
Core Size	8-Bit
Speed	4MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	32
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	512 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/at90s8515-4ai">https://www.e-xfl.com/product-detail/microchip-technology/at90s8515-4ai</a>



one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The AT90S8515 provides the following features: 8K bytes of In-System Programmable Flash, 512 bytes EEPROM, 512 bytes SRAM, 32 general-purpose I/O lines, 32 general-purpose working registers, flexible timer/counters with compare modes, internal and external interrupts, a programmable serial UART, programmable Watchdog Timer with internal oscillator, an SPI serial port and two software-selectable power-saving modes. The Idle Mode stops the CPU while allowing the SRAM, timer/counters, SPI port and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The On-chip In-System Programmable Flash allows the program memory to be reprogrammed In-System through an SPI serial interface or by a conventional nonvolatile memory programmer. By combining an enhanced RISC 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT90S8515 is a powerful microcontroller that provides a highly flexible and cost-effective solution to many embedded control applications.

The AT90S8515 AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators and evaluation kits.

## Pin Descriptions

<b>VCC</b>	Supply voltage.
<b>GND</b>	Ground.
<b>Port A (PA7..PA0)</b>	<p>Port A is an 8-bit bi-directional I/O port. Port pins can provide internal pull-up resistors (selected for each bit). The Port A output buffers can sink 20 mA and can drive LED displays directly. When pins PA0 to PA7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not active.</p> <p>Port A serves as multiplexed address/data input/output when using external SRAM.</p>
<b>Port B (PB7..PB0)</b>	<p>Port B is an 8-bit bi-directional I/O port with internal pull-up resistors. The Port B output buffers can sink 20 mA. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not active.</p> <p>Port B also serves the functions of various special features of the AT90S8515 as listed on page 66.</p>
<b>Port C (PC7..PC0)</b>	<p>Port C is an 8-bit bi-directional I/O port with internal pull-up resistors. The Port C output buffers can sink 20 mA. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not active.</p> <p>Port C also serves as address output when using external SRAM.</p>
<b>Port D (PD7..PD0)</b>	<p>Port D is an 8-bit bi-directional I/O port with internal pull-up resistors. The Port D output buffers can sink 20 mA. As inputs, Port D pins that are externally pulled low will source</p>

into T by the BST instruction and a bit in T can be copied into a bit in a register in the register file by the BLD instruction.

- **Bit 5 – H: Half-carry Flag**

The half-carry flag H indicates a half-carry in some arithmetic operations. See the Instruction Set description for detailed information.

- **Bit 4 – S: Sign Bit,  $S = N \oplus V$**

The S-bit is always an exclusive or between the negative flag N and the two's complement overflow flag V. See the Instruction Set description for detailed information.

- **Bit 3 – V: Two's Complement Overflow Flag**

The two's complement overflow flag V supports two's complement arithmetics. See the Instruction Set description for detailed information.

- **Bit 2 – N: Negative Flag**

The negative flag N indicates a negative result after the different arithmetic and logic operations. See the Instruction Set description for detailed information.

- **Bit 1 – Z: Zero Flag**

The zero flag Z indicates a zero result after the different arithmetic and logic operations. See the Instruction Set description for detailed information.

- **Bit 0 – C: Carry Flag**

The carry flag C indicates a carry in an arithmetic or logic operation. See the Instruction Set description for detailed information.

Note that the Status Register is not automatically stored when entering an interrupt routine and restored when returning from an interrupt routine. This must be handled by software.

## Stack Pointer – SP

The general AVR 16-bit Stack Pointer is effectively built up of two 8-bit registers in the I/O space locations \$3E (\$5E) and \$3D (\$5D). As the AT90S8515 supports up to 64 Kb external SRAM, all 16 bits are used.

Bit	15	14	13	12	11	10	9	8	
\$3E (\$5E)	<b>SP15</b>	<b>SP14</b>	<b>SP13</b>	<b>SP12</b>	<b>SP11</b>	<b>SP10</b>	<b>SP9</b>	<b>SP8</b>	<b>SPH</b>
\$3D (\$5D)	<b>SP7</b>	<b>SP6</b>	<b>SP5</b>	<b>SP4</b>	<b>SP3</b>	<b>SP2</b>	<b>SP1</b>	<b>SP0</b>	<b>SPL</b>
	7	6	5	4	3	2	1	0	
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	
	0	0	0	0	0	0	0	0	

The Stack Pointer points to the data SRAM stack area where the Subroutine and Interrupt stacks are located. This stack space in the data SRAM must be defined by the program before any subroutine calls are executed or interrupts are enabled. The Stack Pointer must be set to point above \$60. The Stack Pointer is decremented by 1 when data is pushed onto the stack with the PUSH instruction and it is decremented by 2 when an address is pushed onto the stack with subroutine calls and interrupts. The Stack Pointer is incremented by 1 when data is popped from the stack with the POP instruction and it is incremented by 2 when an address is popped from the stack with return from subroutine RET or return from interrupt RETI.

## Reset and Interrupt Handling

The AT90S8515 provides 12 different interrupt sources. These interrupts and the separate reset vector each have a separate program vector in the program memory space. All interrupts are assigned individual enable bits that must be set (one) together with the I-bit in the Status Register in order to enable the interrupt.

The lowest addresses in the program memory space are automatically defined as the Reset and Interrupt vectors. The complete list of vectors is shown in Table 2. The list also determines the priority levels of the different interrupts. The lower the address, the higher the priority level. RESET has the highest priority, and next is INT0 (the External Interrupt Request 0), etc.

**Table 2.** Reset and Interrupt Vectors

Vector No.	Program Address	Source	Interrupt Definition
1	\$000	RESET	External Reset, Power-on Reset and Watchdog Reset
2	\$001	INT0	External Interrupt Request 0
3	\$002	INT1	External Interrupt Request 1
4	\$003	TIMER1 CAPT	Timer/Counter1 Capture Event
5	\$004	TIMER1 COMPA	Timer/Counter1 Compare Match A
6	\$005	TIMER1 COMPB	Timer/Counter1 Compare Match B
7	\$006	TIMER1 OVF	Timer/Counter1 Overflow
8	\$007	TIMER0, OVF	Timer/Counter0 Overflow
9	\$008	SPI, STC	Serial Transfer Complete
10	\$009	UART, RX	UART, Rx Complete
11	\$00A	UART, UDRE	UART Data Register Empty
12	\$00B	UART, TX	UART, Tx Complete
13	\$00C	ANA_COMP	Analog Comparator

The most typical and general program setup for the Reset and Interrupt vector addresses are:

Address	Labels	Code	Comments
\$000		rjmp RESET	; Reset Handler
\$001		rjmp EXT_INT0	; IRQ0 Handler
\$002		rjmp EXT_INT1	; IRQ1 Handler
\$003		rjmp TIM1_CAPT	; Timer1 Capture Handler
\$004		rjmp TIM1_COMPA	; Timer1 CompareA Handler
\$005		rjmp TIM1_COMPB	; Timer1 CompareB Handler
\$006		rjmp TIM1_OVF	; Timer1 Overflow Handler
\$007		rjmp TIM0_OVF	; Timer0 Overflow Handler
\$008		rjmp SPI_STC	; SPI Transfer Complete Handler
\$009		rjmp UART_RXC	; UART RX Complete Handler
\$00a		rjmp UART_DRE	; UDR Empty Handler
\$00b		rjmp UART_TXC	; UART TX Complete Handler
\$00c		rjmp ANA_COMP	; Analog Comparator Handler
			;
\$00d	MAIN:	ldi r16,high(RAMEND);	Main program start
\$00e		out SPH,r16	

The user can select the start-up time according to typical oscillator start-up. The number of WDT oscillator cycles used for each time-out is shown in Table 4. The frequency of the Watchdog Oscillator is voltage-dependent as shown in “Typical Characteristics” on page 95.

**Table 4.** Number of Watchdog Oscillator Cycles

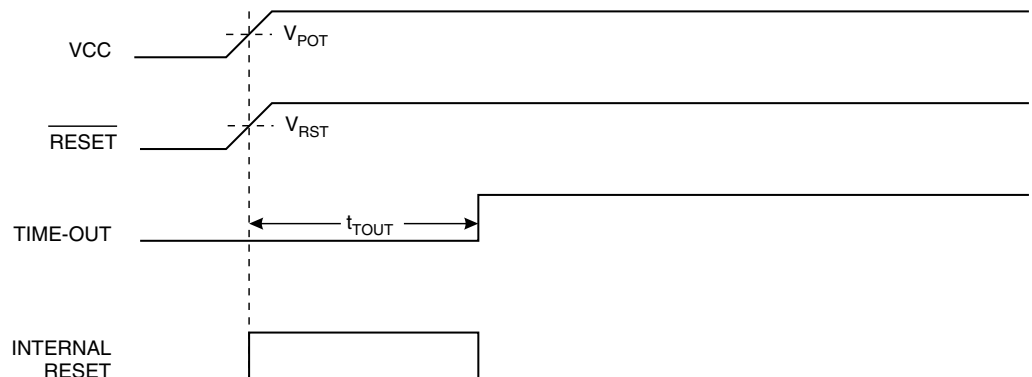
FSTRT	Time-out at $V_{CC} = 5V$	Number of WDT Cycles
Programmed	0.28 ms	256
Unprogrammed	16.0 ms	16K

## Power-on Reset

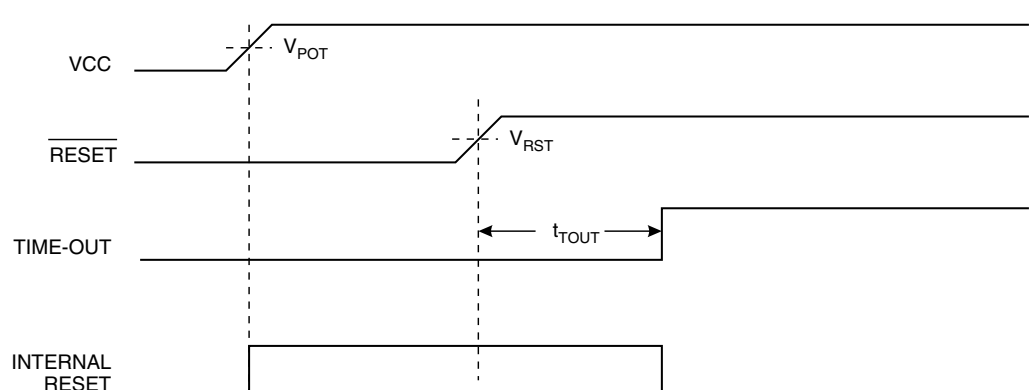
A Power-on Reset (POR) circuit ensures that the device is reset from power-on. As shown in Figure 23, an internal timer clocked from the Watchdog Timer oscillator prevents the MCU from starting until after a certain period after  $V_{CC}$  has reached the Power-on Threshold Voltage ( $V_{POT}$ ), regardless of the  $V_{CC}$  rise time (see Figure 24). The FSTRT Fuse bit in the Flash can be programmed to give a shorter start-up time if a ceramic resonator or any other fast-start oscillator is used to clock the MCU.

If the built-in start-up delay is sufficient,  $\overline{RESET}$  can be connected to  $V_{CC}$  directly or via an external pull-up resistor. By holding the pin low for a period after  $V_{CC}$  has been applied, the Power-on Reset period can be extended. Refer to Figure 25 for a timing example of this.

**Figure 24.** MCU Start-up,  $\overline{RESET}$  Tied to  $V_{CC}$ .



**Figure 25.** MCU Start-up,  $\overline{RESET}$  Controlled Externally



The AT90S8515 provides two general-purpose Timer/Counters – one 8-bit T/C and one 16-bit T/C. The Timer/Counters have individual prescaling selection from the same 10-bit prescaling timer. Both Timer/Counters can either be used as a timer with an internal clock time base or as a counter with an external pin connection that triggers the counting.

Figure 28 shows the general Timer/Counter prescaler.

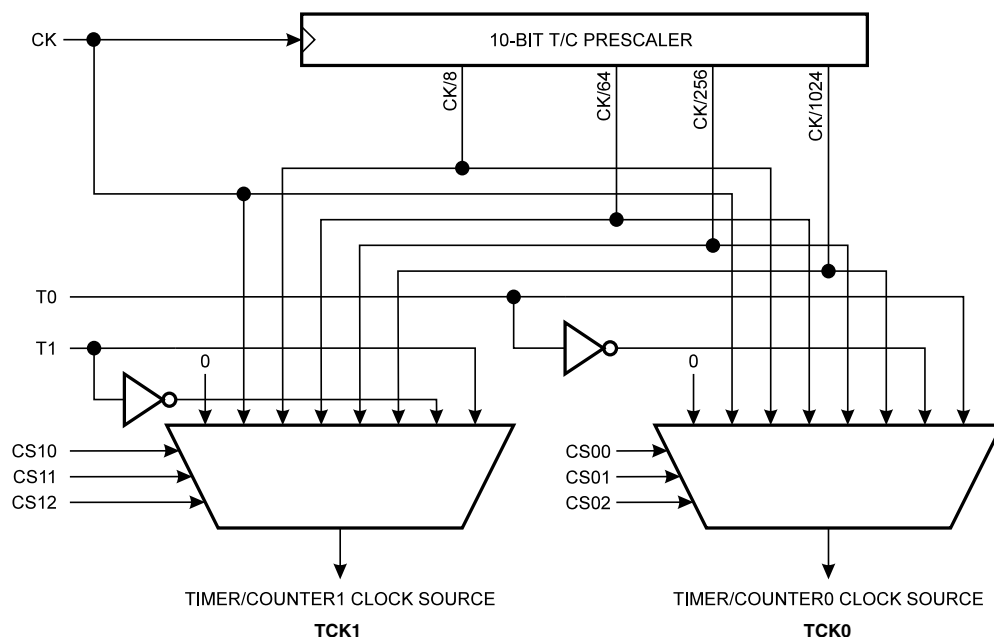


Figure 29 shows the block diagram for Timer/Counter0.

The 8-bit Timer/Counter0 can select clock source from CK, prescaled CK or an external pin. In addition, it can be stopped as described in the specification for the Timer/Counter0 Control Register (TCCR0). The overflow status flag is found in the Timer/Counter Interrupt Flag Register (TIFR). Control signals are found in the Timer/Counter0 Control Register (TCCR0). The interrupt enable/disable settings for Timer/Counter0 are found in the Timer/Counter Interrupt Mask Register (TIMSK).

When Timer/Counter0 is externally clocked, the external signal is synchronized with the oscillator frequency of the CPU. To assure proper sampling of the external clock, the minimum time between two external clock transitions must be at least one internal CPU clock period. The external clock signal is sampled on the rising edge of the internal CPU clock.

The 8-bit Timer/Counter0 features both a high-resolution and a high-accuracy usage with the lower prescaling opportunities. Similarly, the high prescaling opportunities make the Timer/Counter0 useful for lower speed functions or exact timing functions with infrequent actions.

The Stop condition provides a Timer Enable/Disable function. The CK down divided modes are scaled directly from the CK oscillator clock. If the external pin modes are used for Timer/Counter0, transitions on PB0/(T0) will clock the counter even if the pin is configured as an output. This feature can give the user software control of the counting.

## Timer Counter0 – TCNT0

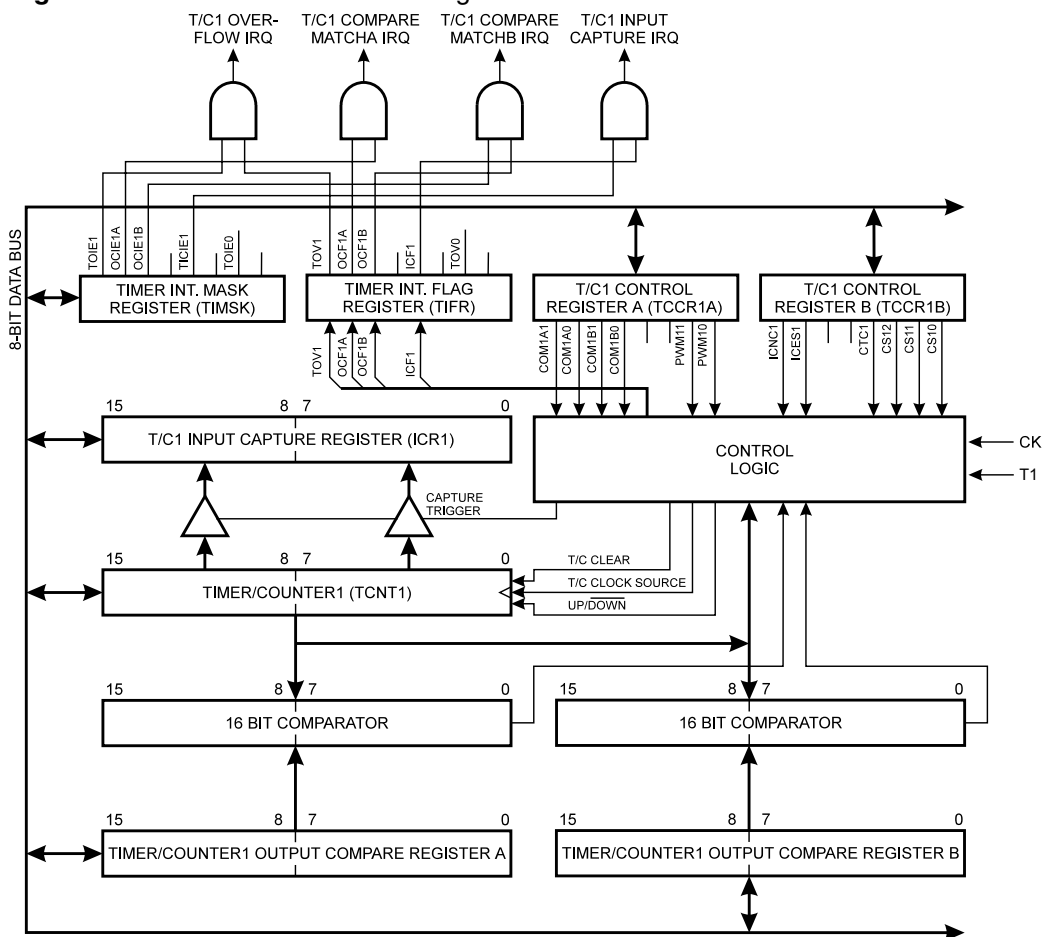
Bit	7	6	5	4	3	2	1	0	
\$32 (\$52)	<b>MSB</b>							<b>LSB</b>	TCNT0
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The Timer/Counter0 is realized as an up-counter with read and write access. If the Timer/Counter0 is written and a clock source is present, the Timer/Counter0 continues counting in the clock cycle following the write operation.

## 16-bit Timer/Counter1

Figure 30 shows the block diagram for Timer/Counter1.

**Figure 30. Timer/Counter1 Block Diagram**



The 16-bit Timer/Counter1 can select clock source from CK, prescaled CK or an external pin. In addition, it can be stopped as described in the specification for the Timer/Counter1 Control Registers (TCCR1A and TCCR1B). The different status flags (overflow, compare match and capture event) are found in the Timer/Counter Interrupt Flag Register (TIFR). Control signals are found in the Timer/Counter1 Control Registers

# Timer/Counter1 Control Register B – TCCR1B

Bit	7	6	5	4	3	2	1	0	
\$2E (\$4E)	ICNC1	ICES1	–	–	CTC1	CS12	CS11	CS10	TCCR1B
Read/Write	R/W	R/W	R	R	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

## • Bit 7 – ICNC1: Input Capture1 Noise Canceler (4 CKs)

When the ICNC1 bit is cleared (zero), the input capture trigger noise canceler function is disabled. The input capture is triggered at the first rising/falling edge sampled on the ICP (input capture pin) as specified. When the ICNC1 bit is set (one), four successive samples are measured on the ICP, and all samples must be high/low according to the input capture trigger specification in the ICES1 bit. The actual sampling frequency is XTAL clock frequency.

## • Bit 6 – ICES1: Input Capture1 Edge Select

While the ICES1 bit is cleared (zero), the Timer/Counter1 contents are transferred to the Input Capture Register (ICR1) on the falling edge of the input capture pin (ICP). While the ICES1 bit is set (one), the Timer/Counter1 contents are transferred to the ICR1 on the rising edge of the ICP.

## • Bits 5, 4 – Res: Reserved Bits

These bits are reserved bits in the AT90S8515 and always read zero.

## • Bit 3 – CTC1: Clear Timer/Counter1 on Compare Match

When the CTC1 control bit is set (one), the Timer/Counter1 is reset to \$0000 in the clock cycle after a compareA match. If the CTC1 control bit is cleared, Timer/Counter1 continues counting and is unaffected by a compare match. Since the compare match is detected in the CPU clock cycle following the match, this function will behave differently when a prescaling higher than 1 is used for the timer. When a prescaling of 1 is used, and the compareA register is set to C, the timer will count as follows if CTC1 is set:

... | C-2 | C-1 | C | 0 | 1 | ...

When the prescaler is set to divide by 8, the timer will count like this:

... | C-2, C-2, C-2, C-2, C-2, C-2, C-2, C-2 | C-1, C-1, C-1, C-1, C-1, C-1, C-1, C-1 | C, 0, 0, 0, 0, 0, 0 | ...

In PWM mode, this bit has no effect.

## • Bits 2, 1, 0 – CS12, CS11, CS10: Clock Select1, Bits 2, 1 and 0

The Clock Select1 bits 2, 1 and 0 define the prescaling source of Timer/Counter1.

**Table 10.** Clock 1 Prescale Select

CS12	CS11	CS10	Description
0	0	0	Stop, the Timer/Counter1 is stopped.
0	0	1	CK
0	1	0	CK/8
0	1	1	CK/64
1	0	0	CK/256
1	0	1	CK/1024
1	1	0	External Pin T1, falling edge
1	1	1	External Pin T1, rising edge



The TEMP register is also used when accessing TCNT1, OCR1A and OCR1B. If the main program and interrupt routines perform access to registers using TEMP, interrupts must be disabled during access from the main program (and from interrupt routines if interrupts are allowed from within interrupt routines).

#### Timer/Counter1 in PWM Mode

When the PWM mode is selected, Timer/Counter1, the Output Compare Register1A (OCR1A) and the Output Compare Register1B (OCR1B) form a dual 8-, 9- or 10-bit, free-running, glitch-free and phase-correct PWM with outputs on the PD5(OC1A) and OC1B pins. Timer/Counter1 acts as an up/down counter, counting up from \$0000 to TOP (see Table 11), where it turns and counts down again to zero before the cycle is repeated. When the counter value matches the contents of the 10 least significant bits of OCR1A or OCR1B, the PD5(OC1A)/OC1B pins are set or cleared according to the settings of the COM1A1/COM1A0 or COM1B1/COM1B0 bits in the Timer/Counter1 Control Register (TCCR1A). Refer to Table 12 for details.

**Table 11.** Timer TOP Values and PWM Frequency

PWM Resolution	Timer TOP Value	Frequency
8-bit	\$00FF (255)	$f_{TCK1}/510$
9-bit	\$01FF (511)	$f_{TCK1}/1022$
10-bit	\$03FF(1023)	$f_{TCK1}/2046$

**Table 12.** Compare1 Mode Select in PWM Mode

COM1X1	COM1X0	Effect on OCX1
0	0	Not connected
0	1	Not connected
1	0	Cleared on compare match, up-counting. Set on compare match, down-counting (non-inverted PWM).
1	1	Cleared on compare match, down-counting. Set on compare match, up-counting (inverted PWM).

Note: X = A or B

Note that in the PWM mode, the 10 least significant OCR1A/OCR1B bits, when written, are transferred to a temporary location. They are latched when Timer/Counter1 reaches the value TOP. This prevents the occurrence of odd-length PWM pulses (glitches) in the event of an unsynchronized OCR1A/OCR1B write. See Figure 32 for an example.

**Table 17. UBRR Settings at Various Crystal Frequencies**

Baud Rate	1 MHz	%Error	1.8432 MHz	%Error	2 MHz	%Error	2.4576 MHz	%Error
2400	UBRR= 25	0.2	UBRR= 47	0.0	UBRR= 51	0.2	UBRR= 63	0.0
4800	UBRR= 12	0.2	UBRR= 23	0.0	UBRR= 25	0.2	UBRR= 31	0.0
9600	UBRR= 6	7.5	UBRR= 11	0.0	UBRR= 12	0.2	UBRR= 15	0.0
14400	UBRR= 3	7.8	UBRR= 7	0.0	UBRR= 8	3.7	UBRR= 10	3.1
19200	UBRR= 2	7.8	UBRR= 5	0.0	UBRR= 6	7.5	UBRR= 7	0.0
28800	UBRR= 1	7.8	UBRR= 3	0.0	UBRR= 3	7.8	UBRR= 4	6.3
38400	UBRR= 1	22.9	UBRR= 2	0.0	UBRR= 2	7.8	UBRR= 3	0.0
57600	UBRR= 0	7.8	UBRR= 1	0.0	UBRR= 1	7.8	UBRR= 2	12.5
76800	UBRR= 0	22.9	UBRR= 1	33.3	UBRR= 1	22.9	UBRR= 1	0.0
115200	UBRR= 0	84.3	UBRR= 0	0.0	UBRR= 0	7.8	UBRR= 0	25.0

Baud Rate	3.2768 MHz	%Error	3.6864 MHz	%Error	4 MHz	%Error	4.608 MHz	%Error
2400	UBRR= 84	0.4	UBRR= 95	0.0	UBRR= 103	0.2	UBRR= 119	0.0
4800	UBRR= 42	0.8	UBRR= 47	0.0	UBRR= 51	0.2	UBRR= 59	0.0
9600	UBRR= 20	1.6	UBRR= 23	0.0	UBRR= 25	0.2	UBRR= 29	0.0
14400	UBRR= 13	1.6	UBRR= 15	0.0	UBRR= 16	2.1	UBRR= 19	0.0
19200	UBRR= 10	3.1	UBRR= 11	0.0	UBRR= 12	0.2	UBRR= 14	0.0
28800	UBRR= 6	1.6	UBRR= 7	0.0	UBRR= 8	3.7	UBRR= 9	0.0
38400	UBRR= 4	6.3	UBRR= 5	0.0	UBRR= 6	7.5	UBRR= 7	6.7
57600	UBRR= 3	12.5	UBRR= 3	0.0	UBRR= 3	7.8	UBRR= 4	0.0
76800	UBRR= 2	12.5	UBRR= 2	0.0	UBRR= 2	7.8	UBRR= 3	6.7
115200	UBRR= 1	12.5	UBRR= 1	0.0	UBRR= 1	7.8	UBRR= 2	20.0

Baud Rate	7.3728 MHz	%Error	8 MHz	%Error	9.216 MHz	%Error	11.059 MHz	%Error
2400	UBRR= 191	0.0	UBRR= 207	0.2	UBRR= 239	0.0	UBRR= 287	-
4800	UBRR= 95	0.0	UBRR= 103	0.2	UBRR= 119	0.0	UBRR= 143	0.0
9600	UBRR= 47	0.0	UBRR= 51	0.2	UBRR= 59	0.0	UBRR= 71	0.0
14400	UBRR= 31	0.0	UBRR= 34	0.8	UBRR= 39	0.0	UBRR= 47	0.0
19200	UBRR= 23	0.0	UBRR= 25	0.2	UBRR= 29	0.0	UBRR= 35	0.0
28800	UBRR= 15	0.0	UBRR= 16	2.1	UBRR= 19	0.0	UBRR= 23	0.0
38400	UBRR= 11	0.0	UBRR= 12	0.2	UBRR= 14	0.0	UBRR= 17	0.0
57600	UBRR= 7	0.0	UBRR= 8	3.7	UBRR= 9	0.0	UBRR= 11	0.0
76800	UBRR= 5	0.0	UBRR= 6	7.5	UBRR= 7	6.7	UBRR= 8	0.0
115200	UBRR= 3	0.0	UBRR= 3	7.8	UBRR= 4	0.0	UBRR= 5	0.0

#### UART BAUD Rate Register – UBRR

Bit	7	6	5	4	3	2	1	0	
\$09 (\$29)	MSB							LSB	UBRR
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

The UBRR register is an 8-bit read/write register that specifies the UART Baud Rate according to the equation on the previous page.

## Port B

Port B is an 8-bit bi-directional I/O port.

Three I/O memory address locations are allocated for the Port B, one each for the Data Register – PORTB, \$18(\$38), Data Direction Register – DDRB, \$17(\$37) and the Port B Input Pins – PINB, \$16(\$36). The Port B Input Pins address is read-only, while the Data Register and the Data Direction Register are read/write.

All port pins have individually selectable pull-up resistors. The Port B output buffers can sink 20 mA and thus drive LED displays directly. When pins PB0 to PB7 are used as inputs and are externally pulled low, they will source current if the internal pull-up resistors are activated.

The Port B pins with alternate functions are shown in Table 20.

**Table 20.** Port B Pin Alternate Functions

Port Pin	Alternate Functions
PB0	T0 (Timer/Counter 0 External Counter Input)
PB1	T1 (Timer/Counter 1 External Counter Input)
PB2	AIN0 (Analog Comparator positive input)
PB3	AIN1 (Analog Comparator negative input)
PB4	$\overline{SS}$ (SPI Slave Select Input)
PB5	MOSI (SPI Bus Master Output/Slave Input)
PB6	MISO (SPI Bus Master Input/Slave Output)
PB7	SCK (SPI Bus Serial Clock)

When the pins are used for the alternate function, the DDRB and PORTB registers have to be set according to the alternate function description.

### Port B Data Register – PORTB

Bit	7	6	5	4	3	2	1	0	
\$18 (\$38)	<b>PORTB7</b>	<b>PORTB6</b>	<b>PORTB5</b>	<b>PORTB4</b>	<b>PORTB3</b>	<b>PORTB2</b>	<b>PORTB1</b>	<b>PORTB0</b>	PORTB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

### Port B Data Direction Register – DDRB

Bit	7	6	5	4	3	2	1	0	
\$17 (\$37)	<b>DDB7</b>	<b>DDB6</b>	<b>DDB5</b>	<b>DDB4</b>	<b>DDB3</b>	<b>DDB2</b>	<b>DDB1</b>	<b>DDB0</b>	DDRB
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Initial Value	0	0	0	0	0	0	0	0	

### Port B Input Pins Address – PINB

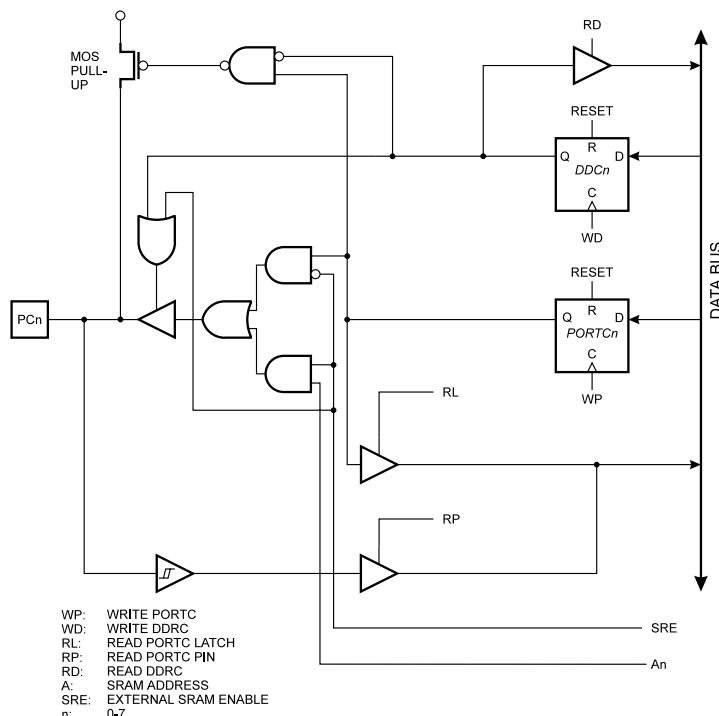
Bit	7	6	5	4	3	2	1	0	
\$16 (\$36)	<b>PINB7</b>	<b>PINB6</b>	<b>PINB5</b>	<b>PINB4</b>	<b>PINB3</b>	<b>PINB2</b>	<b>PINB1</b>	<b>PINB0</b>	PINB
Read/Write	R	R	R	R	R	R	R	R	
Initial Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	

The Port B Input Pins address (PINB) is not a register; this address enables access to the physical value on each Port B pin. When reading PORTB, the Port B Data Latch is read and when reading PINB, the logical values present on the pins are read.

## Port C Schematics

Note that all port pins are synchronized. The synchronization latch is, however, not shown in the figure.

**Figure 52.** Port C Schematic Diagram (Pins PC0 - PC7)



## Port D

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors.

Three I/O memory address locations are allocated for the Port D, one each for the Data Register – PORTD, \$12(\$32), Data Direction Register – DDRD, \$11(\$31) and the Port D Input Pins – PIND, \$10(\$30). The Port D Input Pins address is read-only, while the Data Register and the Data Direction Register are read/write.

The Port D output buffers can sink 20 mA. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated.

Some Port D pins have alternate functions as shown in Table 23.

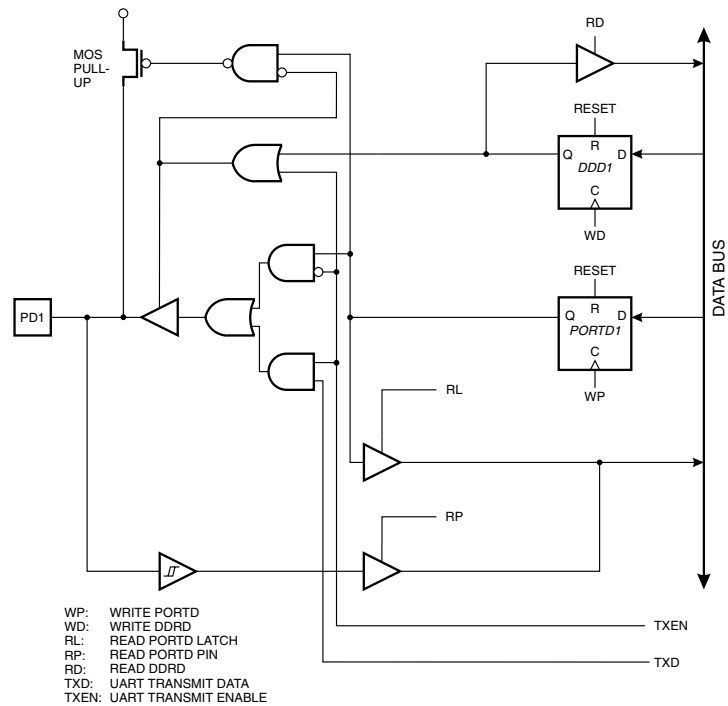
**Table 23.** Port D Pin Alternate Functions

Port Pin	Alternate Function
PD0	RXD (UART Input Line)
PD1	TXD (UART Output Line)
PD2	INT0 (External interrupt 0 Input)
PD3	INT1 (External interrupt 1 Input)
PD5	OC1A (Timer/Counter1 Output CompareA Match Output)
PD6	$\overline{WR}$ (Write Strobe to External Memory)
PD7	$\overline{RD}$ (Read Strobe to External Memory)

When the pins are used for the alternate function, the DDRD and PORTD registers have to be set according to the alternate function description.



**Figure 54. Port D Schematic Diagram (Pin PD1)**



**Figure 55.** Port D Schematic Diagram (Pins PD2 and PD3)

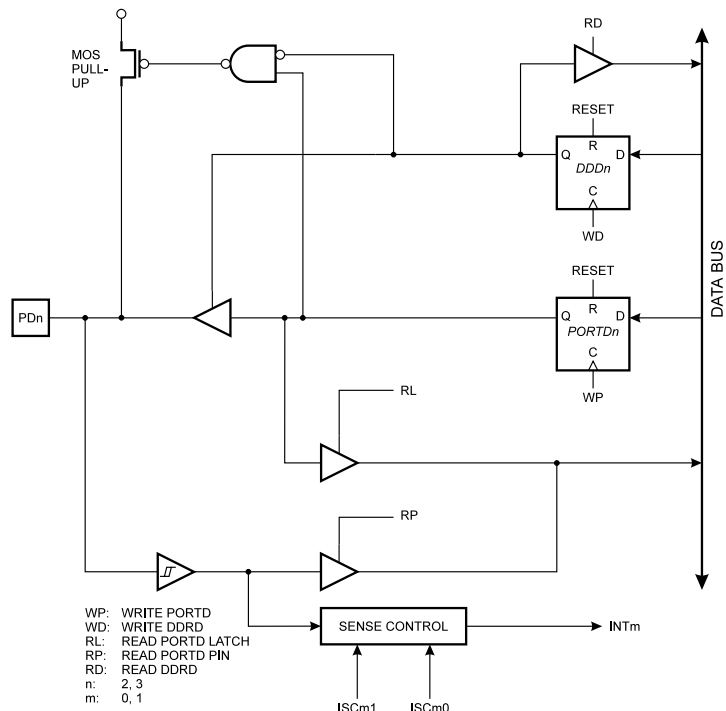


Figure 58. Port D Schematic Diagram (Pin PD6)

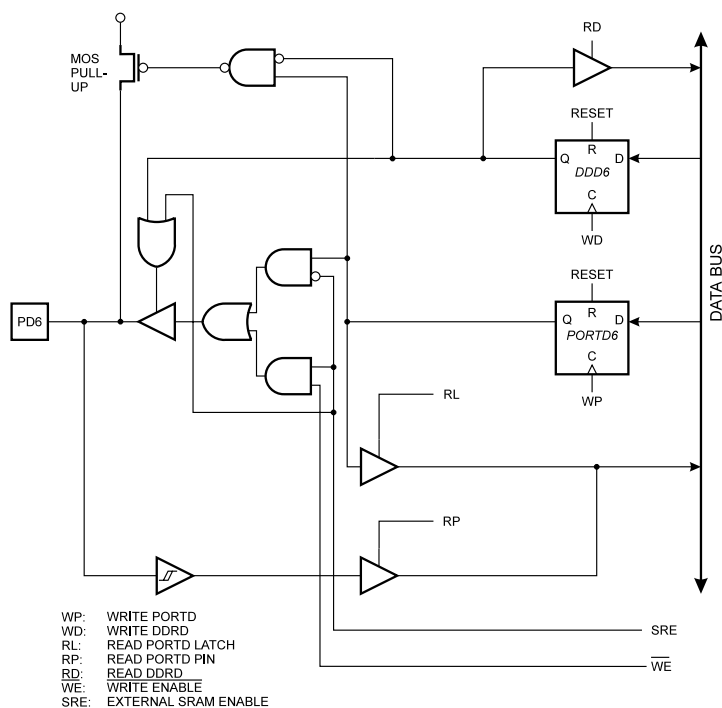
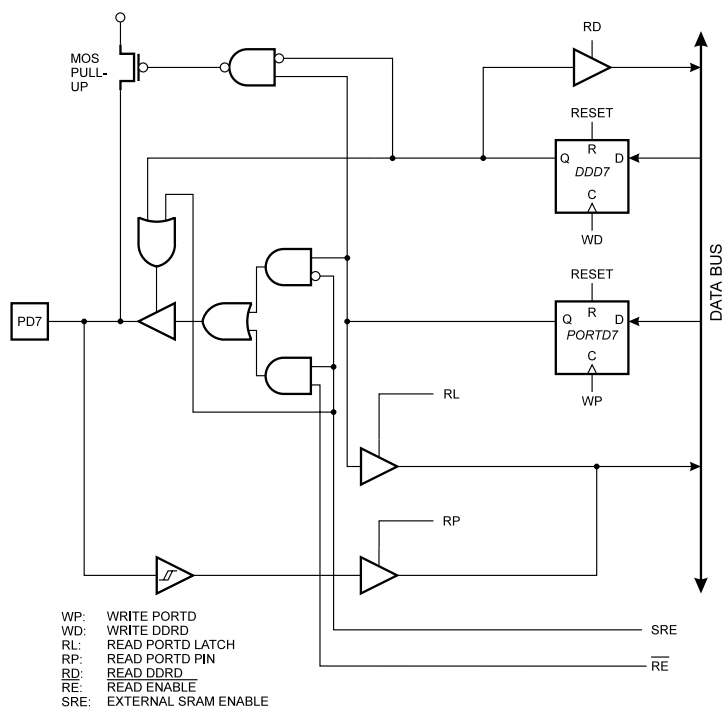


Figure 59. Port D Schematic Diagram (Pin PD7)



## Parallel Programming Characteristics

Figure 63. Parallel Programming Timing

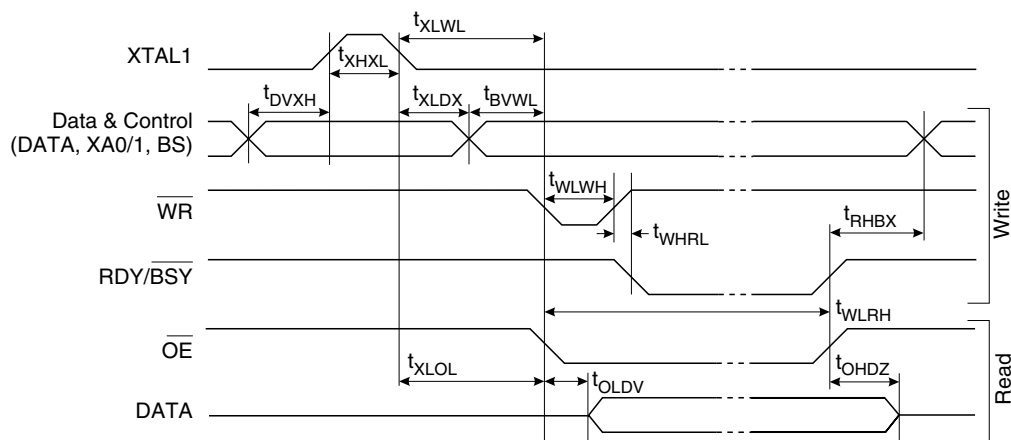


Table 30. Parallel Programming Characteristics,  $T_A = 25^\circ\text{C} \pm 10\%$ ,  $V_{CC} = 5\text{V} \pm 10\%$

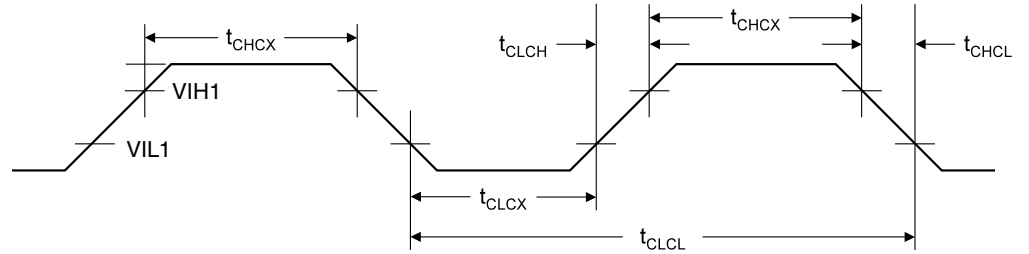
Symbol	Parameter	Min	Typ	Max	Units
$V_{PP}$	Programming Enable Voltage	11.5		12.5	V
$I_{PP}$	Programming Enable Current			250.0	$\mu\text{A}$
$t_{DVXH}$	Data and Control Setup before XTAL1 High	67.0			ns
$t_{XHXL}$	XTAL1 Pulse Width High	67.0			ns
$t_{XLDX}$	Data and Control Hold after XTAL1 Low	67.0			ns
$t_{XLWL}$	XTAL1 Low to $\overline{WR}$ Low	67.0			ns
$t_{BVWL}$	BS Valid to $\overline{WR}$ Low	67.0			ns
$t_{RHBX}$	BS Hold after RDY/ $\overline{BSY}$ High	67.0			ns
$t_{WLWH}$	$\overline{WR}$ Pulse Width Low <sup>(1)</sup>	67.0			ns
$t_{WHRL}$	$\overline{WR}$ High to RDY/ $\overline{BSY}$ Low <sup>(2)</sup>		20.0		ns
$t_{WLRH}$	$\overline{WR}$ Low to RDY/ $\overline{BSY}$ High <sup>(2)</sup>	0.5	0.7	0.9	ms
$t_{XLOL}$	XTAL1 Low to $\overline{OE}$ Low	67.0			ns
$t_{OLDV}$	$\overline{OE}$ Low to DATA Valid		20.0		ns
$t_{OHDZ}$	$\overline{OE}$ High to DATA Tri-stated			20.0	ns
$t_{WLWH\_CE}$	$\overline{WR}$ Pulse Width Low for Chip Erase	5.0	10.0	15.0	ms
$t_{WLWH\_PFB}$	$\overline{WR}$ Pulse Width Low for Programming the Fuse Bits	1.0	1.5	1.8	ms

- Notes: 1. Use  $t_{WLWH\_CE}$  for Chip Erase and  $t_{WLWH\_PFB}$  for programming the Fuse bits.  
2. If  $t_{WLWH}$  is held longer than  $t_{WLRH}$ , no RDY/ $\overline{BSY}$  pulse will be seen.



## External Clock Drive Waveforms

**Figure 67.** External Clock

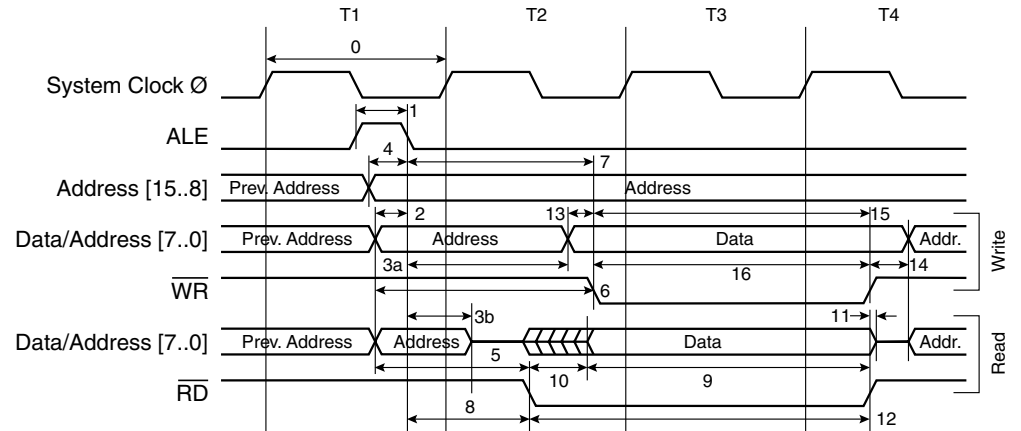


**Table 36.** External Clock Drive

Symbol	Parameter	V <sub>CC</sub> = 2.7V to 4.0V		V <sub>CC</sub> = 4.0V to 6.0V		Units
		Min	Max	Min	Max	
1/t <sub>CLCL</sub>	Oscillator Frequency	0	4.0	0	8.0	MHz
t <sub>CLCL</sub>	Clock Period	250.0		125.0		ns
t <sub>CHCX</sub>	High Time	100.0		50.0		ns
t <sub>CLCX</sub>	Low Time	100.0		50.0		ns
t <sub>CLCH</sub>	Rise Time		1.6		0.5	μs
t <sub>CHCL</sub>	Fall Time		1.6		0.5	μs

Note: See “External Data Memory Timing” for a description of how the duty cycle influences the timing for the external data memory.

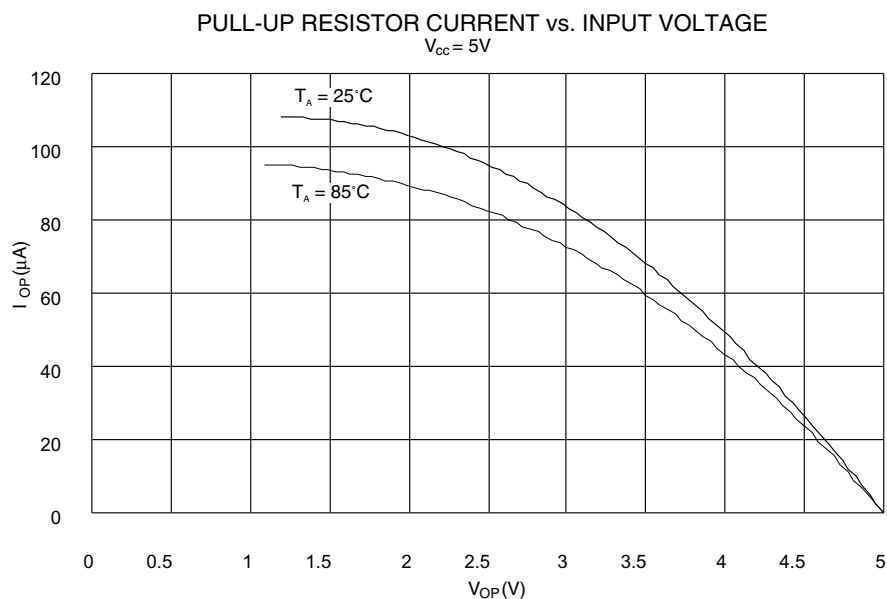
**Figure 68.** External RAM Timing



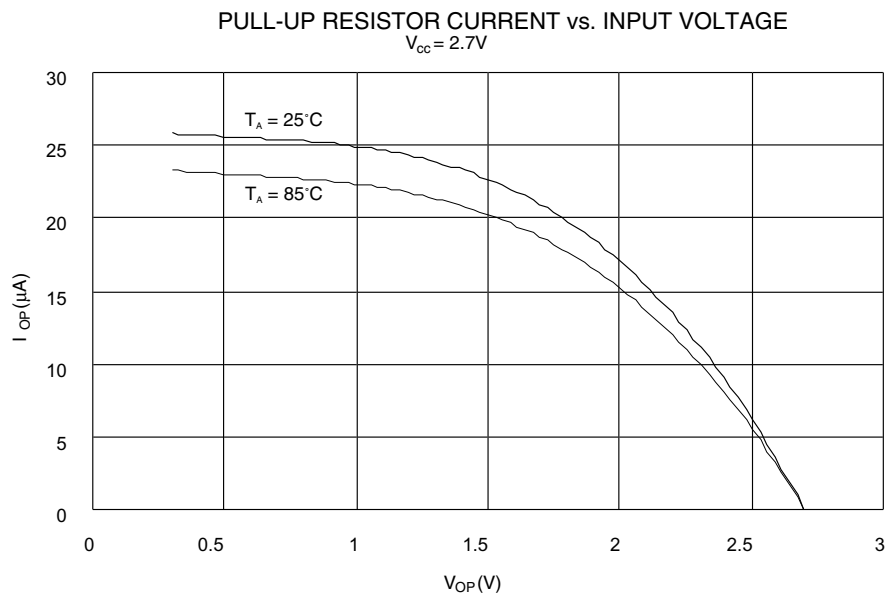
Note: Clock cycle T3 is only present when external SRAM wait state is enabled.

Sink and source capabilities of I/O ports are measured on one pin at a time.

**Figure 80.** Pull-up Resistor Current vs. Input Voltage



**Figure 81.** Pull-up Resistor Current vs. Input Voltage

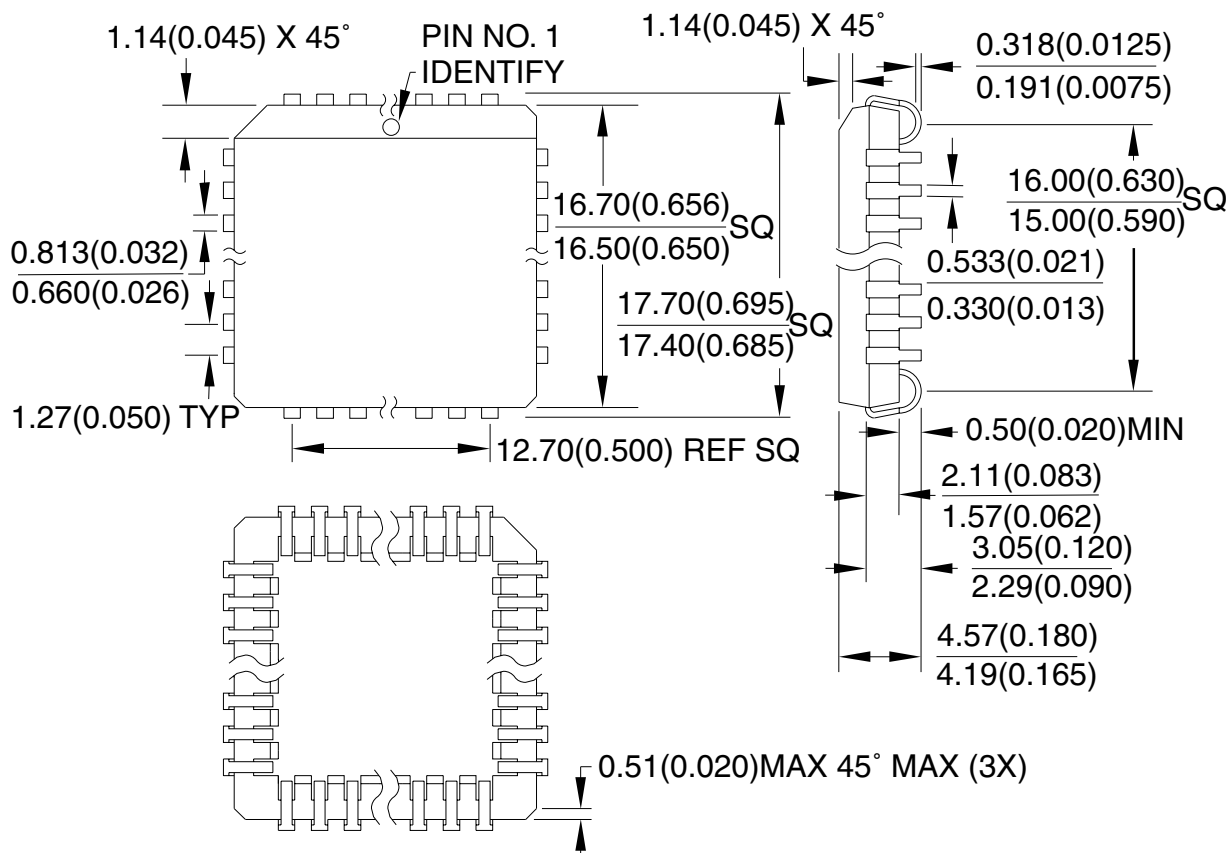


## Instruction Set Summary

Mnemonic	Operands	Description	Operation	Flags	# Clocks
<b>ARITHMETIC AND LOGIC INSTRUCTIONS</b>					
ADD	Rd, Rr	Add Two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry Two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	Rdl, K	Add Immediate to Word	$Rdh:Rdl \leftarrow Rdh:Rdl + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract Two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBC	Rd, Rr	Subtract with Carry Two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
SBIW	Rdl, K	Subtract Immediate from Word	$Rdh:Rdl \leftarrow Rdh:Rdl - K$	Z,C,N,V,S	2
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \bullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd \vee Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \vee K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	$Rd \leftarrow \$FF - Rd$	Z,C,N,V	1
NEG	Rd	Two's Complement	$Rd \leftarrow \$00 - Rd$	Z,C,N,V,H	1
SBR	Rd, K	Set Bit(s) in Register	$Rd \leftarrow Rd \vee K$	Z,N,V	1
CBR	Rd, K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (\$FF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	$Rd \leftarrow \$FF$	None	1
<b>BRANCH INSTRUCTIONS</b>					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP		Indirect Jump to (Z)	$PC \leftarrow Z$	None	2
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect Call to (Z)	$PC \leftarrow Z$	None	3
RET		Subroutine Return	$PC \leftarrow STACK$	None	4
RETI		Interrupt Return	$PC \leftarrow STACK$	I	4
CPSE	Rd, Rr	Compare, Skip if Equal	if (Rd = Rr) $PC \leftarrow PC + 2$ or 3	None	1/2/3
CP	Rd, Rr	Compare	$Rd - Rr$	Z,N,V,C,H	1
CPC	Rd, Rr	Compare with Carry	$Rd - Rr - C$	Z,N,V,C,H	1
CPI	Rd, K	Compare Register with Immediate	$Rd - K$	Z,N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b) = 0) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b) = 1) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if (P(b) = 0) $PC \leftarrow PC + 2$ or 3	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if (P(b) = 1) $PC \leftarrow PC + 2$ or 3	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRCC	k	Branch if Carry Cleared	if (C = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRMI	k	Branch if Minus	if (N = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRPL	k	Branch if Plus	if (N = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRGE	k	Branch if Greater or Equal, Signed	if (N $\oplus$ V = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRLT	k	Branch if Less Than Zero, Signed	if (N $\oplus$ V = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRHS	k	Branch if Half-carry Flag Set	if (H = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRHC	k	Branch if Half-carry Flag Cleared	if (H = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRTS	k	Branch if T-flag Set	if (T = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRTC	k	Branch if T-flag Cleared	if (T = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then $PC \leftarrow PC + k + 1$	None	1/2

44J

44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)  
 Dimensions in Millimeters and (Inches)\*  
 JEDEC STANDARD MS-018 AC

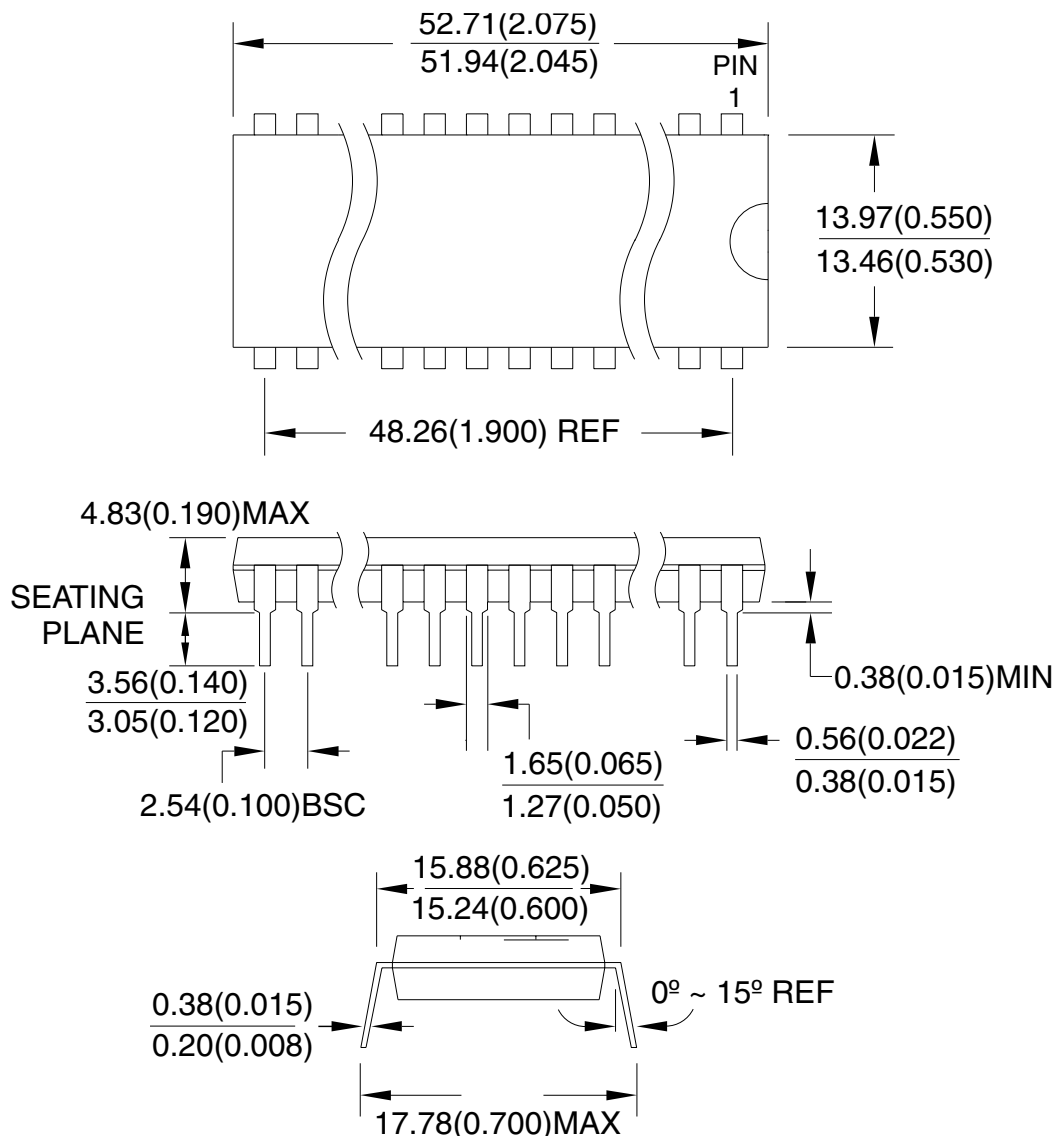


\*Controlling dimensions: Inches

REV. A 04/11/2001

40P6

40-lead, Plastic Dual Inline  
 Package (PDIP), 0.600" wide  
 Dimension in Millimeters and (Inches)\*  
 JEDEC STANDARD MS-011 AC



\*Controlling dimension: Inches

REV. A 04/11/2001