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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	28MHz
Connectivity	EBI/EMI, SCI
Peripherals	DMA, PWM, WDT
Number of I/O	35
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	112-BQFP
Supplier Device Package	112-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6417014f28v

2.1.2 Control Registers

The 32-bit control registers consist of the 32-bit status register (SR), global base register (GBR), and vector base register (VBR). The status register indicates processing states. The global base register functions as a base address for the indirect GBR addressing mode to transfer data to the registers of on-chip peripheral modules. The vector base register functions as the base address of the exception processing vector area (including interrupts). Figure 2.2 shows a control register.

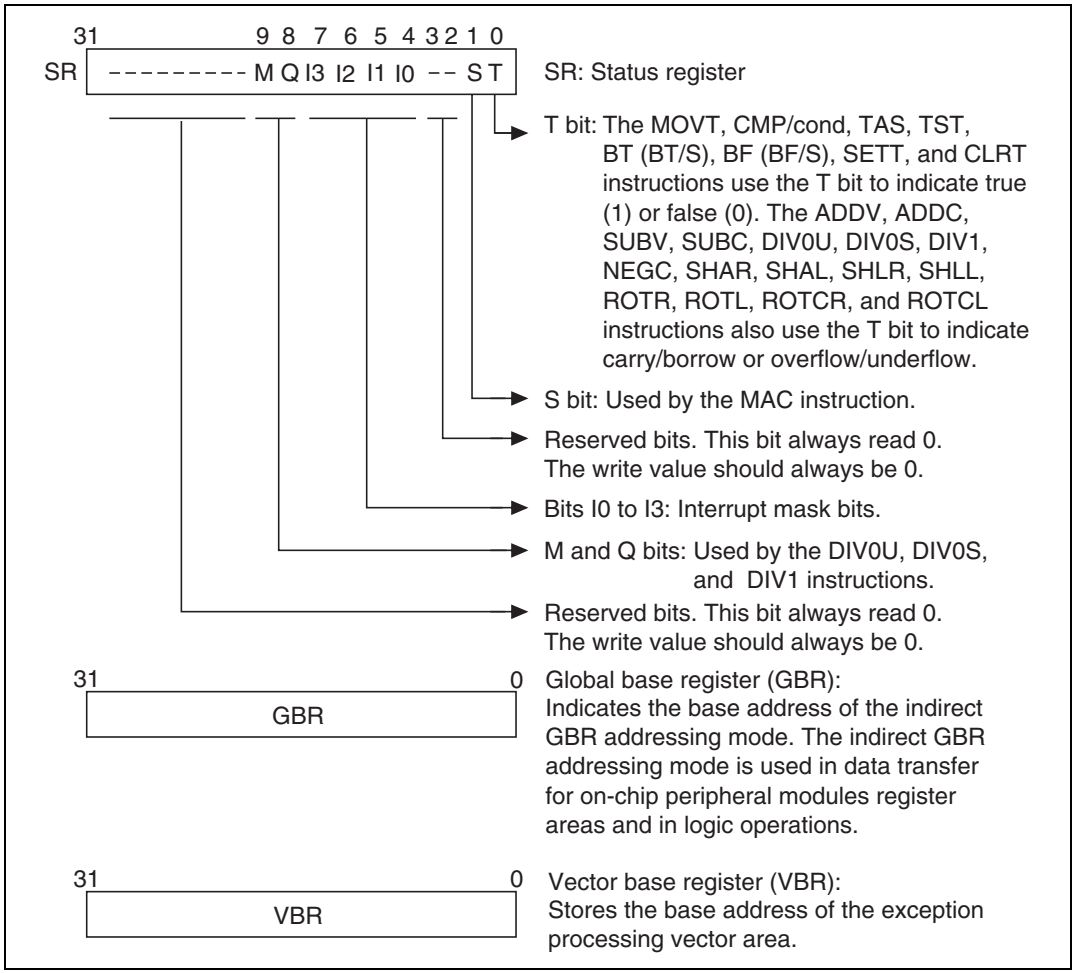

Figure 2.2 Control Registers

Instruction	Instruction Code	Operation	Exec. Cycles	T Bit
MOV.W Rm,@(R0,Rn)	0000nnnnmmmm0101	Rm → (R0 + Rn)	1	—
MOV.L Rm,@(R0,Rn)	0000nnnnmmmm0110	Rm → (R0 + Rn)	1	—
MOV.B @(R0,Rm),Rn	0000nnnnmmmm1100	(R0 + Rm) → Sign extension → Rn	1	—
MOV.W @(R0,Rm),Rn	0000nnnnmmmm1101	(R0 + Rm) → Sign extension → Rn	1	—
MOV.L @(R0,Rm),Rn	0000nnnnmmmm1110	(R0 + Rm) → Rn	1	—
MOV.B R0,@(disp,GBR)	11000000dddddddd	R0 → (disp + GBR)	1	—
MOV.W R0,@(disp,GBR)	11000001dddddddd	R0 → (disp × 2 + GBR)	1	—
MOV.L R0,@(disp,GBR)	11000010dddddddd	R0 → (disp × 4 + GBR)	1	—
MOV.B @(disp,GBR),R0	11000100dddddddd	(disp + GBR) → Sign extension → R0	1	—
MOV.W @(disp,GBR),R0	11000101dddddddd	(disp × 2 + GBR) → Sign extension → R0	1	—
MOV.L @(disp,GBR),R0	11000110dddddddd	(disp × 4 + GBR) → R0	1	—
MOVA @(disp,PC),R0	11000111dddddddd	disp × 4 + PC → R0	1	—
MOVT Rn	0000nnnn00101001	T → Rn	1	—
SWAP.B Rm,Rn	0110nnnnmmmm1000	Rm → Swap the bottom two bytes → Rn	1	—
SWAP.W Rm,Rn	0110nnnnmmmm1001	Rm → Swap two consecutive words → Rn	1	—
XTRCT Rm,Rn	0010nnnnmmmm1101	Rm: Middle 32 bits of Rn → Rn	1	—

Table 2.16 Branch Instructions

Instruction	Instruction Code	Operation	Exec. Cycles	T Bit
BF label	10001011dddddddd	If T = 0, disp × 2 + PC → PC; if T = 1, NOP	3/1*	—
BF/S label	10001111dddddddd	Delayed branch, if T = 0, disp × 2 + PC → PC; if T = 1, NOP	3/1*	—
BT label	10001001dddddddd	If T = 1, disp × 2 + PC → PC; if T = 0, NOP	3/1*	—
BT/S label	10001101dddddddd	Delayed branch, if T = 1, disp × 2 + PC → PC; if T = 0, NOP	2/1*	—
BRA label	1010dddddddddddd	Delayed branch, disp × 2 + PC → PC	2	—
BRAF Rm	0000mmmm00100011	Delayed branch, Rm + PC → PC	2	—
BSR label	1011dddddddddddd	Delayed branch, PC → PR, disp × 2 + PC → PC	2	—
BSRF Rm	0000mmmm00000011	Delayed branch, PC → PR, Rm + PC → PC	2	—
JMP @Rm	0100mmmm00101011	Delayed branch, Rm → PC	2	—
JSR @Rm	0100mmmm00001011	Delayed branch, PC → PR, Rm → PC	2	—
RTS	0000000000001011	Delayed branch, PR → PC	2	—

Note: One state when it does not branch.

Interrupt Source		Interrupt Vector		Interrupt Priority (Initial Value)	Corresponding IPR (Bits)	Priority within IPR Setting Range	Default Priority
		Vector No.	Vector Table Address Offset				
A/D*	ADI	136	H'00000220 to H'00000223	0 to 15 (0)	IPRG (15 to 12)	—	High
		138	H'00000228 to H'0000022B				
CMT0	CMI0	144	H'00000240 to H'00000243	0 to 15 (0)	IPRG (7 to 4)	—	
CMT1	CMI1	148	H'00000250 to H'00000253	0 to 15 (0)	IPRG (3 to 0)	—	
WDT	ITI	152	H'00000260 to H'00000263	0 to 15 (0)	IPRH (15 to 12)	High	
BSC	CMI	153	H'00000264 to H'00000267	0 to 15 (0)		Low	Low

Note: * Vector No. 136 = SH7014 only
138 = SH7016, SH7017 only

8.1.3 Pin Configuration

Table 8.1 shows the bus state controller pin configuration.

Table 8.1 Pin Configuration

Signal	I/O	Description
A21 to A0	O	Address output (A21 to A18 become input ports in power-on reset)
D15 to D0	I/O	16-bit data bus. D15-D0 are address output and data I/O during address/data multiplex I/O.
$\overline{CS0}$ to $\overline{CS3}$	O	Chip select
$\overline{RD}$	O	Strobe that indicates the read cycle for ordinary space/multiplex I/O. Also output during DRAM access.
$\overline{WRH}$	O	Strobe that indicates a write cycle to the higher byte (D15 to D8) for ordinary space/multiplex I/O. Also output during DRAM access.
$\overline{WRL}$	O	Strobe that indicates a write cycle to the lower byte (D7 to D0) for ordinary space/multiplex I/O. Also output during DRAM access.
RDWR	O	Strobe indicating a write cycle to DRAM (used for DRAM space)
$\overline{RAS}$	O	RAS signal for DRAM (used for DRAM space)
$\overline{CASH}$	O	CAS signal when accessing the higher byte (D15 to D8) of DRAM (used for DRAM space)
$\overline{CASL}$	O	CAS signal when accessing the lower byte (D7 to D0) of DRAM (used for DRAM space)
$\overline{AH}$	O	Signal to hold the address during address/data multiplex
$\overline{WAIT}$	I	Wait state request signal

8.1.4 Register Configuration

The BSC has eight registers. These registers are used to control wait states, bus width, and interfaces with memories like DRAM, SRAM, and ROM, as well as refresh control. The register configurations are listed in table 8.2.

All registers are 16 bits. Do not access DRAM space before completing the memory interface settings. All BSC registers are all initialized by a power-on reset. Values are maintained in standby mode.

Bus Modes

Select the appropriate bus mode in the TM bits of CHCR0, CHCR1. There are two bus modes: cycle steal and burst.

Cycle-Steal Mode: In the cycle steal mode, the bus right is given to another bus master after each one-transfer-unit (byte, word, or longword) DMAC transfer. When the next transfer request occurs, the bus rights are obtained from the other bus master and a transfer is performed for one transfer unit. When that transfer ends, the bus right is passed to the other bus master. This is repeated until the transfer end conditions are satisfied.

The cycle steal mode can be used with all categories of transfer destination, transfer source and transfer request. Figure 9.7 shows an example of DMA transfer timing in the cycle steal mode. Transfer conditions are dual address mode and $\overline{\text{DREQ}}$ level detection.

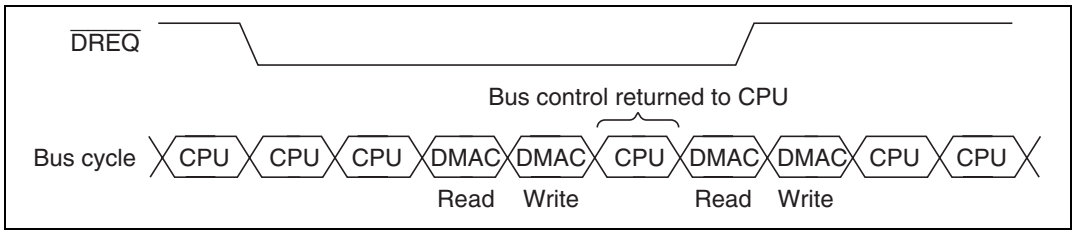

Figure 9.7 DMA Transfer Example in the Cycle-Steal Mode

Burst Mode: Once the bus right is obtained, the transfer is performed continuously until the transfer end condition is satisfied. In the external request mode with low level detection of the $\overline{\text{DREQ}}$ pin, however, when the $\overline{\text{DREQ}}$ pin is driven high, the bus passes to the other bus master after the bus cycle of the DMAC that currently has an acknowledged request ends, even if the transfer end conditions have not been satisfied.

Figure 9.8 shows an example of DMA transfer timing in the burst mode. Transfer conditions are single address mode and $\overline{\text{DREQ}}$ level detection.

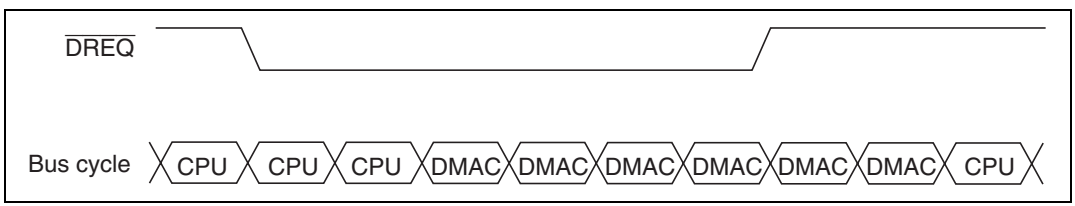

Figure 9.8 DMA Transfer Example in the Burst Mode

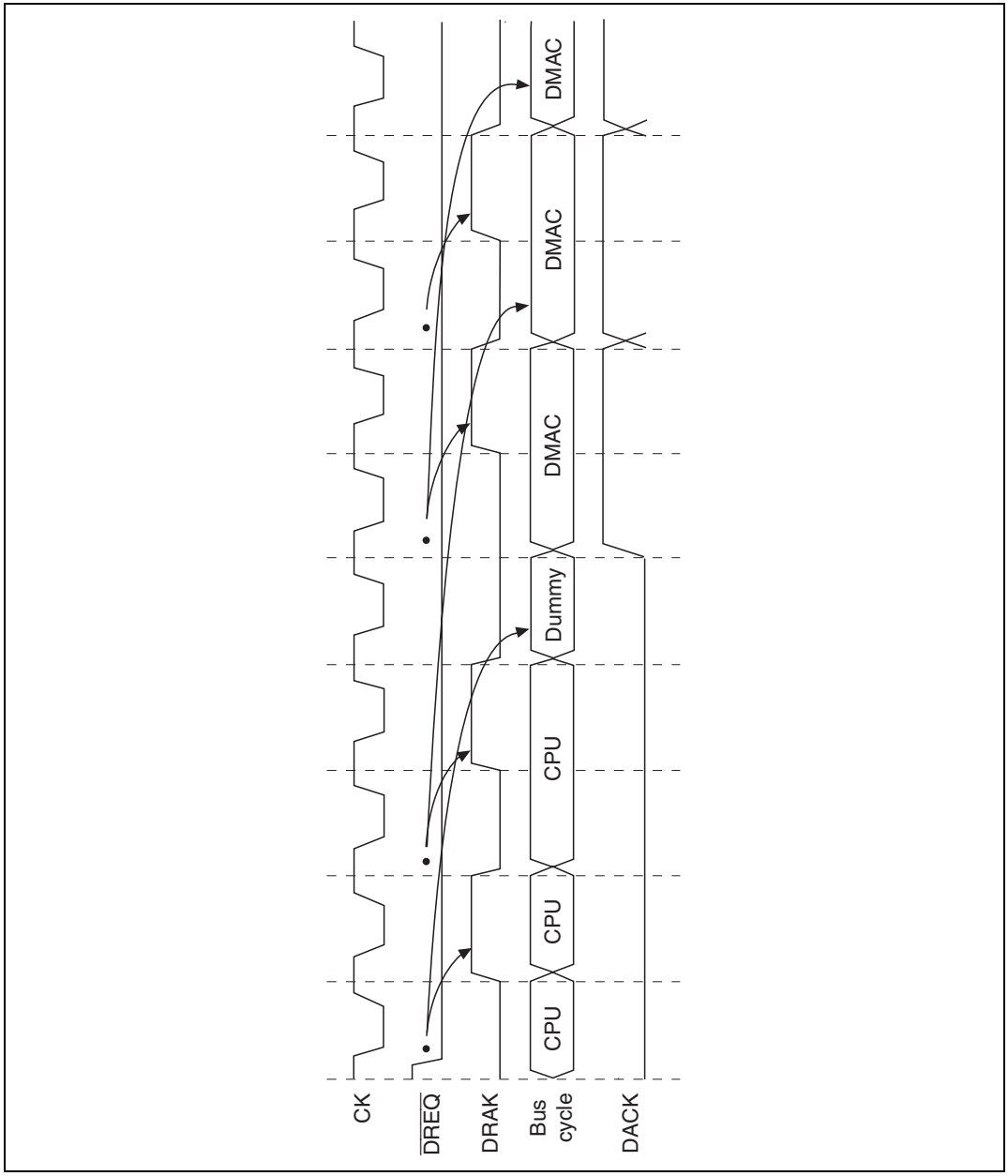

Figure 9.16 Burst Mode, Single Address and Level Detection (Normal Operation)

Input Capture Function: In the input capture mode, the TCNT value is transferred into the TGR register when the input edge is detected at the input capture/output compare pin (TIOC).

Detection can take place on the rising edge, falling edge, or both edges. Channels 0 and 1 can use other channel counter input clocks or compare-match signals as input capture sources.

The procedure for selecting the input capture operation (figure 10.12) is:

1. Set the TIOR to select the input capture function of the TGR, then select the input capture source, and rising edge, falling edge, or both edges as the input edge.
2. Set the CST bit in the TSTR to 1 to start the TCNT counting.

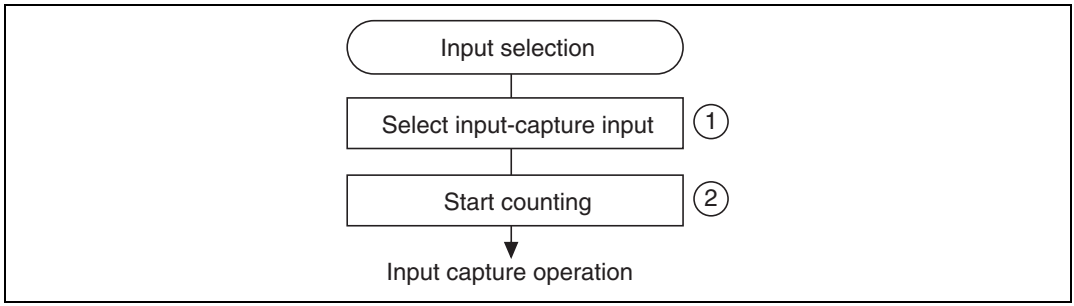

Figure 10.12 Procedure for Selecting Input Capture Operation

10.5 Interrupts

10.5.1 Interrupt Sources and Priority Ranking

The MTU has three interrupt sources: TGR register compare-match/input captures, TCNT counter overflows and TCNT counter underflows. Because each of these three types of interrupts are allocated its own dedicated status flag and enable/disable bit, the issuing of interrupt request signals to the interrupt controller can be independently enabled or disabled.

When an interrupt source is generated, the corresponding status flag in the timer status register (TSR) is set to 1. If the corresponding enable/disable bit in the timer input enable register (TIER) is set to 1 at this time, the MTU makes an interrupt request of the interrupt controller. The interrupt request is canceled by clearing the status flag to 0.

The channel priority order can be changed with the interrupt controller. The priority ranking within a channel is fixed. For more information, see section 6, Interrupt Controller.

Table 10.13 lists the MTU interrupt sources.

Input Capture/Compare Match Interrupts: If the TGIE bit of the timer input enable register (TIER) is already set to 1 when the TGF flag in the timer status register (TSR) is set to 1 by a TGR register input capture/compare-match of any channel, an interrupt request is sent to the interrupt controller. The interrupt request is canceled by clearing the TGF flag to 0. The MTU has 8 input capture/compare-match interrupts; four for channel 0, and two each for channels 1 and 2.

Overflow Interrupts: If the TCIEV bit of the TIER is already set to 1 when the TCFV flag in the TSR is set to 1 by a TCNT counter overflow of any channel, an interrupt request is sent to the interrupt controller. The interrupt request is canceled by clearing the TCFV flag to 0. The MTU has three overflow interrupts, one for each channel.

Underflow Interrupts: If the TCIEU bit of the TIER is already set to 1 when the TCFU flag in the TSR is set to 1 by a TCNT counter underflow of any channel, an interrupt request is sent to the interrupt controller. The interrupt request is canceled by clearing the TCFU flag to 0. The MTU has two underflow interrupts, one each for channels 1 and 2.

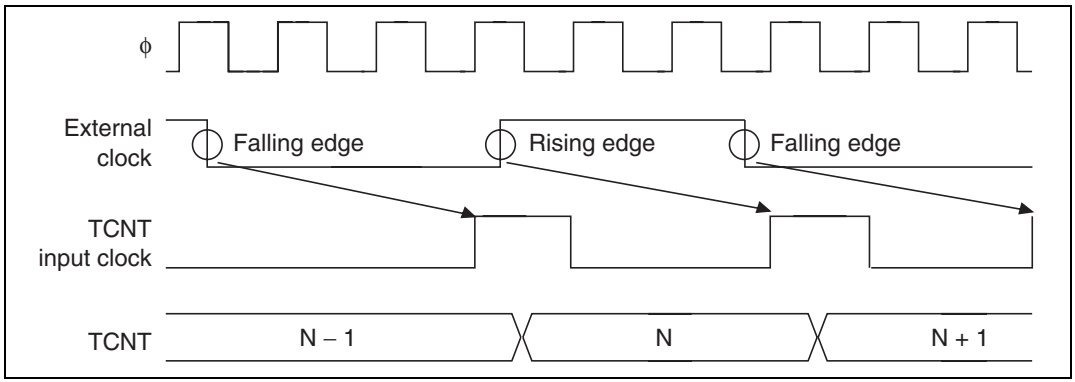

Figure 10.36 TCNT Count Timing during External Clock Operation (Phase Counting Mode)

Output Compare Output Timing: The compare-match signal is generated at the final state of TCNT and TGR matching. When a compare-match signal is issued, the output value set in TIOR is output to the output compare output pin (the TIOC pin). After TCNT and TGR matching, a compare-match signal is not issued until immediately before the TCNT input clock.

Output compare output timing (normal mode and PWM mode) is shown in figure 10.37.

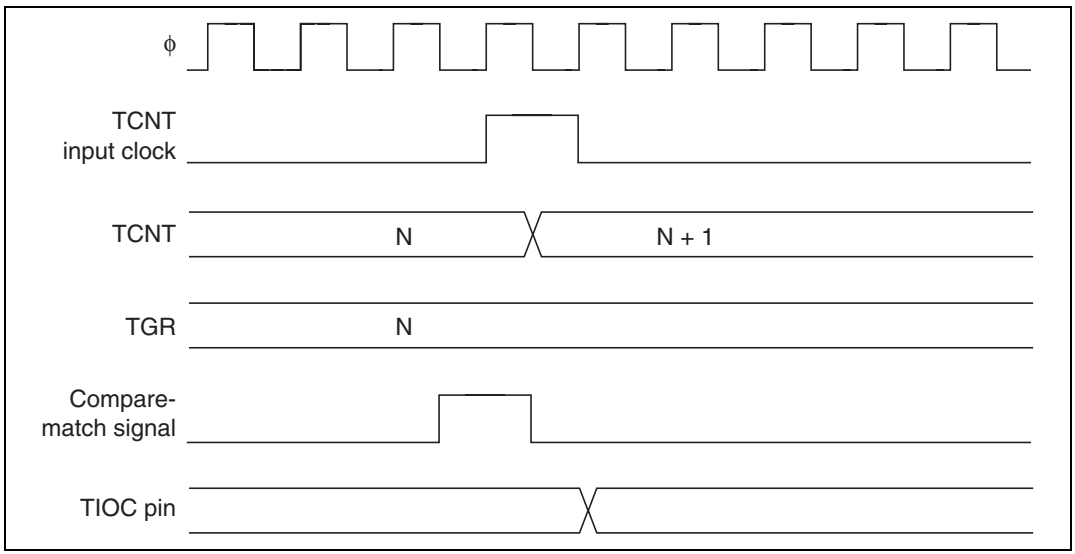

Figure 10.37 Output Compare Output Timing (Normal Mode/PWM Mode)

(3) Operation when Error Occurs during Normal Mode Operation, and Operation is Restarted in PWM Mode 2: Figure 10.62 shows an explanatory diagram of the case where an error occurs in normal mode and operation is restarted in PWM mode 2 after re-setting.

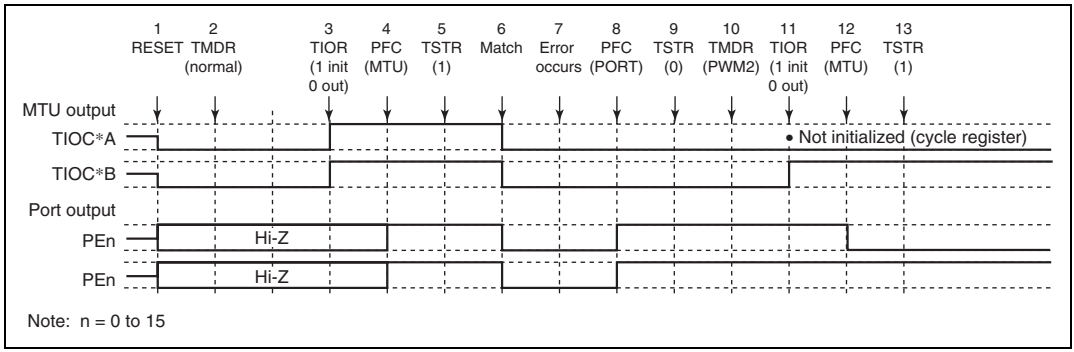

Figure 10.62 Error Occurrence in Normal Mode, Recovery in PWM Mode 2

1 to 9 are the same as in figure 10.60.

10. Set PWM mode 2.
11. Initialize the pins with TIOR. (In PWM mode 2, the cycle register pins are not initialized. If initialization is required, initialize in normal mode, then switch to PWM mode 2.)
12. Set MTU output with the PFC.
13. Operation is restarted by TSTR.

Bit Rate (Bits/s)	φ (MHz)								
	7.3728			8			9.8304		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	130	–0.07	2	141	0.03	2	174	–0.26
150	2	95	0.00	2	103	0.16	2	127	0.00
300	1	191	0.00	1	207	0.16	1	255	0.00
600	1	95	0.00	1	103	0.16	1	127	0.00
1200	0	191	0.00	0	207	0.16	0	255	0.00
2400	0	95	0.00	0	103	0.16	0	127	0.00
4800	0	47	0.00	0	51	0.16	0	63	0.00
9600	0	23	0.00	0	25	0.16	0	31	0.00
14400	0	15	0.00	0	16	2.12	0	20	1.59
19200	0	11	0.00	0	12	0.16	0	15	0.00
28800	0	7	0.00	0	8	–3.55	0	10	–3.03
31250	0	6	5.33	0	7	0.00	0	9	–1.70
38400	0	5	0.00	0	6	–6.99	0	7	0.00

Bit Rate (Bits/s)	φ (MHz)								
	10			11.0592			12		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	177	–0.25	2	195	0.19	2	212	0.03
150	2	129	0.16	2	143	0.00	2	155	0.16
300	2	64	0.16	2	71	0.00	2	77	0.16
600	1	129	0.16	1	143	0.00	1	155	0.16
1200	1	64	0.16	1	71	0.00	1	77	0.16
2400	0	129	0.16	0	143	0.00	0	155	0.16
4800	0	64	0.16	0	71	0.00	0	77	0.16
9600	0	32	–1.36	0	35	0.00	0	38	0.16
14400	0	21	–1.36	0	23	0.00	0	25	0.16
19200	0	15	1.73	0	17	0.00	0	19	–2.34
28800	0	10	–1.36	0	11	0.00	0	12	0.16
31250	0	9	0.00	0	10	0.54	0	11	0.00
38400	0	7	1.73	0	8	0.00	0	9	–2.34

Table 12.6 Maximum Bit Rates during External Clock Input (Asynchronous Mode)

ϕ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (Bits/s)
4	1.0000	62500
4.9152	1.2288	76800
6	1.5000	93750
7.3728	1.8432	115200
8	2.0000	125000
9.8304	2.4576	153600
10	2.5000	156250
11.0592	2.7648	172800
12	3.0000	187500
12.288	3.0720	192000
14	3.5000	218750
14.7456	3.6864	230400
16	4.0000	250000
17.2032	4.3008	268800
18	4.5000	281250
18.432	4.6080	288000
19.6608	4.9152	307200
20	5.0000	312500
22	5.5000	343750
22.1184	5.5296	345600
24	6.0000	375000
24.576	6.1440	384000
25.8048	6.4512	403200
26	6.5000	406250
27.0336	6.7584	422400
28	7.0000	437500

14.1.2 Block Diagram

Figure 14.1 is the block diagram of the mid-speed A/D converter.

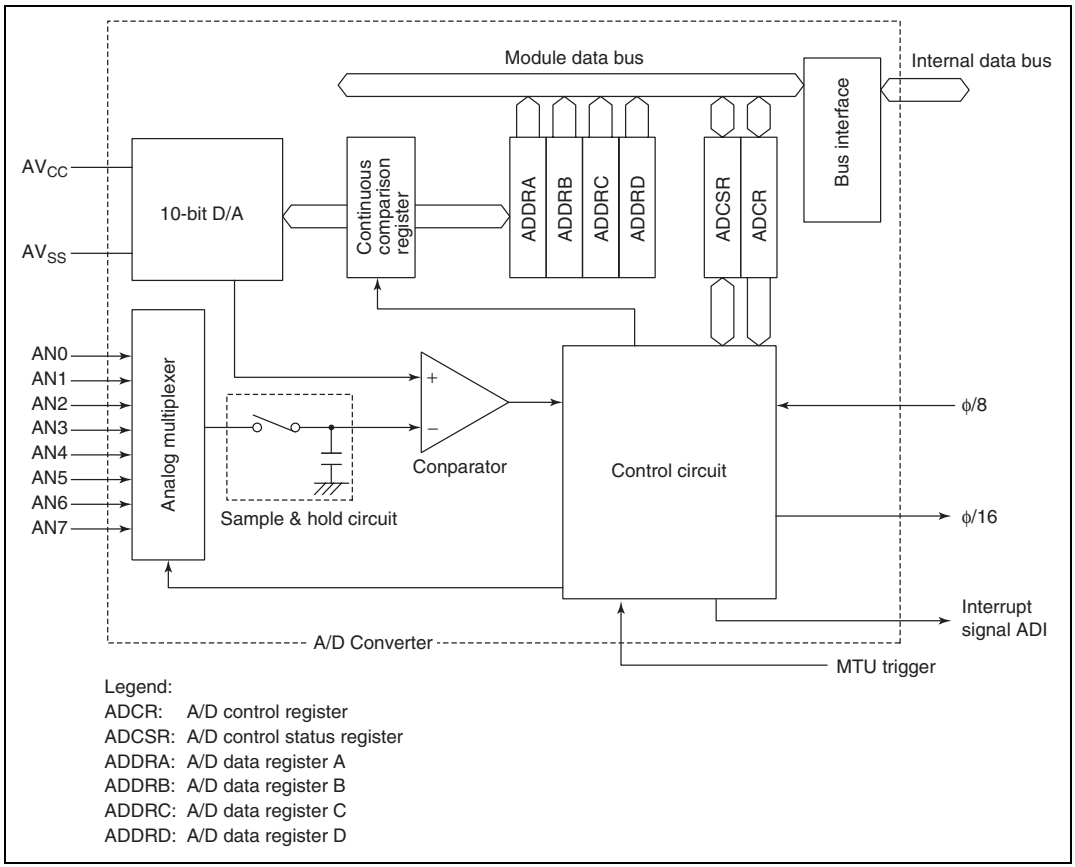

Figure 14.1 Mid-speed A/D converter block diagram

18.11.1 Socket Adapter Pin Correspondence Diagram

Connect the socket adapter to the chip as shown in figure 18.19. This will enable conversion to a 32-pin arrangement. The on-chip ROM memory map is shown in figure 18.18, and the socket adapter pin correspondence diagram in figure 18.19.

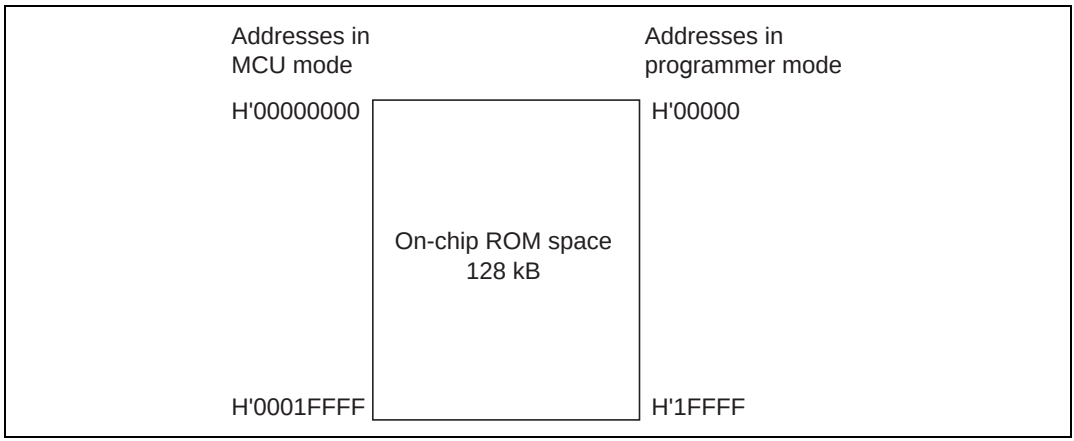

Figure 18.18 On-Chip ROM Memory Map

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFF8348	IPRA									INTC
H'FFFF8349										
H'FFFF834A	IPRB									
H'FFFF834B										
H'FFFF834C	IPRC									
H'FFFF834D										
H'FFFF834E	IPRD									
H'FFFF834F										
H'FFFF8350	IPRE									
H'FFFF8351										
H'FFFF8352	IPRF									
H'FFFF8353										
H'FFFF8354	IPRG									
H'FFFF8355										
H'FFFF8356	IPRH									
H'FFFF8357										
H'FFFF8358	ICR	NMIL	—	—	—	—	—	—	NMIE	
H'FFFF8359		IRQ0S	IRQ1S	IRQ2S	IRQ3S	—	—	IRQ6S	IRQ7S	
H'FFFF835A	ISR	—	—	—	—	—	—	—	—	
H'FFFF835B		IRQ0F	IRQ1F	IRQ2F	IRQ3F	—	—	IRQ6F	IRQ7F	
H'FFFF835C to H'FFFF8381	—	—	—	—	—	—	—	—	—	
H'FFFF8382	PADRL	PA15DR	PA14DR*[1]	PA13DR*[1]	PA12DR*[1]	PA11DR*[1]	PA10DR*[1]	PA9DR	PA8DR	I/O
H'FFFF8383		PA7DR	PA6DR	PA5DR	PA4DR	PA3DR	PA2DR	PA1DR	PA0DR	
H'FFFF8384	—	—	—	—	—	—	—	—	—	PFC
H'FFFF8385	—	—	—	—	—	—	—	—	—	
H'FFFF8386	PAIORL	PA15IOR	PA14IOR*[1]	PA13IOR*[1]	PA12IOR*[1]	PA11IOR*[1]	PA10IOR*[1]	PA9IOR*[1]	PA8IOR*[1]	
H'FFFF8387		PA7IOR	PA6IOR	PA5IOR	PA4IOR	PA3IOR	PA2IOR	PA1IOR	PA0IOR	
H'FFFF8388	—	—	—	—	—	—	—	—	—	
H'FFFF8389	—	—	—	—	—	—	—	—	—	

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFF86B0	DMAOR	—	—	—	—	—	—	—	—	DMAC
H'FFFF86B1		—	—	—	—	—	AE	NMIF	DME	
H'FFFF86B2 to H'FFFF86BF	—	—	—	—	—	—	—	—	—	
H'FFFF86C0	SAR0									
H'FFFF86C1										
H'FFFF86C2										
H'FFFF86C3										
H'FFFF86C4	DAR0									
H'FFFF86C5										
H'FFFF86C6										
H'FFFF86C7										
H'FFFF86C8	DMATCR0									
H'FFFF86C9										
H'FFFF86CA										
H'FFFF86CB										
H'FFFF86CC	CHCR0	—	—	—	—	—	—	—	—	
H'FFFF86CD		—	—	—	—	—	RL	AM	AL	
H'FFFF86CE		DM1	DM0	SM1	SM0	RS3	RS2	RS1	RS0	
H'FFFF86CF		—	DS	TM	TS1	TS0	IE	TE	DE	
H'FFFF86D0	SAR1									
H'FFFF86D1										
H'FFFF86D2										
H'FFFF86D3										
H'FFFF86D4	DAR1									
H'FFFF86D5										
H'FFFF86D6										
H'FFFF86D7										
H'FFFF86D8	DMATCR1									
H'FFFF86D9										
H'FFFF86DA										
H'FFFF86DB										
H'FFFF86DC	CHCR1	—	—	—	—	—	—	—	—	
H'FFFF86DD		—	—	—	—	—	RL	AM	AL	
H'FFFF86DE		DM1	DM0	SM1	SM0	RS3	RS2	RS1	RS0	
H'FFFF86DF		—	DS	TM	TS1	TS0	IE	TE	DE	

Address	Register Abbr.	Bit Names								Module
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
H'FFFF87E0 to H'FFFF873F	—	—	—	—	—	—	—	—	—	—
H'FFFF8740	CCR	—	—	—	—	—	—	—	—	CAC
H'FFFF8741		—	—	—	CEDRAM	CECS3	CECS2	CECS1	CECS0	
H'FFFF8742 to H'FFFF87FF	—	—	—	—	—	—	—	—	—	

Notes: 1. Reserved bit in the SH7014.
2. In the SH7014, this address is reserved and must not be accessed.
3. Write address.
4. Read address. For details, see section 13.2.4, Notes on Register Access, in section 13, Watchdog Timer.

MTU

Bit	Name	Value				Description		
3 to 0	I/O Control A3 to A0 (IOA3 to IOA0)	0	0	0	0	TGR0A is an output compare register	Output disabled	(initial value)
					1		Initial output is 0	Output 0 on compare-match
				1	0			Output 1 on compare-match
					1			Toggle output on compare-match
			1	0	0		Output disabled	
					1		Initial output is 1	Output 0 on compare-match
				1	0			Output 1 on compare-match
					1			Toggle output on compare-match
		1	0	0	0	TGR0A is an input capture register	Capture input source is the TIOC0A pin	Input capture on rising edge
					1			Input capture on falling edge
				1	0			Input capture on both edges
					1			
			1	0	0		Capture input source is channel 1/ count clock	Input capture on TCNT1 count up/count down
					1			
				1	0			
					1			

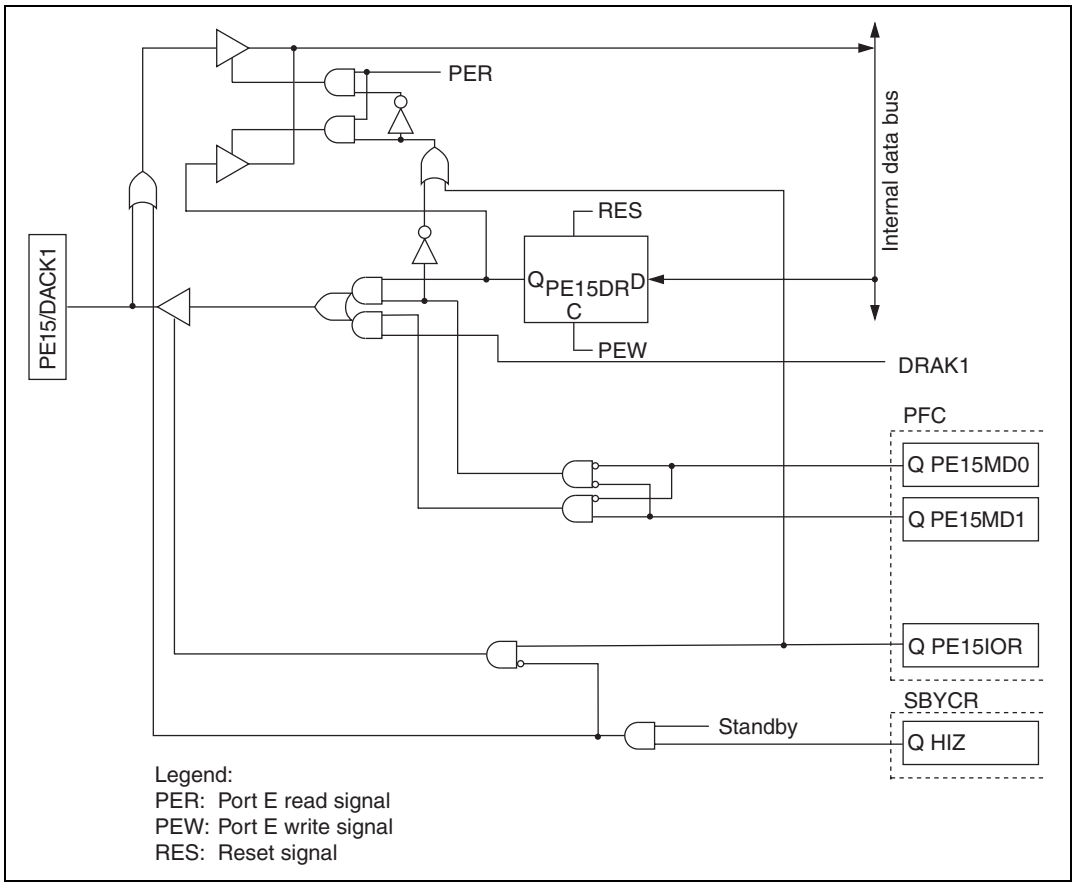

Figure B.21 PE15/DACK1 Block Diagram