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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	28MHz
Connectivity	EBI/EMI, SCI
Peripherals	DMA, PWM, WDT
Number of I/O	35
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	3K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	112-BQFP
Supplier Device Package	112-QFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd6417014rf28v

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Instruction		Instruction Code	Operation	Exec. Cycles	T Bit
SUB	Rm,Rn	0011nnnnmmmm1000	Rn – Rm → Rn	1	—
SUBC	Rm,Rn	0011nnnnmmmm1010	Rn – Rm – T → Rn, Borrow → T	1	Borrow
SUBV	Rm,Rn	0011nnnnmmmm1011	Rn – Rm → Rn, Underflow → T	1	Overflow

Note: * The normal minimum number of execution cycles. (The number in parentheses is the number of cycles when there is contention with following instructions.)

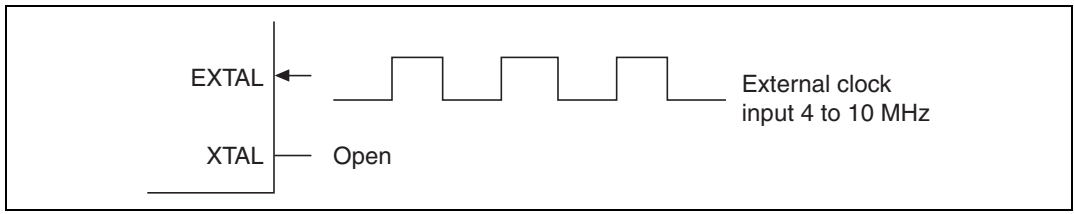

Figure 4.6 Example of External Clock Connection

4.3 Prescaler

The prescaler divides the system clock (ϕ) to generate an internal clock (ϕ/2 to ϕ/8192) for supply to peripheral modules.

Address Modes

Single Address Mode: In the single address mode, both the transfer source and destination are external; one (selectable) is accessed by a DACK signal while the other is accessed by an address. In this mode, the DMAC performs the DMA transfer in 1 bus cycle by simultaneously outputting a transfer request acknowledge DACK signal to one external device to access it while outputting an address to the other end of the transfer. Figure 9.3 shows an example of a transfer between an external memory and an external device with DACK in which the external device outputs data to the data bus while that data is written in external memory in the same bus cycle.

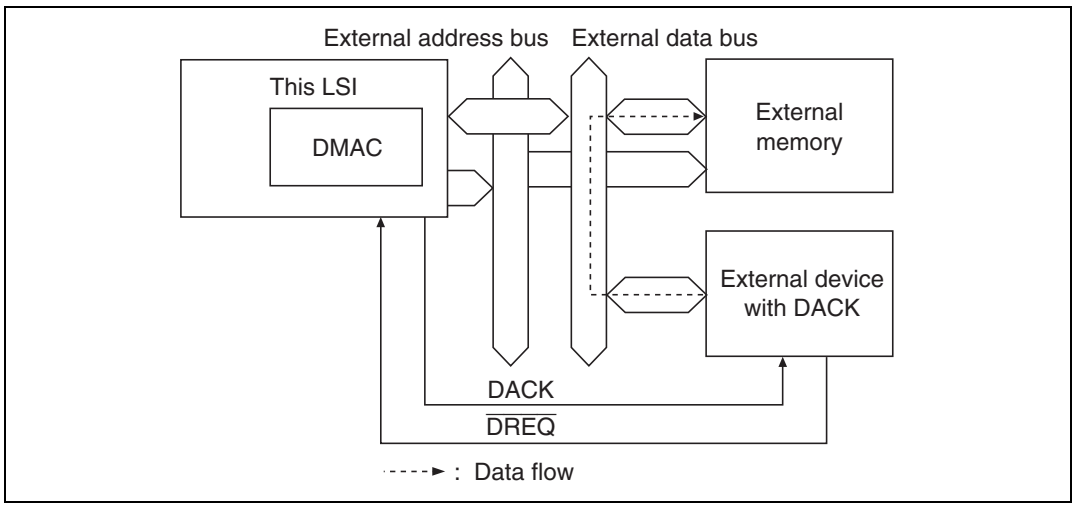

Figure 9.3 Data Flow in Single Address Mode

Two types of transfers are possible in the single address mode: (a) transfers between external devices with DACK and memory-mapped external devices, and (b) transfers between external devices with DACK and external memory. The only transfer requests for either of these is the external request ($\overline{\text{DREQ}}$). Figure 9.4 shows the DMA transfer timing for the single address mode.

10.2.7 Timer General Register (TGR)

Each timer general register (TGR) is a 16-bit register that can function as either an output compare register or an input capture register. There are a total of eight TGR, four for channel 0, and two each for channels 1 and 2. The TGRC and TGRD of channel 0 can be set to operate as buffer registers. The TGR register and buffer register combinations are TGRA with TGRC, and TGRB with TGRD.

The TGRs are initialized to H'FFFF by a power-on reset or in standby mode. Accessing of the TGRs in 8-bit units is disabled; they may only be accessed in 16-bit units.

Bit:	15	14	13	12	11	10	9	8
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

10.2.8 Timer Start Register (TSTR)

The timer start register (TSTR) is an 8-bit read/write register that starts and stops the timer counters (TCNT) of channels 0 to 2. TSTR is initialized to H'00 upon power-on reset or standby mode.

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	CST2	CST1	CST0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

PWM Mode Operation Examples—PWM Mode 2 (Figure 10.25): Channels 0 and 1 are set for synchronous operation, TGR1B register compare-match is used as a TCNT counter clear source, the other TGR register initial output value is 0 and output compare output value is 1, and a 5-phase PWM waveform is output. In this example, the value established in the TGR1B register becomes the period and the value established in the other TGR register becomes the duty cycle.

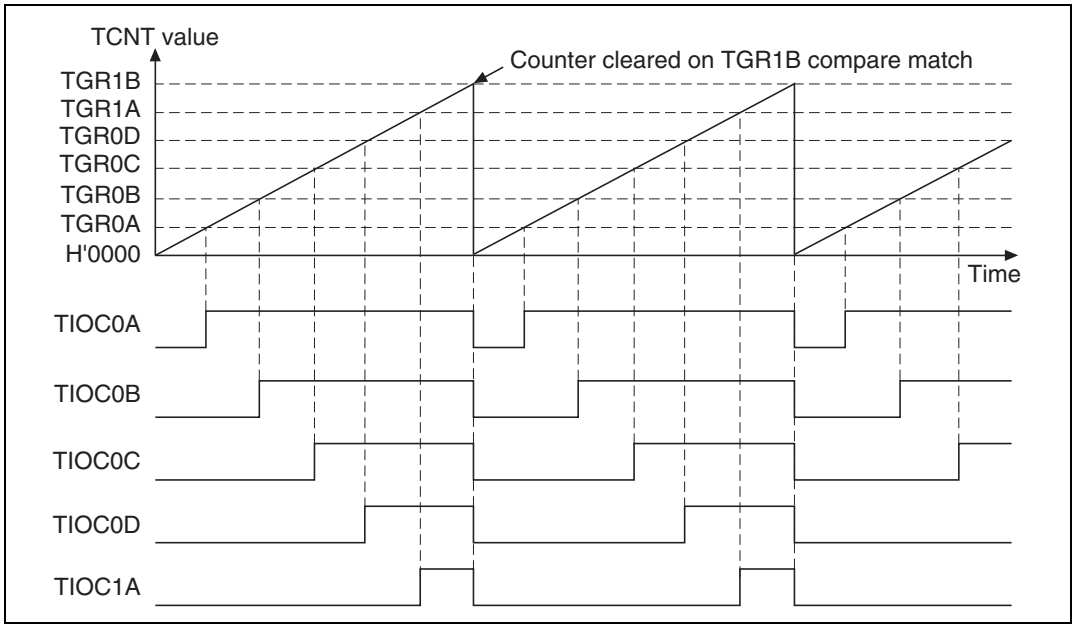

Figure 10.25 PWM Mode Operation Example (Mode 2)

0% Duty Cycle: Figure 10.26 shows an example of a 0% duty cycle PWM waveform output in PWM mode.

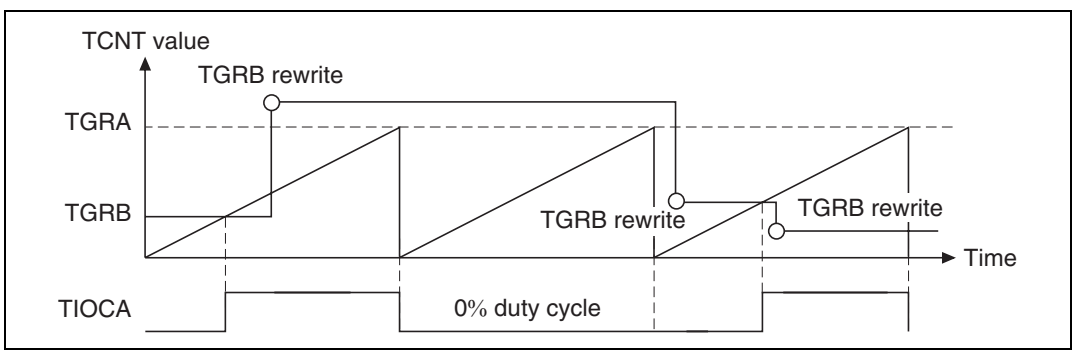

Figure 10.26 PWM Mode Operation Example (0% Duty Cycle)

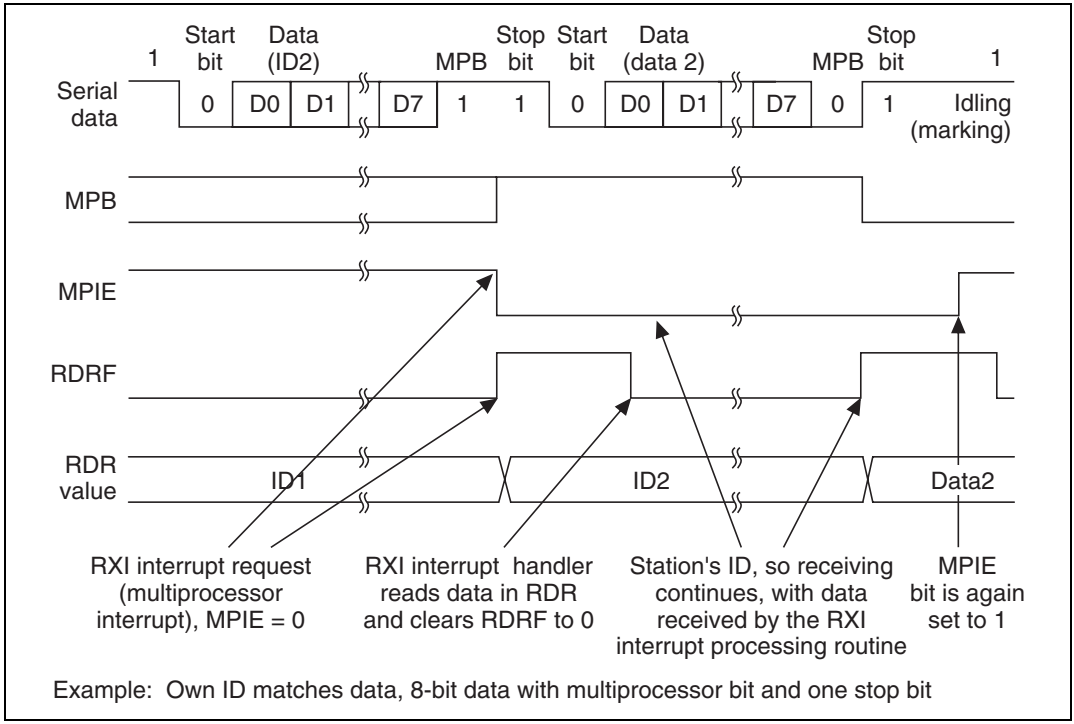

Figure 12.13 Example of SCI Receive Operation (ID Matches) (2)

12.3.4 Clock Synchronous Operation

In the clock synchronous mode, the SCI transmits and receives data in synchronization with clock pulses. This mode is suitable for high-speed serial communication.

The SCI transmitter and receiver are independent, so full duplex communication is possible while sharing the same clock. The transmitter and receiver are also double buffered, so continuous transmitting or receiving is possible by reading or writing data while transmitting or receiving is in progress.

Figure 12.14 shows the general format in clock synchronous serial communication.

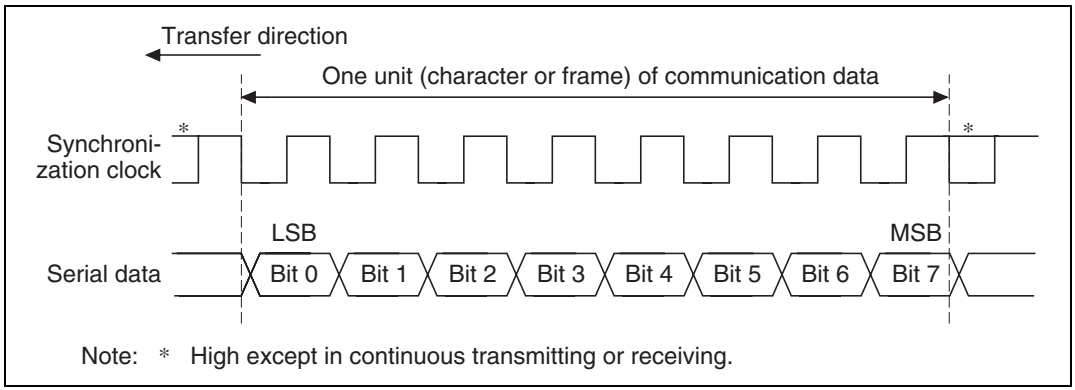

Figure 12.14 Data Format in Clock Synchronous Communication

In clock synchronous serial communication, each data bit is output on the communication line from one falling edge of the serial clock to the next. Data are guaranteed valid at the rising edge of the serial clock. In each character, the serial data bits are transmitted in order from the LSB (first) to the MSB (last). After output of the MSB, the communication line remains in the state of the MSB. In the clock synchronous mode, the SCI transmits or receives data by synchronizing with the falling edge of the synchronization clock.

Communication Format: The data length is fixed at eight bits. No parity bit or multiprocessor bit can be added.

Clock: An internal clock generated by the on-chip baud rate generator or an external clock input from the SCK pin can be selected as the SCI transmit/receive clock. The clock source is selected by the C/$\overline{A}$ bit in the serial mode register (SMR) and bits CKE1 and CKE0 in the serial control register (SCR). See table 12.9.

When the SCI operates on an internal clock, it outputs the clock signal at the SCK pin. Eight clock pulses are output per transmitted or received character. When the SCI is not transmitting or receiving, the clock signal remains in the high state.

Note: An overrun error occurs only during the receive operation, and the sync clock is output until the RE bit is cleared to 0. When you want to perform a receive operation in one-character units, select external clock for the clock source.

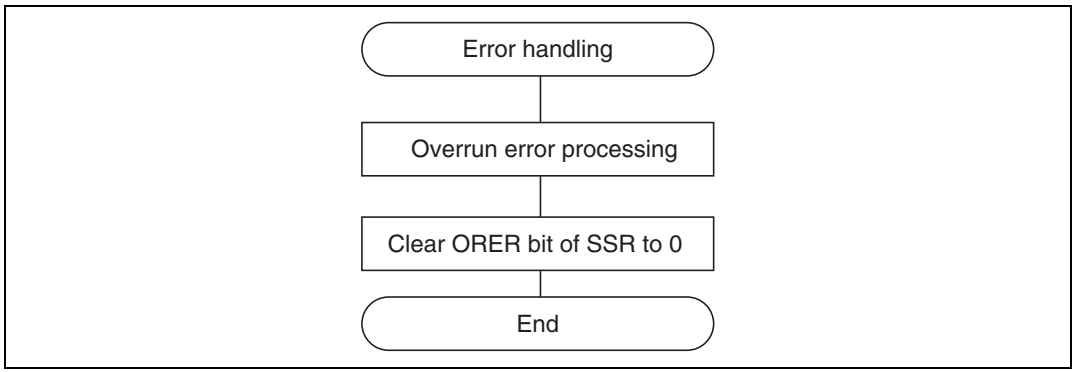

Figure 12.18 Sample Flowchart for Serial Receiving (2)

Figure 12.19 shows an example of the SCI receive operation.

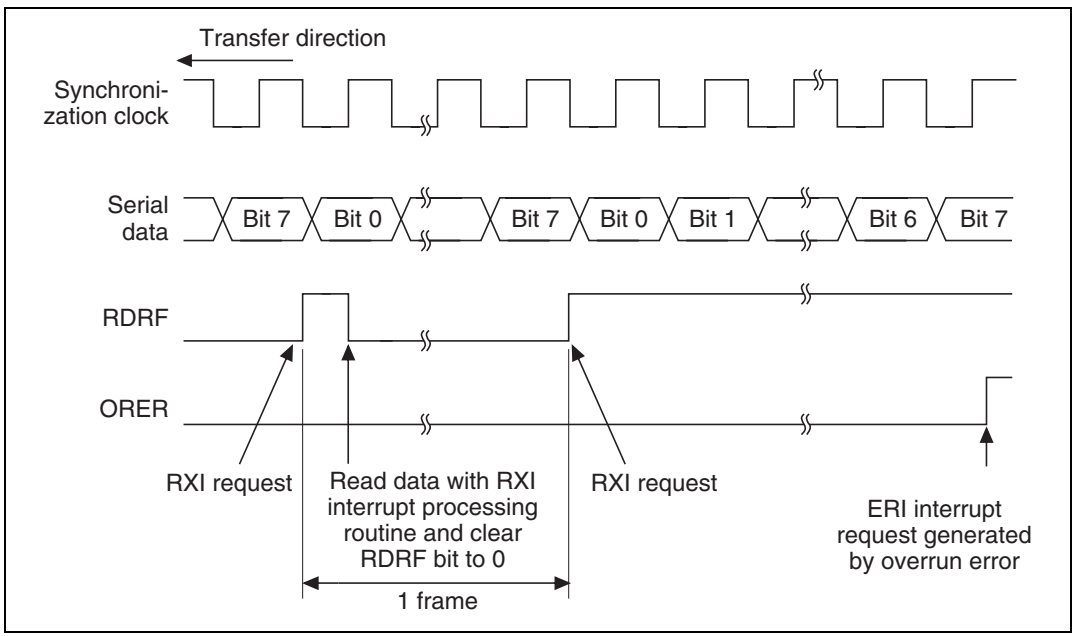

Figure 12.19 Example of SCI Receive Operation

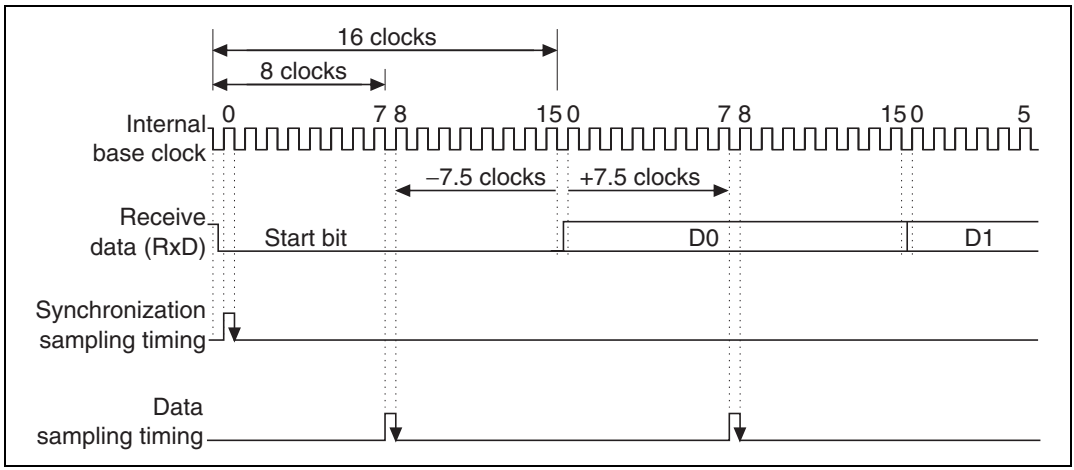

Figure 12.21 Receive Data Sampling Timing in Asynchronous Mode

The receive margin in the asynchronous mode can therefore be expressed as:

$$M = \left| \left(0.5 - \frac{1}{2N}\right) - (L - 0.5)F - \frac{|D - 0.5|}{N}(1 + F) \right| \times 100\ \%$$

Legend:
M : Receive margin (%)
N : Ratio of clock frequency to bit rate (N = 16)
D : Clock duty cycle (D = 0 – 1.0)
L : Frame length (L = 9 – 12)
F : Absolute deviation of clock frequency

From the equation above, if F = 0 and D = 0.5 the receive margin is 46.875%:

D = 0.5, F = 0
M = $(0.5 - 1/(2 \times 16)) \times 100\%$
= 46.875%

This is a theoretical value. A reasonable margin to allow in system designs is 20 to 30%.

16.3.6 Port C Control Register (PCCR) — SH7016, SH7017 —

Bit:	15	14	13	12	11	10	9	8
	PC15 MD	PC14 MD	PC13 MD	PC12 MD	PC11 MD	PC10 MD	PC9 MD	PC8 MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	PC7 MD	PC6 MD	PC5 MD	PC4 MD	PC3 MD	PC2 MD	PC1 MD	PC0 MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PCCR is a 16-bit read/write register that selects the functions for the sixteen port C multiplexed pins. There are instances when these register settings will be ignored, depending on the operation mode. Refer to table 16.3, Pin Arrangement by Mode, for details.

PCCR is initialized to H'0000 by power-on resets but is not initialized for reset by WDT, standby mode, or sleep mode, so the previous data is maintained.

The settings in this register are functional only in the SH7016 and SH7017. In the SH7014, there are no pins corresponding to this register, and it should not be read or written to.

Bit 15—PC15 Mode (PC15MD): Selects the function of the PC15/A15 pin.

Bit 15 PC15MD	Description	
0	General input/output (PC15) (A15 in on-chip ROM invalid mode)	(initial value)
1	Address output (A15) (PC15 in single chip mode)	

16.3.8 Port D Control Register L (PDCRL) — SH7016, SH7017 —

Bit:	15	14	13	12	11	10	9	8
	PD15 MD	PD14 MD	PD13 MD	PD12 MD	PD11 MD	PD10 MD	PD9 MD	PD8 MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	7	6	5	4	3	2	1	0
	PD7 MD	PD6 MD	PD5 MD	PD4 MD	PD3 MD	PD2 MD	PD1 MD	PD0 MD
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

PDCRL is a 16-bit read/write register that selects the multiplexed pin functions for the least significant sixteen port D pins. There are instances when these register settings will be ignored, depending on the operation mode.

On-Chip ROM-Disabled Extended Mode:

— Mode 0 (8-bit bus): Port D pins are data I/O pins; PDCRL settings are disabled.
— Mode 1 (16-bit bus): Port D pins are data I/O pins; PDCRL settings are disabled.

On-Chip ROM-Enabled Extended Mode: The port D pins are shared as data I/O pins and general I/O pins; PDCRL settings are enabled.

Single Chip Mode: The port D pins are general I/O pins; PDCRL settings are disabled.

PDCRL is initialized to H'0000 by external power-on reset but is not initialized for reset by WDT, standby mode, or sleep mode, so the previous data is maintained.

The settings in this register are functional only in the SH7016 and SH7017. In the SH7014, there are no pins corresponding to this register, and it should not be read or written to.

```
        MOV.B   R0,@(FLMCR1,GBR)    ; Clear SWE
;
        RTS
        NOP
;
        .ALIGN  4
PdataBuff       .RES.B  32
```

18.7.3 Erase Mode

When erasing flash memory, the erase/erase-verify flowchart shown in figure 18.14 should be followed.

To perform data or program erasure, set the 1 bit flash memory area to be erased in erase block register 1 (EBR1) at least 10 µs after setting the SWE bit to 1 in flash memory control register 1 (FLMCR1). Next, the watchdog timer is set to prevent overerasing in the event of program runaway, etc. Set 9.2 ms as the WDT overflow period. After this, preparation for erase mode (erase setup) is carried out by setting the ESU bit in FLMCR1, and after the elapse of 200 µs or more, the operating mode is switched to erase mode by setting the E bit in FLMCR1. The time during which the E bit is set is the flash memory erase time. Ensure that the erase time does not exceed 5 ms.

Note: With flash memory erasing, preprogramming (setting all memory data in the memory to be erased to all “0”) is not necessary before starting the erase procedure.

- Sample one-block erase program

  The wait time set values (number of loops) are for the case where f = 28.7 MHz. For other frequencies, the set value is given by the following expression:

  Wait time (μs) × f (MHz) ÷ 4

  The WDT overflow cycle set value is for the case where f = 28.7 MHz. For other frequencies, ensure that the overflow cycle is a minimum of 5.3 ms.

Registers Used

R5 (input): Memory block table pointer
R7 (output): OK (normal) or NG (error)
R0 to R3, R6, R8 and R9: Work registers

```
FLMCR1              .EQU     H'80
FLMCR2              .EQU     H'81
EBR1                .EQU     H'82
EBR2                .EQU     H'83
Wait10u             .EQU     72
Wait2u              .EQU     14
Wait200u            .EQU     1435
Wait5m              .EQU     35875
Wait20u             .EQU     144
Wait5u              .EQU     36
WDT_TCSR            .EQU     H'FFFF8610
WDT_9m              .EQU     H'A57D
SWESET              .EQU     B'01000000
ESUSET              .EQU     B'00100000
ESET                .EQU     B'00000010
ECLEAR              .EQU     B'11111101
ESUCLEAR            .EQU     B'11011111
EVSET               .EQU     B'00001000
EVCLEAR             .EQU     B'11110111
SWECLEAR            .EQU     B'10111111
MAXErase            .EQU     60
;
FlashErase          .EQU     $
        MOV.L       #H'FFFF8500,R0
        LDC         R0,GBR                  ; Initialize GBR
        MOV.L       #1,R2
```

```
;
        MOV.L     #Wait10u,R3
        MOV.L     #FLMCR1,R0
        OR.B      #SWESET,@(R0,GBR)    ; Set SWE
EWait_1 SUBC      R2,R3                ; Wait 10 µs
        BF        EWait_1
;
        MOV.L     #0,R9                ; Initialize n (R9) to 0
;
        MOV.B     @(6,R5),R0
        MOV.B     R0,@(EBR1,GBR)       ; Erase memory block (EBR1) setting
        MOV.B     @(7,R5),R0
        MOV.B     R0,@(EBR2,GBR)       ; Erase memory block (EBR2) setting
;
        MOV.L     #FLMCR1,R0
        MOV.L     @R5,R6               ; Erase memory block start address -> R6
        MOV.L     #H'020000,R7
        CMP/GT    R6,R7
        BT        EraseLoop
        MOV.L     #FLMCR2,R0
;
EraseLoop         .EQU     $
        MOV.L     #WDT_TCSR,R1         ; Enable WDT
        MOV.W     #WDT_9m,R3           ; 9.2 ms cycle
        MOV.W     R3,@R1
;
        MOV.L     #Wait200u,R3
        OR.B      #ESUSET,@(R0,GBR)    ; Set ESU
EWait_2 SUBC      R2,R3                ; Wait 200 µs
        BF        EWait_2
;
        MOV.L     #Wait5m,R3
        OR.B      #ESET,@(R0,GBR)      ; Set E
EWait_3 SUBC      R2,R3                ; Wait 5 ms
        BF        EWait_3
;
        MOV.L     #Wait10u,R3
        AND.B     #ECLEAR,@(R0,GBR)    ; Clear E
```

22.4 A/D Converter Characteristics

Tables 22.15 and 22.16 show A/D converter characteristics for the HD6417014 and HD6417014R, and table 22.17 shows A/D converter characteristics for the SH7016 and SH7017. The HD6417014R has an absolute error of ±8 LSB or less.

Table 22.15 A/D Converter Characteristics (HD6417014)

Conditions: V_{CC} = 5.0 V ±10%, AV_{CC} = 5.0 V ±10%, AV_{CC} = V_{CC} ±10%, V_{SS} = AV_{SS} = 0 V, Ta = –20 to +75°C

	28.7MHz			
Item	**Min**	**Typ**	**Max**	**Unit**
Resolution	10	10	10	Bits
Conversion time*[1]	—	—	2.9	µs
Analog input capacitance	—	—	20	pF
Permitted signal source impedance	—	—	1	kΩ
Non-linear error*[2]	—	—	±8	LSB
Offset error*[2]	—	—	±8	LSB
Full-scale error*[2]	—	—	±8	LSB
Quantization error*[2]	—	—	±0.5	LSB
Absolute error*[1]	—	—	±15	LSB

Notes: 1. CKS = 1
2. Reference values

PFC

Port A Control Register L2 (PACRL2)	H'FFFF838E H'FFFF838F	8/16/32

Item	Bit							
	15	14	13	12	11	10	9	8
Bit name	PA7MD1	PA7MD0	PA6MD1	PA6MD0	PA5MD1	PA5MD0	—	PA4MD
Initial value	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Item	7	6	5	4	3	2	1	0
Bit name	—	PA3MD	PA2MD1	PA2MD0	—	PA1MD	—	PA0MD
Initial value	0	0	0	0	0	0	0	0
R/W	R	R/W	R/W	R/W	R	R/W	R	R/W

Bit	Name	Value		Description
15, 14	PA7 Mode 1, 0 (PA7MD1 and PA7MD0)	0	0	General input/output (PA7) (initial value)
			1	MTU timer clock input (TCLKB)
		1	0	Chip select output ($\overline{CS3}$) (PA7 in single-chip mode)
			1	Reserved
13, 12	PA6 Mode 1, 0 (PA6MD1 and PA6MD0)	0	0	General input/output (PA6) (initial value)
			1	MTU timer clock input (TCLKA)
		1	0	Chip select output ($\overline{CS2}$) (PA6 in single-chip mode)
			1	Reserved
11, 10	PA5 Mode 1, 0 (PA5MD1 and PA5MD0)	0	0	General input/output (PA5) (initial value)
			1	Serial clock input/output (SCK1)
		1	0	DMA transfer request received input ($\overline{DREQ1}$) (PA5 in single-chip mode)
			1	Interrupt request input ($\overline{IRQ1}$)
8	PA4 Mode (PA4MD)	0		General input/output (PA4) (initial value)
		1		Transmit data output (TxD1)
6	PA3 Mode (PA3MD)	0		General input/output (PA3) (initial value)
		1		Receive data input (RxD1)
5, 4	PA2 Mode 1, 0 (PA2MD1 and PA2MD0)	0	0	General input/output (PA2) (initial value)
			1	Serial clock input/output (SCK0)
		1	0	DMA transfer request received input ($\overline{DREQ0}$) (PA2 in single-chip mode)
			1	Interrupt request input ($\overline{IRQ0}$)

Table C.3 Pin Settings for Normal External Space

		Normal External Space			
			16-Bit Space		
Pin Name		**8-Bit Space**	**Upper Word**	**Lower Word**	**Word/Longword**
$\overline{CS0}$ to $\overline{CS2}$		Valid	Valid	Valid	Valid
$\overline{CS3}$		H	H	H	H
$\overline{RAS}$*1		H	H	H	H
$\overline{CASH}$*2		H	H	H	H
$\overline{CASL}$*2		H	H	H	H
RDWR		H	H	H	H
$\overline{AH}$		L	L	L	L
$\overline{RD}$	R	L	L	L	L
	W	H	H	H	H
$\overline{WRH}$	R	H	H	H	H
	W	H	L	H	L
$\overline{WRL}$	R	H	H	H	H
	W	L	H	L	L
A21 to A0		Address	Address	Address	Address
D15 to D8		Hi-Z	Data	Hi-Z	Data
D7 to D0		Data	Hi-Z	Data	Data

Legend:

R: Read

W: Write

Valid: Chip select signal corresponding with accessed area is low; chip select signal in other cases is high.

Notes: 1. L asserted in RAS down state or refresh state.

2. L asserted in refresh state.