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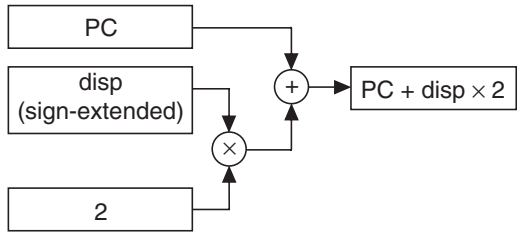
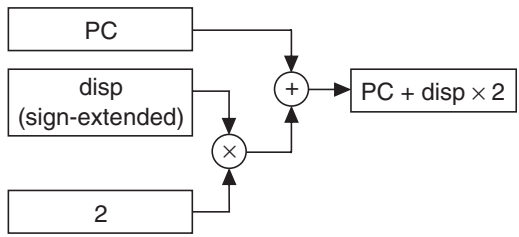
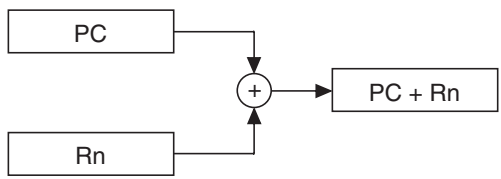
## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | SH-2 |
| Core Size | 32-Bit Single-Core |
| Speed | 28.7MHz |
| Connectivity | EBI/EMI, SCI |
| Peripherals | DMA, PWM, WDT |
| Number of I/O | 74 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 75°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 112-BQFP |
| Supplier Device Package | 112-QFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f7017f28v |

| Item | Page | Revision (See Manual for Details) |
|---|---|---|
| 9.3.6 DMA Transfer Ending Conditions<br>Conditions for Ending All Channels Simultaneously: | 187 | Description amended<br>When the processing of a one unit transfer is complete. In a dual address mode direct address transfer, even if an address error occurs or the NMI flag is set during read processing, the transfer will not be halted until after completion of the following write processing. In such a case, SAR, DAR, and DMATCR values are updated. |
| 9.4.2 Example of DMA Transfer between External RAM and External Device with DACK | 189 | Description amended<br>In this example, an external request, single address mode transfer with external memory as the transfer source and an external device with DACK as the transfer destination is executed using DMAC channel 1. |
| 10.1.1 Features | 191 | Description amended<br>— PWM mode: PWM output can be provided with any duty cycle. When combined with the counter synchronizing function, up to seven-phase PWM output is enabled (with channels 0 to 2 set to PWM mode 2 and channel 0 synchronized with the TGR0A register (channels 0 to 2 phase output: 3, 2, 2)). |
| 10.1.4 Register Configuration<br>Table 10.3 Register Configuration | 198 | Notes amended<br>Notes: Do not access empty addresses.<br>1. 16-bit registers (TCNT, TGR) cannot be read or written in 8-bit units.<br>2. Write 0 to clear flags. |
| 10.2.4 Timer Interrupt Enable Register (TIER)<br>Bit 5—Underflow Interrupt Enable (TCIEU) | 215 | Description amended<br>This bit is reserved for channel 0. It always reads as 0. The write value should always be 0. |
| Bit 3—TGR Interrupt Enable D (TGIED): | 216 | Description amended<br>This bit is reserved for channels 1 and 2. It always reads as 0. The write value should always be 0. |
| Bit 2—TGR Interrupt Enable C (TGIEC): | | Description amended<br>This bit is reserved for channels 1 and 2. It always reads as 0. The write value should always be 0. |
| 10.2.5 Timer Status Register (TSR) | 217 | Description amended<br>The timer status register (TSR) is an 8-bit register that indicates the status of each channel. The MTU has three TSR registers, one each for channel. TSR is initialized to H'C0 by a power-on reset or by standby mode. |

| Addressing Mode | Instruction Format | Effective Addresses Calculation | Equation |
|---|---|---|---|
| PC relative addressing | `disp:8` | The effective address is the PC value sign-extended with an 8-bit displacement (disp), doubled, and added to the PC value.<br>  | PC + disp × 2 |
| | `disp:12` | The effective address is the PC value sign-extended with a 12-bit displacement (disp), doubled, and added to the PC value.<br>  | PC + disp × 2 |
| | `Rn` | The effective address is the register PC value plus Rn.<br>  | PC + Rn |
| Immediate addressing | `#imm:8` | The 8-bit immediate data (imm) for the TST, AND, OR, and XOR instructions are zero-extended. | — |
| | `#imm:8` | The 8-bit immediate data (imm) for the MOV, ADD, and CMP/EQ instructions are sign-extended. | — |
| | `#imm:8` | The 8-bit immediate data (imm) for the TRAPA instruction is zero-extended and is quadrupled. | — |

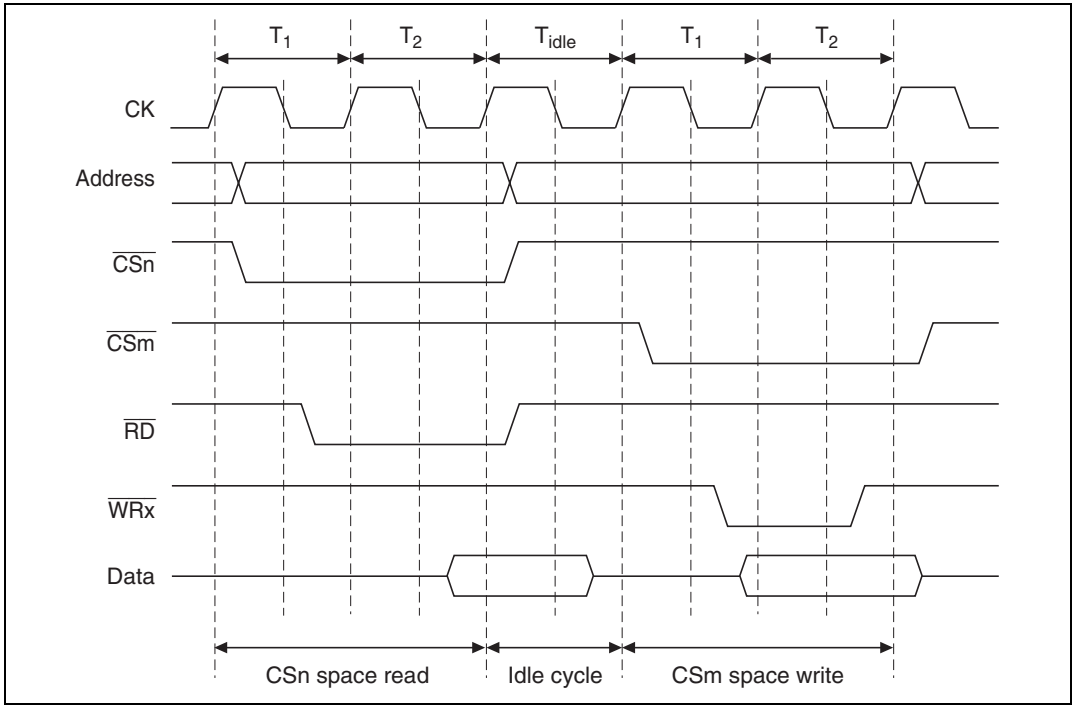



**Figure 8.20 Idle Cycle Insertion Example**

IW31 and IW30 specify the number of idle cycles required after a CS3 space read either to read other external spaces, or for this LSI, to do write accesses. In the same manner, IW21 and IW20 specify the number of idle cycles after a CS2 space read, IW11 and IW10, the number after a CS1 space read, and IW01 and IW00, the number after a CS0 space read.

DIW specifies the number of idle cycles required, after a DRAM space read either to read other external spaces (CS space), or for this LSI, to do write accesses.

0 to 3 cycles can be specified for CS space, and 0 to 1 cycle for DRAM space.

**Bits 13 and 12—Source Address Mode 1, 0 (SM1 and SM0):** These bits specify increment/decrement of the DMA transfer source address. These bit specifications are ignored when transferring data from an external device to address space in single address mode.

| Bit 13 SM1 | Bit 12 SM0 | Description |
|---|---|---|
| 0 | 0 | Source address fixed (initial value) |
| | 1 | Source address incremented (+1 during 8-bit transfer, +2 during 16-bit transfer, +4 during 32-bit transfer) |
| 1 | 0 | Source address decremented (–1 during 8-bit transfer, –2 during 16-bit transfer, –4 during 32-bit transfer) |
| | 1 | Setting prohibited |

**Bits 11 to 8—Resource Select 3 to 0 (RS3 to RS0):** These bits specify the transfer request source.

| Bit 11 RS3 | Bit 10 RS2 | Bit 9 RS1 | Bit 8 RS0 | Description |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | External request, dual address mode (initial value) |
| | | | 1 | Prohibited |
| | | 1 | 0 | External request, single address mode. External address space → external device. |
| | | | 1 | External request, single address mode. External device → external address space. |
| | 1 | 0 | 0 | Auto-request |
| | | | 1 | Prohibited |
| | | 1 | 0 | MTU TGI0A |
| | | | 1 | MTU TGI1A |
| 1 | 0 | 0 | 0 | MTU TGI2A |
| | | | 1 | Prohibited |
| | | 1 | 0 | Prohibited |
| | | | 1 | A/D ADI |
| | 1 | 0 | 0 | SCI0 TXI0 |
| | | | 1 | SCI0 RXI0 |
| | | 1 | 0 | SCI1 TXI1 |
| | | | 1 | SCI1 RXI1 |

**Bit 6—$\overline{\text{DREQ}}$ Select (DS):** Sets the sampling method for the $\overline{\text{DREQ}}$ pin in external request mode to either low-level detection or falling-edge detection. When specifying an on-chip peripheral module or auto-request as the transfer request source, this bit setting is ignored. The sampling method is fixed at falling-edge detection in cases other than auto-request.

| Bit 6 DS | Description | |
|---|---|---|
| 0 | Low-level detection | (initial value) |
| 1 | Falling-edge detection | |

**Bit 5—Transfer Mode (TM):** Specifies the bus mode for data transfer.

| Bit 5 TM | Description | |
|---|---|---|
| 0 | Cycle steal mode | (initial value) |
| 1 | Burst mode | |

**Bits 4 and 3—Transfer Size 1, 0 (TS1, TS0):** Specifies size of data for transfer.

| Bit 4 TS1 | Bit 3 TS0 | Description | |
|---|---|---|---|
| 0 | 0 | Specifies byte size (8 bits) | (initial value) |
| | 1 | Specifies word size (16 bits) | |
| 1 | 0 | Specifies longword size (32 bits) | |
| | 1 | Prohibited | |

**Bit 2—Interrupt Enable (IE):** When this bit is set to 1, interrupt requests are generated after the number of data transfers specified in the DMATCR (when TE = 1).

| Bit 2 IE | Description |
|---|---|
| 0 | Interrupt request not generated after DMATCR-specified transfer count (initial value) |
| 1 | Interrupt request enabled on completion of DMATCR specified number of transfers |

### 9.2.5 DMAC Operation Register (DMAOR)

The DMAOR is a 16-bit read/write register that specifies the transfer mode of the DMAC. Bits 15 to 3 of this register always read as 0. The write value should always be 0.

Register values are initialized to 0 during power-on reset or in software standby mode.

| Bit: | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | — | — | — |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R | R | R | R | R | R | R | R |

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | — | AE | NMIF | DME |
| Initial value: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R | R | R | R | R | R/(W)* | R/(W)* | R |

Note: * 0 write only is valid after 1 is read.

**Bit 2—Address Error Flag (AE):** Indicates that an address error has occurred during DMA transfer. If this bit is set during a data transfer, transfers on all channels are suspended. The CPU cannot write a 1 to the AE bit. Clearing is effected by 0 write after 1 read.

| Bit 2 AE | Description | |
|---|---|---|
| 0 | No address error, DMA transfer enabled | (initial value) |
| | Clearing condition: Write AE = 0 after reading AE = 1 | |
| 1 | Address error, DMA transfer disabled | |
| | Setting condition: Address error due to DMAC | |

**Channel 2**

| Bit 2 TPSC2 | Bit 1 TPSC1 | Bit 0 TPSC0 | Description |
|---|---|---|---|
| 0 | 0 | 0 | Internal clock: count with $\phi$/1 (initial value) |
| | | 1 | Internal clock: count with $\phi$/4 |
| | 1 | 0 | Internal clock: count with $\phi$/16 |
| | | 1 | Internal clock: count with $\phi$/64 |
| 1 | 0 | 0 | External clock: count with the TCLKA pin input |
| | | 1 | External clock: count with the TCLKB pin input |
| | 1 | 0 | External clock: count with the TCLKC pin input |
| | | 1 | Internal clock: count with $\phi$/1024 |

Note: These settings are ineffective when channel 2 is in phase counting mode.

### 10.2.2 Timer Mode Register (TMDR)

The TMDR is an 8-bit read/write register that sets the operating mode for each channel. The MTU has three TMDR registers, one for each channel. TMDR is initialized to H'C0 by a power-on reset or the standby mode.

**Channel 0: TMDR0**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | — | — | BFB | BFA | MD3 | MD2 | MD1 | MD0 |
| Initial value: | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

**Channels 1, 2: TMDR1, TMDR2**

| Bit: | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | — | — | — | — | MD3 | MD2 | MD1 | MD0 |
| Initial value: | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W: | R | R | R | R | R/W | R/W | R/W | R/W |

**Table 10.13 MTU Interrupt Sources**

| Channel | Interrupt Source | Description | DMAC Activation | Priority* |
|---|---|---|---|---|
| 0 | TGI0A | TGR0A input capture/compare-match | Yes | High |
| | TGI0B | TGR0B input capture/compare-match | No | |
| | TGI0C | TGR0C input capture/compare-match | No | |
| | TGI0D | TGR0D input capture/compare-match | No | |
| | TCI0V | TCNT0 overflow | No | |
| 1 | TGI1A | TGR1A input capture/compare-match | Yes | |
| | TGI1B | TGR1B input capture/compare-match | No | |
| | TCI1V | TCNT1 overflow | No | |
| | TCI1U | TCNT1 underflow | No | |
| 2 | TGI2A | TGR2A input capture/compare-match | Yes | |
| | TGI2B | TGR2B input capture/compare-match | No | |
| | TCI2V | TCNT2 overflow | No | |
| | TCI2U | TCNT2 underflow | No | Low |

Note: * Indicates the initial status following reset. The ranking of channels can be altered using the interrupt controller.

### 10.5.2 DMAC Activation

The TGRA register input capture/compare-match interrupt of any channel can be used as a source to activate the on-chip DMAC. For details, refer to section 9, Direct Memory Access Controller (DMAC).

The MTU has three TGRA register input capture/compare-match interrupts, one for any channel, that can be used as DMAC activation sources.

### 10.5.3 A/D Converter Activation

The TGRA register input capture/compare-match of any channel can be used to activate the on-chip A/D converter.

If the TTGE bit of the TIER is already set to 1 when the TGFA flag in the TSR is set to 1 by a TGRA register input capture/compare-match of any of the channels, an A/D conversion start request is sent to the A/D converter. If the MTU conversion start trigger is selected at such a time on the A/D converter side when this happens, the A/D conversion starts.

**Bit 4—Receive Enable (RE):** Enables or disables the SCI serial receiver.

| Bit 4 RE | Description | |
|---|---|---|
| 0 | Receiver disabled*[1] | (initial value) |
| 1 | Receiver enabled*[2] | |

Notes: 1. Clearing RE to 0 does not affect the receive flags (RDRF, FER, PER, ORER). These flags retain their previous values.
2. Serial reception starts when a start bit is detected in the asynchronous mode, or synchronous clock input is detected in the clock synchronous mode. Select the receive format in the SMR before setting RE to 1.

**Bit 3—Multiprocessor Interrupt Enable (MPIE):** Enables or disables multiprocessor interrupts. The MPIE setting is used only in the asynchronous mode, and only if the multiprocessor mode bit (MP) in the serial mode register (SMR) is set to 1 during reception. The MPIE setting is ignored in the clock synchronous mode or when the MP bit is cleared to 0.

| Bit 3 MPIE | Description |
|---|---|
| 0 | Multiprocessor interrupts are disabled (normal receive operation) (initial value)<br>MPIE is cleared when the MPIE bit is cleared to 0, or the multiprocessor bit (MPB) is set to 1 in receive data. |
| 1 | Multiprocessor interrupts are enabled*<br>Receive-data-full interrupt requests (RXI), receive-error interrupt requests (ERI), and setting of the RDRF, FER, and ORER status flags in the serial status register (SSR) are disabled until data with the multiprocessor bit set to 1 is received. |

Note: * The SCI does not transfer receive data from the RSR to the RDR, does not detect receive errors, and does not set the RDRF, FER, and ORER flags in the serial status register (SSR). When it receives data that includes MPB = 1, MPB is set to 1, and the SCI automatically clears MPIE to 0, generates RXI and ERI interrupts (if the TIE and RIE bits in the SCR are set to 1), and allows the FER and ORER bits to be set.

| Bit Rate (Bits/s) | φ (MHz) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 18.432 | | | 19.6608 | | | 20 | | |
| | n | N | Error (%) | n | N | Error (%) | n | N | Error (%) |
| 110 | 3 | 81 | –0.22 | 3 | 86 | 0.31 | 3 | 88 | –0.25 |
| 150 | 2 | 239 | 0.00 | 2 | 255 | 0.00 | 3 | 64 | 0.16 |
| 300 | 2 | 119 | 0.00 | 2 | 127 | 0.00 | 2 | 129 | 0.16 |
| 600 | 1 | 239 | 0.00 | 1 | 255 | 0.00 | 2 | 64 | 0.16 |
| 1200 | 1 | 119 | 0.00 | 1 | 127 | 0.00 | 1 | 129 | 0.16 |
| 2400 | 0 | 239 | 0.00 | 0 | 255 | 0.00 | 1 | 64 | 0.16 |
| 4800 | 0 | 119 | 0.00 | 0 | 127 | 0.00 | 0 | 129 | 0.16 |
| 9600 | 0 | 59 | 0.00 | 0 | 63 | 0.00 | 0 | 64 | 0.16 |
| 14400 | 0 | 39 | 0.00 | 0 | 42 | –0.78 | 0 | 42 | 0.94 |
| 19200 | 0 | 29 | 0.00 | 0 | 31 | 0.00 | 0 | 32 | –1.36 |
| 28800 | 0 | 19 | 0.00 | 0 | 20 | 1.59 | 0 | 21 | –1.36 |
| 31250 | 0 | 17 | 2.40 | 0 | 19 | –1.70 | 0 | 19 | 0.00 |
| 38400 | 0 | 14 | 0.00 | 0 | 15 | 0.00 | 0 | 15 | 1.73 |

| Bit Rate (Bits/s) | φ (MHz) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | 22 | | | 22.1184 | | | 24 | | |
| | n | N | Error (%) | n | N | Error (%) | n | N | Error (%) |
| 110 | 3 | 97 | –0.35 | 3 | 97 | 0.19 | 3 | 106 | –0.44 |
| 150 | 3 | 71 | –0.54 | 3 | 71 | 0.00 | 3 | 77 | 0.16 |
| 300 | 2 | 142 | 0.16 | 2 | 143 | 0.00 | 2 | 155 | 0.16 |
| 600 | 2 | 71 | –0.54 | 2 | 71 | 0.00 | 2 | 77 | 0.16 |
| 1200 | 1 | 142 | 0.16 | 1 | 143 | 0.00 | 1 | 155 | 0.16 |
| 2400 | 1 | 71 | –0.54 | 1 | 71 | 0.00 | 1 | 77 | 0.16 |
| 4800 | 0 | 142 | 0.16 | 0 | 143 | 0.00 | 0 | 155 | 0.16 |
| 9600 | 0 | 71 | –0.54 | 0 | 71 | 0.00 | 0 | 77 | 0.16 |
| 14400 | 0 | 47 | –0.54 | 0 | 47 | 0.00 | 0 | 51 | 0.16 |
| 19200 | 0 | 35 | –0.54 | 0 | 35 | 0.00 | 0 | 38 | 0.16 |
| 28800 | 0 | 23 | –0.54 | 0 | 23 | 0.00 | 0 | 25 | 0.16 |
| 31250 | 0 | 21 | 0.00 | 0 | 21 | 0.54 | 0 | 23 | 0.00 |
| 38400 | 0 | 17 | –0.54 | 0 | 17 | 0.00 | 0 | 19 | –2.34 |

### 12.3.2 Operation in Asynchronous Mode

In the asynchronous mode, each transmitted or received character begins with a start bit and ends with a stop bit. Serial communication is synchronized one character at a time.

The transmitting and receiving sections of the SCI are independent, so full duplex communication is possible. The transmitter and receiver are both double buffered, so data can be written and read while transmitting and receiving are in progress, enabling continuous transmitting and receiving.

Figure 12.2 shows the general format of asynchronous serial communication. In asynchronous serial communication, the communication line is normally held in the marking (high) state. The SCI monitors the line and starts serial communication when the line goes to the space (low) state, indicating a start bit. One serial character consists of a start bit (low), data (LSB first), parity bit (high or low), and stop bit (high), in that order.

When receiving in the asynchronous mode, the SCI synchronizes on the falling edge of the start bit. The SCI samples each data bit on the eighth pulse of a clock with a frequency 16 times the bit rate. Receive data is latched at the center of each bit.

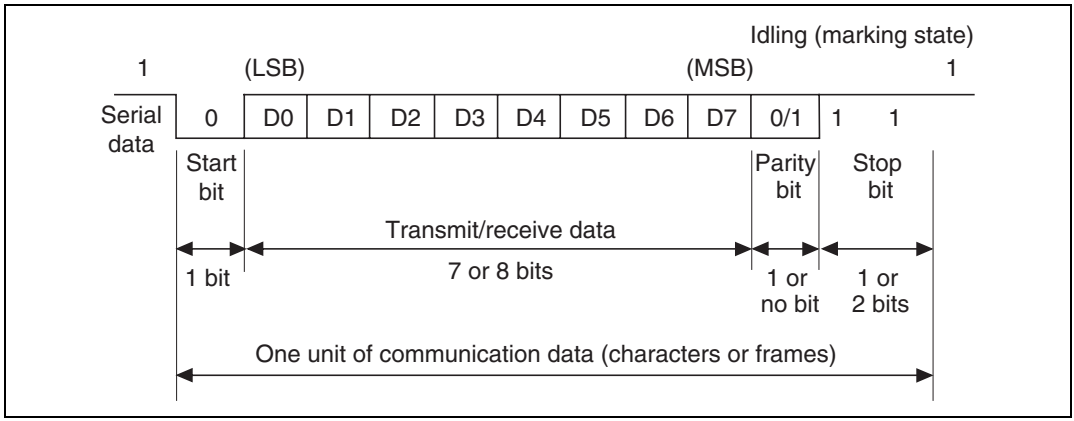



**Figure 12.2 Data Format in Asynchronous Communication (Example: 8-bit Data with Parity and Two Stop Bits)**

**Transmit/Receive Operations**

**SCI Initialization (Clock Synchronous Mode):** Before transmitting or receiving, software must clear the TE and RE bits to 0 in the serial control register (SCR), then initialize the SCI as follows.

When changing the mode or communication format, always clear the TE and RE bits to 0 before following the procedure given below. Clearing TE to 0 sets TDRE to 1 and initializes the transmit shift register (TSR). Clearing RE to 0, however, does not initialize the RDRF, PER, FER, and ORER flags and receive data register (RDR), which retain their previous contents.

Figure 12.15 is a sample flowchart for initializing the SCI.

1. Select the clock source in the serial control register (SCR). Leave RIE, TIE, TEIE, MPIE, TE, and RE cleared to 0.
2. Select the communication format in the serial mode register (SMR).
3. Write the value corresponding to the bit rate in the bit rate register (BRR) unless an external clock is used.
4. Wait for at least the interval required to transmit or receive one bit, then set TE or RE in the serial control register (SCR) to 1. Also set RIE, TIE, TEIE, and MPIE. The TxD, RxD pins becomes usable in response to the PFC corresponding bits and the TE, RE bit settings.

### 13.4.7 Conversion Start Modes

The conversion start mode of the high speed A/D converter is set by the PWR bit of the ADCSR. When the PWR bit is cleared to 0, low-power conversion mode is set and the internal analog circuit becomes inactive. High-speed start mode is set by setting the PWR bit to 1, and the analog circuit becomes active.

In the low-power conversion mode, power is applied to the analog circuitry simultaneous to the conversion start (ADST set). When 200 cycles of the reference clock have elapsed, conversion becomes possible for the analog circuit and the first A/D conversion begins. When performing consecutive conversions, the second and later conversions are executed in 20 cycles. Select the basic clock with the CKS bit of the ADCSR. When the A/D conversion ends, ADST is cleared to 0 and the analog circuit power supply is automatically cut off. Because the analog circuit is only active during the A/D conversion operation period in this mode, current consumption can be reduced.

In high-speed start mode, ADST is cleared to 0 when A/D conversion ends. Power continues to be supplied to the analog circuitry, and conversion-ready status is maintained. Conversion is restarted immediately by resetting ADST to 1. However, the first conversion after power-on begins 200 cycles after setting ADST. Clear the PWR bit to 0 to switch off the analog power supply. When performing consecutive conversions, the second and later conversions are executed in 20 cycles. Because the analog circuit is always active in this mode, A/D conversion can be executed at high speed.

When A/D conversion is forcibly halted by clearing the ADST bit to 0 during conversion in high-speed start mode (when ADST = 1), the first conversion following a restart may not be performed normally. The second and subsequent conversions are performed normally.

Figures 13.9 and 13.10 show the timing of the conversion start operation.

## 13.6 Usage Notes

Note the following points concerning the high speed A/D converter.

### 13.6.1 Analog Input Voltage Range

During A/D conversions, see that the voltage applied to the analog input pins AN0 to AN7 is within the range of $AV_{SS} \leq$ AN0 to AN7 $\leq AV_{CC}$.

### 13.6.2 $AV_{CC}$, $AV_{SS}$ Input Voltages

The $AV_{CC}$, $AV_{SS}$ input voltages should be $AV_{CC} = V_{CC} \pm 10\%$, and $AV_{SS} = V_{SS}$. When not using the high speed A/D converter, make $AV_{CC} = V_{CC}$ and $AV_{SS} = V_{SS}$. When in standby mode, make $V_{RAM} \leq AV_{CC} \leq 5.5$ V, and $AV_{SS} = V_{SS}$. $V_{RAM}$ is the RAM standby voltage.

### 13.6.3 Input Ports

Make the time constant of circuitry connected to an input port shorter than the high speed A/D converter sampling time. If the time constant of the circuit is longer, there will be occasions where the input voltage is not adequately sampled.

### 13.6.4 Conversion Start Modes

Current consumption will be different for the A/D conversion operation in high speed start mode and low-power conversion mode according to the PWR bit setting.

### 13.6.5 A/D Conversion Termination (HD6417014R only)

If conversion is terminated while in progress (when ADST = 1) in high-speed start mode (PWR = 1) by clearing the ADST bit, there may be a large degree of error in the first conversion following the restart (on channel 1 in normal mode, or channel 2 in simultaneous sampling mode). Subsequent conversions will be performed normally

If A/D conversion is terminated while in progress, use one of the following methods to solve this problem:

(a) Ignore the first data following a restart after termination.
(b) If the first data after a restart is used, perform a single dummy conversion in single mode after the termination, terminate A/D conversion, then restart.
(c) After termination, write 0 to the PWR bit before restarting. (In this case, the first conversion after the restart will begin after the elapse of 200 A/D reference clock cycles.)

### 14.2.2 A/D Control/Status Register (ADCSR)

| Bit : | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | ADF | ADIE | ADST | SCAN | CKS | CH2 | CH1 | CH0 |
| Initial value : | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| R/W : | R/(W)* | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Note: * Only 0 can be written to clear the flag.

The A/D control/status register (ADCSR) is register that can read/write in 8 bits and control mid-speed A/D converter operations such as mode selection.

The ADCSR is initialized to H'00 during power-on reset.

**Bit 7—A/D End Flag (ADF):** Status flag that indicates end of A/D conversion.

| Bit 7 ADF | Description | |
|---|---|---|
| 0 | [Clear conditions] | (Initial value) |
| | 1. Writing 0 to ADF after reading ADF with ADF = 1 | |
| | 2. When registers of the mid-speed converter are accessed after the DMAC is activated by ADI interrupt. | |
| 1 | [Set conditions] | |
| | 1. Single mode: When A/D conversion is complete | |
| | 2. Scan mode: When A/D conversion of all designated channels are complete | |

**Bit 6—A/D Interrupt Enable (ADIE):** Enables or disables interrupt request (ADI) due to completion of A/D conversion.

| Bit 6 ADIE | Description | |
|---|---|---|
| 0 | Disables interrupt request (ADI) due to completion of A/D conversion | (Initial value) |
| 1 | Enables interrupt request (ADI) due to completion of A/D conversion | |

## 15.5 Usage Notes

Take care that the contentions described in sections 15.5.1 to 15.5.3 do not arise during CMT operation.

### 15.5.1 Contention between CMCNT Write and Compare Match

If a compare match signal is generated during the $T_2$ state of the CMCNT counter write cycle, the CMCNT counter clear has priority, so the write to the CMCNT counter is not performed. Figure 15.6 shows the timing.

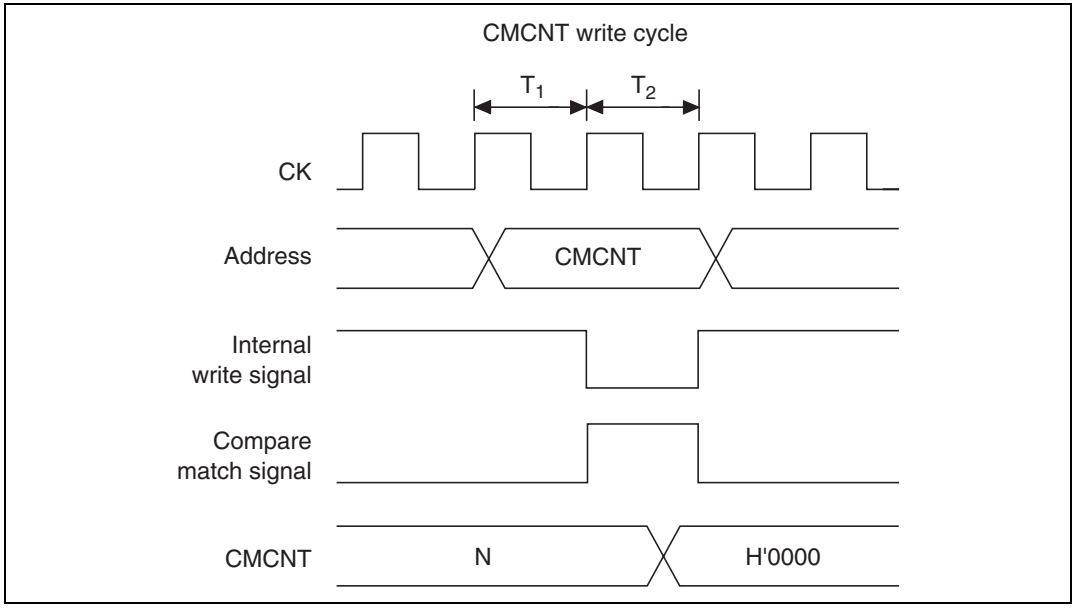



**Figure 15.6 CMCNT Write and Compare Match Contention**

### 18.7.2 Program-Verify Mode

In program-verify mode, the data written in program mode is read to check whether it has been correctly written in the flash memory.

After the elapse of a given programming time, the programming mode is exited (the P bit in FLMCR1 is cleared, then the PSUn bit is cleared at least 10 μs later). The watchdog timer is cleared after the elapse of 10 μs or more, and the operating mode is switched to program-verify mode by setting the PV bit in FLMCR1. Before reading in program-verify mode, a dummy write of H'FF data should be made to the addresses to be read. The dummy write should be executed after the elapse of 4 μs or more. When the flash memory is read in this state (verify data is read in 32-bit units), the data at the latched address is read. Wait at least 2 μs after the dummy write before performing this read operation. Next, the written data is compared with the verify data, and reprogram data is computed (see figure 18.13) and transferred to the reprogram data area. After 32 bytes of data have been verified, exit program-verify mode, wait for at least 4 μs, then clear the SWE bit in FLMCR1. If reprogramming is necessary, set program mode again, and repeat the program/program-verify sequence as before. However, ensure that the program/program-verify sequence is not repeated more than 1000 times on the same bits.

| Item | Pin | Symbol | Min | Typ | Max | Unit | Measurement Conditions |
|---|---|---|---|---|---|---|---|
| Output high-level voltage | All output pins | $V_{OH}$ | $V_{CC}$ –0.5 | — | — | V | $I_{OH}$ = –200 µA |
| | | | 3.5 | — | — | V | $I_{OH}$ = –1 mA |
| Output low-level voltage | All output pins | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 1.6 mA |
| Input capacitance | $\overline{RES}$ | Cin | — | — | 80 | pF | Vin = 0 V, f = 1 MHz, Ta = 25°C |
| | NMI | | — | — | 50 | pF | |
| | All other input pins | | — | — | 20 | pF | |
| Current consumption (SH7014) | Ordinary operation | $I_{CC}$ | — | 130 | 180 | mA | f = 28 MHz |
| | Sleep | | — | 100 | 150 | mA | f = 28 MHz |
| | Standby | | — | 0.01 | 5 | µA | Ta ≤ 50°C |
| | | | — | — | 20 | µA | Ta > 50°C |
| Current consumption (SH7016, SH7017) | Ordinary operation | $I_{CC}$ | — | 140 | 180 | mA | f = 28 MHz |
| | Sleep | | — | 110 | 150 | mA | f = 28 MHz |
| | Standby | | — | 0.01 | 5 | µA | Ta ≤ 50°C |
| | | | — | — | 20 | µA | Ta > 50°C |
| Analog supply current (SH7014) | | $AI_{CC}$ | — | 13 | 22 | mA | |
| Analog supply current (SH7016, SH7017) | | $AI_{CC}$ | — | 5 | 10 | mA | |
| RAM standby voltage | | $V_{RAM}$ | 2.0 | — | — | V | |

Notes: 1. When the A/D converter is not used (including during standby), do not release the $AV_{CC}$ and $AV_{SS}$ pins. Connect the $AV_{CC}$ pin to $V_{CC}$ and the $AV_{SS}$ pin to $V_{SS}$.

2. The current consumption is measured when $V_{IH}$min = $V_{CC}$ –0.5 V, $V_{IL}$ max = 0.5 V, with all output pins unloaded.

3. The F-ZTAT and mask versions have the same functions, and the electrical characteristics of both are within specification, but characteristic-related performance values, operating margins, noise margins, noise emission, etc., are different. Caution is therefore required in carrying out system design, and when switching between F-ZTAT and mask versions.

BSC

| Wait Control Register 2 (WCR2) | H'FFFF8626 | 8/16/32 |
|---|---|---|

| Item | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Bit name | — | — | — | — | — | — | — | — |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R |
| Item | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Bit name | — | — | DDW1 | DDW0 | DSW3 | DSW2 | DSW1 | DSW0 |
| Initial value | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| R/W | R | R | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Name | Value | | | | Description |
|---|---|---|---|---|---|---|
| 5, 4 | DRAM Space DMA Single Address Mode Access Wait Specification (DDW1, DDW0) | 0 | | 0 | | 2-cycle (no wait) external wait disabled (initial value) |
| | | 0 | | 1 | | 3-cycle (1 wait) external wait disabled |
| | | 1 | | 0 | | 4-cycle (2 wait) external wait enabled |
| | | 1 | | 1 | | 5-cycle (3 wait) external wait enabled |
| 3 to 0 | CS Space DMA Single Address Mode Access Wait Specification (DSW3 to DSW0) | 0 | 0 | 0 | 0 | No wait (external wait input disabled) |
| | | 0 | 0 | 0 | 1 | 1 wait (external wait input enabled) |
| | | … | | | | |
| | | 1 | 1 | 1 | 1 | 15 wait (external wait input enabled) (initial value) |

| DRAM Area Control Register (DCR) | H'FFFF862A | 8/16/32 |
|---|---|---|

| Item | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Bit name | TPC | RCD | TRAS1 | TRAS0 | DWW1 | DWW0 | DWR1 | DWR0 |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Item | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Bit name | DIW | — | BE | RASD | — | SZ0 | AMX1 | AMX0 |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R | R/W | R/W | R | R/W | R/W | R/W |

BSC

| Refresh Timer Control/Status Register (RTCSR) | H'FFFF862C | 8/16/32 |
|---|---|---|

| Item | Bit | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Bit name | — | — | — | — | — | — | — | — |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R | R | R | R | R | R | R |
| Item | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Bit name | — | CMF | CMIE | CKS2 | CKS1 | CKS0 | RFSH | RMD |
| Initial value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

| Bit | Name | Value | | | Description |
|---|---|---|---|---|---|
| 6 | Compare Match Flag (CMF) | 0 | | | Clear condition: After RTCSR is read when CMF is 1, 0 is written in CMF (initial value) |
| | | 1 | | | Set condition: RTCNT = RTCOR<br>Note: When both RTCNT and RTCOR are in an initialized state (when values have not been rewritten since initialization, and RTCNT has not had its value changed due to a countup), RTCNT and RTCOR match, as both are H'0000, but in this case CMF is not set. |
| 5 | Compare Match Interrupt Enable (CMIE) | 0 | | | Disables an interrupt request caused by CMF (initial value) |
| | | 1 | | | Enables an interrupt request caused by CMF |
| 4 to 2 | Clock Select (CKS2 to CKS0) | 0 | 0 | 0 | Stops count-up (initial value) |
| | | | | 1 | φ/2 |
| | | | 1 | 0 | φ/8 |
| | | | | 1 | φ/32 |
| | | 1 | 0 | 0 | φ/128 |
| | | | | 1 | φ/512 |
| | | | 1 | 0 | φ/2048 |
| | | | | 1 | φ/4096 |
| 1 | Refresh Control (RFSH) | 0 | | | Do not refresh DRAM (initial value) |
| | | 1 | | | Refresh DRAM |
| 0 | Refresh Mode (RMD) | 0 | | | CAS-before-RAS refresh (initial value) |
| | | 1 | | | Self-refresh |