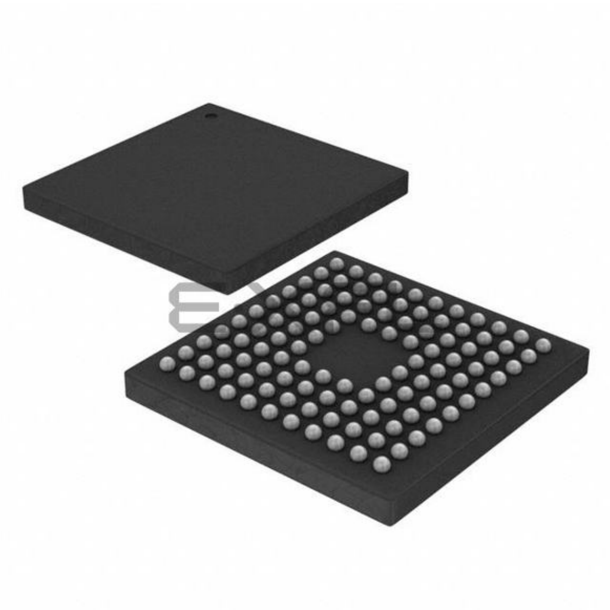

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	28
Program Memory Size	256KB (128K x 8 x 2)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	2.9V ~ 3.6V
Data Converters	A/D 22x14b; D/A 8x12b
Oscillator Type	Internal
Operating Temperature	-10°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-TFBGA, CSPBGA
Supplier Device Package	112-CSPBGA (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/aducm310bbcz-rl

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- ADuCM310 Evaluation Board

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Application Notes

- AN-1160: Cortex-M3 Based ADuCxxx Serial Download Protocol
- AN-1322: ADuCM320 Code Execution Speed

Data Sheet

- ADuCM310: Precision Analog Microcontroller, Tunable Optical Control Microcontroller Data Sheet

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- UG-549: How to Set Up and Use the ADuCM310
- UG-829: ADuCM310 Development Systems Getting Started Tutorial

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GENERAL DESCRIPTION

The ADuCM310 is a multidie stack, on-chip system designed for diagnostic control of tunable laser optical module applications. The ADuCM310 features a 16-bit (14-bit accurate) multichannel successive approximation register (SAR) ADC, an ARM Cortex™-M3 processor, eight voltage DACs (VDACs), six current output DACs, and Flash/EE memory packaged in a 6 mm × 6 mm, 112-ball CSP_BGA package.

The bottom die in the stack supports the bulk of the low voltage analog circuitry and is the largest of the three die. It contains the ADC, VDACs, main IDAC circuits, as well as other analog support circuits, such as the low drift precision 2.5 V voltage reference source.

The middle die in the stack supports the bulk of the digital circuitry, including the ARM Cortex-M3 processor, the flash and SRAM blocks, and all of the digital communication peripherals. In addition, this die provides the clock sources for the whole chip. A 16 MHz internal oscillator is the source of the internal PLL that outputs an 80 MHz system clock.

The top die, which is the smallest die, was developed on a high voltage process, and this die supports the −5 V and +5 V VDAC outputs. It also implements the SOA IDAC current sink circuit that allows the external SOA diode to pull to a −3.0 V level to implement the fast shutdown of the laser output.

Regarding the individual blocks, the ADC is capable of operating at conversion rates up to 800 kSPS. There are 10 external inputs to the ADC, which can be single ended or differential. Several internal channels are included, such as the supply monitor channels, an on-chip temperature sensor, and internal voltage reference monitors.

The VDACs are 12-bit string DACs with output buffers capable of sourcing between 10 mA and 50 mA, and these DACs are all capable of driving 10 nF capacitive loads.

The low drift current DACs have 14-bit resolution and varied full-scale output ranges from 0 mA to 20 mA to 0 mA to 250 mA on the SOA IDAC (IDAC3). The SOA IDAC also comes with a 0 mA to −80 mA current sink capability.

A precision 2.5 V on-chip reference source is available. The internal ADC, IDACs, and VDAC circuits use this on-chip reference source to ensure low drift performance for all of these peripherals

The ADuCM310 also provides 2× buffered reference outputs capable of sourcing up to 1.2 mA. These outputs can be used externally to the chip.

The ADuCM310 integrates an 80 MHz ARM Cortex-M3 processor. It is a 32-bit reduced instruction set computer (RISC) machine, offering up to 100 DMIPS peak performance. The ARM Cortex-M3 processor also has a flexible 14-channel direct memory access (DMA) controller supporting serial peripheral interface (SPI), UART, and I^{2}C communication peripherals. The ADuCM310 has 256 kB of nonvolatile Flash/EE memory and 32 kB of SRAM integrated on-chip.

A 16 MHz on-chip oscillator generates the 80 MHz system clock. This clock internally divides to allow the processor to operate at lower frequency, thus saving power. A low power internal 32 kHz oscillator is available and can clock the timers. The ADuCM310 includes three general-purpose timers, a wake-up timer (which can be used as a general-purpose timer), and a system watchdog timer.

A range of communication peripherals can be configured as required in a specific application. These peripherals include UART, 2 × I^{2}C, 2 × SPI, GPIO ports, and pulse-width modulation (PWM).

On-chip factory firmware supports in-circuit serial download via the UART, while nonintrusive emulation and program download are supported via the serial wire debug port (SW-DP) interface. These features are supported on the EVAL-ADuCM310QSPZ development system.

The ADuCM310 operates from 2.9 V to 3.6 V and is specified over a temperature range of −10°C to +85°C.

Note that, throughout this data sheet, multifunction pins, such as P1.0/SIN/ECLKIN/PLAI[4], are referred to either by the entire pin name or by a single function of the pin, for example, P1.0, when only that function is relevant.

For additional information on the ADuCM310, see the ADuCM310 reference manual, *How to Set Up and Use the ADuCM310*.

SPECIFICATIONS

$AV_{DD} = IOV_{DD} = DV_{DD}$ = 2.9 V to 3.6 V (the input supply voltages). The difference between AV_{DD}, IOV_{DD}, and DV_{DD} must be ≤0.3 V. AV_{NEG} (the supply voltage) = −5.5 V to −4.65 V. $VDACV_{DD}$ (the VDAC supply voltage) = 3.07 V to 5.35 V (for VDAC6 and VDAC7), and $VDACV_{DD}$ must be ≥ AV_{DD}. PV_{DD} (the IDAC supply voltage) for the IDACs = 1.8 V to 2.7 V. $AV_{DD} \geq PV_{DD}$ + 0.4V. V_{REF} = 2.5 V internal reference, f_{CORE} = 80 MHz, T_A = −10°C to +85°C, unless otherwise noted.

For power sequencing, apply power to the AV_{NEG} or $VDACV_{DD}$ pin before connecting the ground pins.

For register and bit information, see the ADuCM310 reference manual, *How to Set Up and Use the ADuCM310*.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC CHANNEL SPECIFICATIONS					All measurements in single-ended mode, unless otherwise stated
ADC Power-Up Time		5		µs	f_{SAMPLE} ≥500 kSPS
DC Accuracy					
Resolution	14			Bits	
Integral Nonlinearity					
Input Buffer					
Disabled		±1.5		LSB	2.5 V internal reference
Enabled		±2.5		LSB	
Disabled		±1.5		LSB	External reference
Differential Nonlinearity	−0.99	±0.7	+1.5	LSB	2.5 V internal reference; no missing codes
	−0.99	±0.7	+1.5[1]	LSB	2.5 V external reference; no missing codes
DC Code Distribution		±3		LSB	ADC input voltage = 1.25 V dc
ENDPOINT ERRORS					
Offset Error (All Channels Except the Internal Channels)					ADC update rate up to 800 kSPS
Buffer On or Buffer Off	−0.6	±0.2	+0.6	mV	Buffer on, chop mode on and automatic zero or buffer off
Offset Error Drift[1]					
Buffer On or Buffer Off		±2.5		µV/°C	Buffer on, chop mode on and automatic zero or buffer off
Full-Scale Error					ADC update rate up to 800 kSPS
Buffer On or Buffer Off	−0.7	±0.2	+0.6	mV	Excluding internal channels
Internal Channels		±0.2	+0.6	% of full scale	Input buffer on; AV_{DD}/2, IOV_{DD}/2, PV_{DD} voltage on PVDD_IDAC2 pin
		0.75	1.5	% of full scale	Input buffer on; IDAC0 to IDAC5; measured with 1.5 V on the IDAC0 to IDAC5 pins
Gain Error Drift[1]		2		µV/°C	Full-scale error drift minus offset error drift; all modes; internal reference
DYNAMIC PERFORMANCE[1]					f_{IN} = 665.283 Hz sine wave; f_{SAMPLE} = 100 kSPS; internally unbuffered channels; the filter on the analog inputs is a 15 Ω resistor and a 2 nF capacitor
Signal-to-Noise Ratio (SNR)					
Input Buffer					
Disabled		80		dB	Includes distortion and noise components
Enabled		78		dB	Chop mode on
		74		dB	Automatic zero

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Total Harmonic Distortion (THD)					
Input Buffer					
Disabled		−86		dB	
Enabled		−86		dB	Chop mode on and automatic zero
Peak Harmonic or Spurious Noise		−88		dB	Buffer on and off
Channel-to-Channel Crosstalk		−95		dB	Measured on adjacent channels; f_{IN} = 25 kHz sine wave; buffer on and off
ANALOG INPUT					
Absolute Input Voltage Range					
Unbuffered Mode	AGND		AV_{DD}	V	Voltage level on AINx pin
Buffered Mode	AGND + 0.15		2.5	V	Voltage level on AINx pin
Input Voltage Ranges					
Differential Mode	$-V_{REF}$		$+V_{REF}$	V	Voltage difference between AIN+ (positive input) and AIN− (negative input)
Common-Mode Voltage Range	0.9		1.6	V	
Single-Ended Mode	AGND		V_{REF}	V	Voltage difference between AIN+ and AIN−
Input Current[2]					
Buffered Mode					V_{IN} = 0.15 V to 2.5 V
AIN0, AIN1, AIN2, and AIN3	−10[1]	±5	+12.5[1]	nA	ADC sampling rate ≤ 100 kSPS
	−40	±15	+60	nA	ADC sampling rate ≤ 500 kSPS
	−60[1]	±25	+90[1]	nA	ADC sampling rate ≤ 800 kSPS
Input Current Drift		±10		pA/°C	Input buffer on, ADC sampling rate ≤ 500 kSPS
		±20		pA/°C	Input buffer on, ADC sampling rate ≤ 800 kSPS
AIN4 to AIN9	−50[1]	±20	+50[1]	nA	AIN4 to AIN9 ≤ 100 kSPS
	−210[1]	±50	+110[1]	nA	ADC sampling rate ≤ 500 kSPS
	−350[1]	−90	+90[1]	nA	ADC sampling rate ≤ 800 kSPS
Unbuffered Mode	−1100[1]	+750	+1700[1]	nA	V_{IN} = 0 V to 2.5 V, all channels, all sampling rates
Input Current Drift		±140		pA/°C	V_{IN} = 1 V
Input Capacitance		20		pF	During ADC acquisition, buffer on
Input Leakage Current	−1.6[1]	+1	+3.5[1]	nA	ADC off, buffer off or buffer on, AINx connected 2.5 V
ON-CHIP VOLTAGE REFERENCE					0.47 µF from VREF_1.2 to AGND
Output Voltage		2.505		V	
Accuracy[3]			±5	mV	T_A = 25°C
Reference Temperature Coefficient[1, 4]		15	30	ppm/°C	
Power Supply Rejection Ratio		70		dB	
Output Impedance		3		Ω	For ADC_CAPP, T_A = 25°C
Internal V_{REF} Power-On Time[1]		38	50	ms	Turned on by default
EXTERNAL REFERENCE INPUT[1]					
Input Voltage Range[1]	1.8		2.5	V	ADC maximum reference voltage = 2.5 V
Switching Time					
External to Internal Reference		2.5		ms	
Internal to External Reference		1		ms	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
BUFFERED VREF OUTPUTS (BUF_VREF2.5x PINS)					
Output Voltage		2.5		V	
Accuracy			±5	mV	T_A = 25°C, load = 0.4 mA
Reference Temperature Coefficient[1]		15	30	ppm/°C	100 nF capacitor required on both outputs
Load Regulation		2.5		mV/mA	
Output Impedance		3		Ω	T_A = 25°C
Load Current			1.2	mA	
Power Supply Rejection Ratio		70		dB	
IDAC CHANNEL SPECIFICATIONS[5, 6]					
Voltage Compliance Range[1]					Output voltage compliance; minimum compliance if IDACx set to full scale, see Figure 15 to Figure 20
IDAC0, IDAC1, and IDAC2	0.4	PV_{DD} − 200 mV	PV_{DD} − 275 mV	V	
IDAC4 and IDAC5	0.4		PV_{DD} − 200 mV	V	
IDAC3	0.5		PV_{DD} − 450 mV	V	
	−3.7	−3.0		V	At −3.5 V, maximum sink current is 80 mA; pin voltage clamped to −3.5 V, tolerance of clamping voltage is ±200 mV
Reference Current Generator					
Reference Current		0.38		mA	Using internal reference, 0.1%, ≤5 ppm, 3.16 kΩ external resistor
IDAC Reference Current Shutdown Threshold		0.76		mA	If the external resistor (R_{EXT}) value drops below 1.580 kΩ, IDAC output currents disable
Temperature Coefficient[1, 4]		7	25	ppm/°C	Using internal reference;
Over Heat Shutdown		135		°C	Junction temperature
Resolution					
IDAC0, IDAC1, IDAC4,and IDAC5		14		Bits	11-bit MSBs and 5-bit LSBs are guaranteed monotonic
IDAC2		14		Bits	11-bit MSBs and 5-bit LSBs are guaranteed monotonic
IDAC3		14		Bits	0 V to 2 V compliant range, 11-bit MSBs and 5-bit LSBs are guaranteed monotonic
IDAC3	8			Bits	−4.5 V to 0 V compliant range
Full-Scale Output					
IDAC0 and IDAC1		100		mA	
IDAC4 and IDAC5		20		mA	
IDAC2		200		mA	
IDAC3		250		mA	Current source
	−80				Current sink
Integral Nonlinearity	−2.5	±1.5	+4	LSB	11-bit
Noise Current					RMS noise; maximum bandwidth setting, IDACxCON[5:2] = 0000b
IDAC0 and IDAC1		1.5		µA	Measured driving 10 Ω
IDAC4 and IDAC5		0.3		µA	Measured driving 100 Ω
IDAC2		4		µA	Measured driving 5 Ω
IDAC3		5		µA	Measured driving 5 Ω

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Full-Scale Error					
IDAC0 and IDAC1	−2.3	±0.25	1	%	
IDAC4 and IDAC 5	−0.7	±0.25	±0.7	%	
IDAC2	−1.75	±0.25	±0.65	%	
IDAC3	−2	±0.25	±1.4	%	
Full-Scale Error Drift vs. Temperature					Including internal reference drift and 5 ppm external resistor
IDAC4 and IDAC5	−40	−12	+30	ppm/°C	
IDAC2 and IDAC3		+55		ppm/°C	Full temperature range
IDAC2 and IDAC3		+40		ppm/°C	Reduced 25°C to 85°C range
IDAC0 and IDAC1	−145	+55	+145	ppm/°C	Full temperature range
IDAC0 and IDAC1	−100	+40	+100	ppm/°C	Reduced 25°C to 85°C range
Full-Scale Error Drift vs. Time[7]					Long-term stability
IDAC0		200		μA/ 1000 hours	
IDAC1		450		μA/ 1000 hours	
IDAC2		500		μA/ 1000 hours	
IDAC3		2250		μA/ 1000 hours	
IDAC4 and IDAC5		40		μA/ 1000 hours	
Zero-Scale Error					Pull-down current off
IDAC0 and IDAC1	−120		+75	μA	
Pull-Down Current	−135		−100	μA	
IDAC4 and IDAC5	−25		+15	μA	
Pull-Down Current	−30		−22	μA	
IDAC2 and IDAC3	−350		+280	μA	
Pull-Down Current for IDAC2	−300		−160	μA	
Zero-Scale Error Drift[1]					
IDAC0 and IDAC1	−850	±300	+1200	nA/°C	
IDAC4 and IDAC5	−120	±50	+205	nA/°C	
IDAC2 and IDAC3		±1		μA/°C	
Settling Time					
IDAC0, IDAC1, IDAC2, and IDAC3		1		ms	To 0.1%, IDACxCON[5:2] = 0101b, ±1 mA change in output current
IDAC4 and IDAC5		2		ms	
IDAC0, IDAC1, IDAC2, and IDAC3		250		μs	To 1%, IDACxCON[5:2] = 0101b, ±1 mA change in output current
IDAC4 and IDAC5		1.2		ms	
IDAC0, IDAC1, IDAC2, and IDAC3		50		μs	To 1%, IDACxCON[5:2] = 0000b, ±1 mA change in output current
IDAC4 and IDAC5		1.1		ms	
IDAC3 Switching Time[1]			1	μs	Time to switch from current source to current sink

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Transconductance					Analog input signal coupled on to CDAMP_IDACx pin via 1 nF capacitor; frequency range = 100 kHz to 1000 kHz; voltage is the peak to peak voltage on the CDAMP_IDACx pin of the associated IDAC; current is peak-to-peak current change
IDAC0 and IDAC1		7.99/100		mA/mV	
IDAC2		12.6/100		mA/mV	
IDAC3		18.6/100		mA/mV	
IDAC4 and IDAC5		1.16/100		mA/mV	
IDAC Shutdown Temperature		125		°C	Die temperature; enabled via IDACxCON[6]
VDAC CHANNEL SPECIFICATIONS[5, 8, 9]					
DC Accuracy					
Resolution	12			Bits	
Relative Accuracy					
VDAC0, VDAC1, and VDAC2	−6	±1	+10	LSB	
VDAC4 and VDAC5	−7	±2	+11	LSB	
VDAC3, VDAC6, and VDAC7	−7	±2	+8	LSB	
Differential Nonlinearity	−0.99	±0.6	+1	LSB	Guaranteed monotonic
Offset Error					
Calculated		±5		mV	2.5 V internal reference
Actual					Measured at Code 0
VDAC0, VDAC1, VDAC4, and VDAC5		4	7	mV	
VDAC6 and VDAC7		15	22	mV	
VDAC2 and VDAC3	−30	−20		mV	
Full-Scale Error			±0.7	% of full scale	For VDAC2, VDAC3, VDAC4, VDAC5, and VDAC6
VDAC0, VDAC1, and VDAC7[1]			±0.7	%	With 500 Ω load
VDAC0 and VDAC1		±0.5		%	With 75 Ω load, over full temperature range
VDAC7		±0.5		%	With 100 Ω load, over full temperature range
Gain Mismatch Error		0.1		%	VDAC0 relative to VDAC1
		0.2		%	VDAC2 relative to VDAC3
		0.1		%	VDAC4 relative to VDAC5
		0.35		%	VDAC6 relative to VDAC7; both driving a 500 Ω load
Offset Error Drift					
Calculated					
VDAC0, VDAC1, VDAC4, and VDAC5		±5		µV/°C	
VDAC2, VDAC3, VDAC6, and VDAC7		±25		µV/°C	
Actual					Measured at Code 0
VDAC0, VDAC1, VDAC4, and VDAC5		±13		µV/°C	
VDAC2, VDAC3, VDAC6, and VDAC7		±75		µV/°C	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
EXTERNAL RESET					
External Reset Minimum Pulse Width[1]	1.5			µs	Minimum pulse width required on external $\overline{RESET}$ pin to trigger a reset sequence
Reset Pin Glitch Immunity[1]			50	ns	Maximum low pulse width on $\overline{RESET}$ pin that does not generate a reset
TEMPERATURE SENSOR					
Accuracy[1]	1.25	1.37	1.494	V	Indicates die temperature; ADC measured voltage for temperature sensor channel without calibration, T_A = 25°C
FLASH/EE MEMORY					
Endurance	10,000			Cycles	
Data Retention	20			Years	T_J = 85°C
INTERNAL HIGH POWER OSCILLATOR		16		MHz	Used as input to PLL to generate 80 MHz clock
Accuracy	−2.25		+2.25	%	
INTERNAL LOW POWER OSCILLATOR		32.768		kHz	
Accuracy	−12	±8	+12	%	
LOGIC INPUTS					
Input Low Voltage (V_{INL})			0.2 × IOV_{DD}	V	
Input High Voltage (V_{INH})	0.7 × IOV_{DD}			V	
Short-Circuit Current[1]			12	mA	
LOGIC OUTPUTS					
Output High Voltage (V_{OH})[10]	IOV_{DD} − 0.4			V	I_{SOURCE} = 2 mA
Output Low Voltage (V_{OL})[10]			0.4	V	I_{SINK} = 2 mA
Short-Circuit Current[1]			12	mA	
INPUT LEAKAGE CURRENT					
Logic 1		80		µA	V_{INH} = 3.6 V
Internal Pull-Up Disabled	−20	+6	+20	nA	
Logic 0		80		µA	V_{INH} = 0 V
Internal Pull-Up Disabled	−20	+6	+20	nA	
Pull-Up	30	40	65	kΩ	If not disabled, disabled at reset; pull-up can be described as an 80 µA (typical) current source
CRYSTAL INPUTS XCLKI AND XCLKO (16 MHz)					
Logic Inputs, XCLKI Only					
Input Low Voltage (V_{INL})		1.1		V	
Input High Voltage (V_{INH})		1.7		V	
XCLKI Input Capacitance		8		pF	
XCLKO Output Capacitance		8		pF	
MICROCONTROLLER UNIT CLOCK RATE					
Using PLL Output[1]	0.05		80	MHz	
PROCESSOR START-UP TIME					
At Power-On[1]		38	50	ms	Includes kernel power-on execution time
After Reset Event		1.44		ms	Includes kernel power-on execution time
After Processor Power Down					
Mode 1, Mode 2, or Mode 3		3 to 5		f_{CLK}	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
Power Supply Voltage Range					
AV_{DD}	2.9	3.3	3.6	V	Measured between AVDDx and AGND
IOV_{DD}	2.9	3.3	3.6	V	Measured between IOVDDx and AGND
Analog Power Supply Currents					
AV_{DD} Current		6.5	7.2	mA	ADC, VDACs, IDACs off
Digital Power Supply Current					
Current in Normal Mode					
DV_{DD}		29	32	mA	CLKCON1[2:0] = [000b]
IOV_{DD}		2.7	3.1	mA	All GPIO pull-ups enabled
Additional Power Supply Currents					
ADC[1]		3.1	3.6	mA	ADC continuously converting at 100 kSPS
ADC Input Buffer[1]		4.1	4.8	mA	Both buffers enabled
IDAC[1]		26.5	30	mA	
DAC[1]		2.7	3.1	mA	Total for all VDACs driving maximum allowed load with DACxDAT = 0
VDAC2 and VDAC3[1]		−1.7		mA	I_{DD} when VDAC2 and VDAC3 are driving maximum allowed load with DACxDAT set to 0
VDAC6 and VDAC7[1]		1		mA	I_{DD} sourced from the $VDACV_{DD}$ supply when VDAC6 and VDAC7 are driving the maximum allowed load with DACxDAT set to 0

[1] These numbers are not production tested but are guaranteed by design and/or characterization data at production release.
[2] The input current is the total input current including the input pad and mux leakage plus the charge current for the full input circuit. The input current relates to the ADC sampling frequency.
[3] The internal reference calibration and trimming are performed when the processor operates in normal mode with CD = 0, when ADC is enabled and converting, when IDACs are all on, and when VDACs are on. V_{REF} accuracy can vary under other operating conditions.
[4] Measured using the following box method:

$$\frac{V_{REF}\ Maximum(at\ Any\ Temperature) - V_{REF}\ Minimum(at\ Any\ Temperature)}{2.5 \times (Temperature\ Maximum - Temperature\ Minimum)} \times 1^6$$

[5] VDAC linearity specifications are calculated with following ranges:
VDAC0 and VDAC1 = +150 mV to +2.699 V
VDAC2 and VDAC3: −150 mV to −4.22 V
VDAC4 and VDAC5: +150 mV to +2.98 V
VDAC6: +150 mV to +4.747 V
VDAC7: +150 mV to +4.297 V
[6] Analog Devices, Inc., production IDAC full-scale trimming conditions include PVDD_IDACx pin voltage = 0.7 V, all IDACs on.
[7] The long-term stability specifications is noncumulative. The drift in subsequent 1000 hour periods is significantly lower than in the first 1000 hour period.
[8] For all VDAC specifications for VDAC0, VDAC1, VDAC4, and VDAC5, DACxCON[10:9] = 11.
[9] VDACx minimum and maximum limits apply to the internal reference only (DACxCON[1:0] = 00_b). AVDDx supply valid only with typical specifications.
[10] The average current from the GPIO pins must not exceed 3 mA per pin. See Figure 22.

TIMING SPECIFICATIONS

I^2C Timing

Table 2. I^2C Timing in Standard Mode (100 kHz)

Parameter	Description	Slave Min	Slave Typ	Slave Max	Unit
t_L	SCLx low pulse width	4.7			µs
t_H	SCLx high pulse width	4.0			ns
t_{SHD}	Start condition hold time	4.0			µs
t_{DSU}	Data setup time	250			ns
t_{DHD}	Data hold time (SDAx held internally for 300 ns after falling edge of SCLx)	0		3.45	µs
t_{RSU}	Setup time for repeated start	4.7			µs
t_{PSU}	Stop condition setup time	4.0			µs
t_{BUF}	Bus free time between a stop condition and a start condition	4.7			µs
t_R	Rise time for both SCLx and SDAx			1	µs
t_F	Fall time for both SCLx and SDAx		15	300	ns
$t_{VD;DAT}$	Data valid time			3.45	µs
$t_{VD;ACK}$	Data valid acknowledge time			3.45	µs

Table 3. I^2C Timing in Fast Mode (400 kHz)

Parameter	Description	Slave Min	Slave Typ	Slave Max	Unit
t_L	SCLx low pulse width	1.3			µs
t_H	SCLx high pulse width	0.6			ns
t_{SHD}	Start condition hold time	0.3			µs
t_{DSU}	Data setup time	100			ns
t_{DHD}	Data hold time (SDAx held internally for 300 ns after falling edge of SCLx)	0			µs
t_{RSU}	Setup time for repeated start	0.6			µs
t_{PSU}	Stop condition setup time	0. 3			µs
t_{BUF}	Bus free time between a stop condition and a start condition	1.3			µs
t_R	Rise time for both SCLx and SDAx	20		300	ns
t_F	Fall time for both SCLx and SDAx		15	300	ns
$t_{VD;DAT}$	Data valid time			0.9	µs
$t_{VD;ACK}$	Data valid acknowledge time			0.9	µs

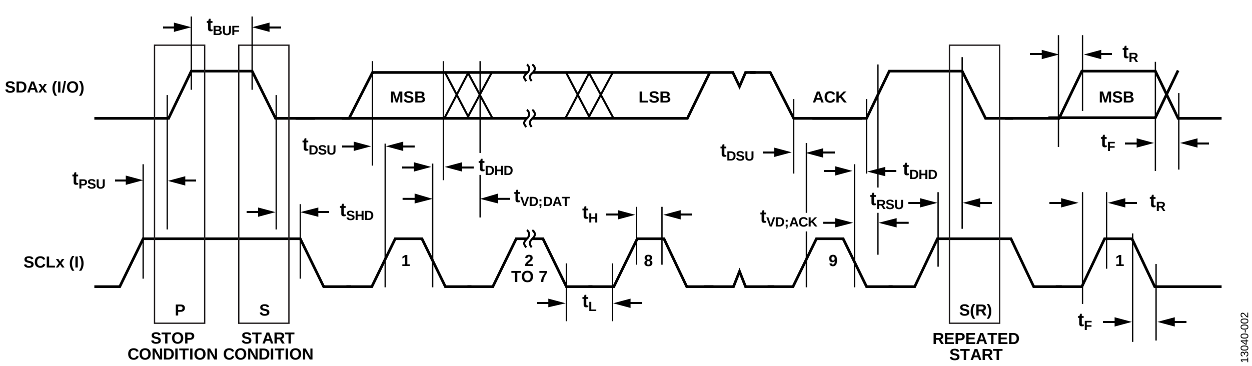


Figure 2. I^2C Compatible Interface Timing

Table 7. SPI Slave Mode Timing (Phase Mode = 0)

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS0}}/t_{\overline{CS1}}$	$\overline{CS0}/\overline{CS1}$ to SCLKx edge	10			ns
$t_{\overline{CSM}}$	$\overline{CS0}/\overline{CS1}$ high time between active periods	SCLKx			ns
t_{SL}	SCLKx low pulse width		(SPIxDIV[1] + 1) × t_{HCLK}[2]		ns
t_{SH}	SCLKx high pulse width		(SPIxDIV[1] + 1) × t_{HCLK}[2]		ns
t_{DAV}	Data output valid after SCLKx edge		20		ns
t_{DSU}	Data input setup time before SCLKx edge	10			ns
t_{DHD}	Data input hold time after SCLKx edge	10			ns
t_{DF}	Data output fall time		25		ns
t_{DR}	Data output rise time		25		ns
t_{SR}	SCLKx rise time	1			ns
t_{SF}	SCLKx fall time	1			ns
t_{DOCS}	Data output valid after $\overline{CS0}/\overline{CS1}$ edge	20			ns
t_{SFS}	$\overline{CS0}/\overline{CS1}$ high after SCLKx edge	10			ns

[1] For SPI0, x is 0, and for SPI1, x is 1
[2] t_{HCLK} is the divided system clock, UCLK/CLKCON1[2:0].

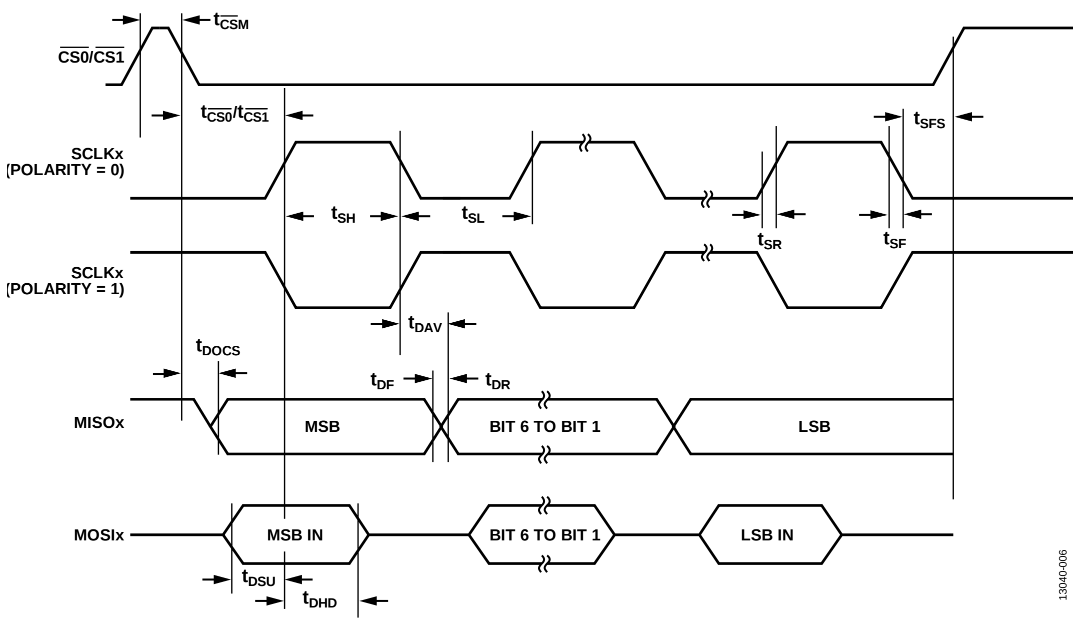


Figure 6. SPI Slave Mode Timing (Phase Mode = 0)

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
AV_{DD} to AGNDx	−0.3 V to +3.96 V
AV_{NEG} to AGNDx	−5.5 V to +0.3 V
$VDACV_{DD}$ to AGNDx	−0.3 V to +5.5 V
IOVDDx to DGNDx	−0.3 V to +3.96 V
Digital Input Voltage to DGNDx	−0.3 V to IOVDDx + 0.3 V
Digital Output Voltage to DGNDx	−0.3 V to IOVDDx + 0.3 V
Analog Inputs to AGNDx	−0.3 V to AV_{DD} + 0.3 V
Total Positive GPIO Pins Current	0 mA to 30 mA
Total Negative GPIO Pins Current	−30 mA to 0 mA
IDAC3 Pull-Down Voltage	AV_{NEG} − 0.3 V
IDAC3 Pull-Down Current	−100 mA
Operating Temperature Range	−10°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
ESD Rating, All Pins	
Human Body Model (HBM)	1 kV
Field-Induced Charged Device Model (FICDM)	1.25 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

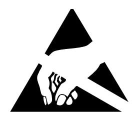
THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 9. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
112-Ball CSP_BGA	44.5	11	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

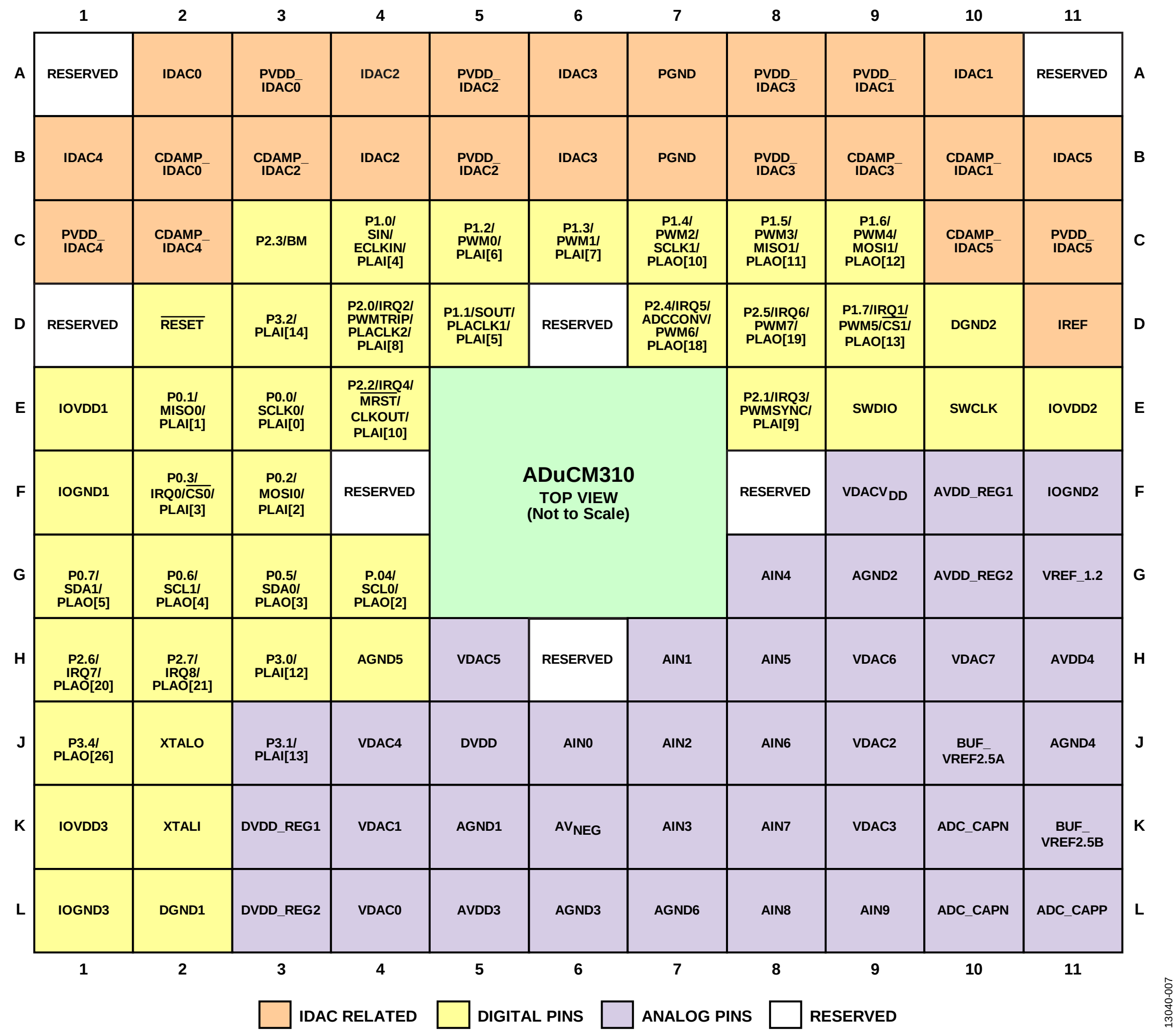


Figure 7. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
D2	$\overline{\text{RESET}}$	I	Reset Input (Active Low). An internal pull-up is included on this pin.
E3	P0.0/SCLK0/PLAI[0]	I/O	General-Purpose Input and Output Port 0.0/SPI0 Clock/Input to PLA Element 0. This pin defaults as an input with the internal pull-up resistor disabled.
E2	P0.1/MISO0/PLAI[1]	I/O	General-Purpose Input and Output Port 0.1/SPI0 Data Master Input-Slave Output/Input to PLA Element 1. This pin defaults as an input with the internal pull-up disabled.
F3	P0.2/MOSI0/PLAI[2]	I/O	General-Purpose Input and Output Port 0.2/SPI0 Data Master Output-Slave Input/Input of PLA Element 2. This pin defaults as an input with the internal pull-up disabled.
F2	P0.3/IRQ0/$\overline{\text{CS0}}$/PLAI[3]	I/O	General-Purpose Input and Output Port 0.3/External Interrupt Request 0/SPI0 Chip Select Input/Input of PLA Element 3. This pin defaults as an input with the internal pull-up disabled. If SPI0 is used, configure this pin as $\overline{\text{CS0}}$.
G4	P0.4/SCL0/PLAO[2]	I/O	General-Purpose Input and Output Port 0.4/I^{2}C Interface Clock for I2C0/Output of PLA Element 2. This pin defaults as an input with the internal pull-up disabled.

Pin No.	Mnemonic	Type[1]	Description
J3	P3.1/PLAI[13]	I/O	General-Purpose Input and Output Port 3.1/Input to PLA Element 13. This pin defaults as an input with the internal pull-up disabled.
D3	P3.2/PLAI[14]	I/O	General-Purpose Input and Output Port 3.2/Input to PLA Element 14. This pin defaults as an input with the internal pull-up disabled.
J1	P3.4/PLAO[26]	I/O	General-Purpose Input and Output Port 3.4/Output of PLA Element 26. This pin defaults as an input with the internal pull-up disabled.
E10	SWCLK	I	Serial Wire Debug Clock Input Pin.
E9	SWDIO	I/O	Serial Wire Debug Data Input/Output Input Pin.
G11	VREF_1.2	AO	1.2 V Reference Output. This pin cannot be used to source current externally. Connect this pin to AGND via a 470 nF capacitor.
D11	IREF	AI	This pin generates the reference current for the IDACs. Connect this pin to analog ground via a 5 ppm, 3.16 kΩ external resistor (R_{EXT}).
J6	AIN0	AI	Single-Ended or Differential Analog Input 0.
H7	AIN1	AI	Single-Ended or Differential Analog Input 1.
J7	AIN2	AI	Single-Ended or Differential Analog Input 2.
K7	AIN3	AI	Single-Ended or Differential Analog Input 3.
G8	AIN4	AI	Single-Ended or Differential Analog Input 4. This is also the input for the digital comparator.
H8	AIN5	AI	Single-Ended or Differential Analog Input 5.
J8	AIN6	AI	Single-Ended or Differential Analog Input 6.
K8	AIN7	AI	Single-Ended or Differential Analog Input 7.
L8	AIN8	AI	Single-Ended or Differential Analog Input 8.
L9	AIN9	AI	Single-Ended or Differential Analog Input 9.
L4	VDAC0	AO	12-Bit VDAC Output 0, 0 V to 3 V Range.
K4	VDAC1	AO	12-Bit VDAC Output 1, 0 V to 3 V Range.
J9	VDAC2	AO	12-Bit VDAC Output 2, −5 V to 0 V Range.
K9	VDAC3	AO	12-Bit VDAC Output 3, −5 V to 0 V Range.
J4	VDAC4	AO	12-Bit VDAC Output 4, 0 V to 3 V Range.
H5	VDAC5	AO	12-Bit VDAC Output 5, 0 V to 3 V Range.
H9	VDAC6	AO	12-Bit VDAC Output 6, 0 V to 5 V Range.
H10	VDAC7	AO	12-Bit VDAC Output 7, 0 V to 5 V Range.
A2	IDAC0	AO	IDAC0 (100 mA).
A3	PVDD_IDAC0	S	Power for IDAC0.
B2	CDAMP_IDAC0	AI	Damping Capacitor Pin for IDAC0. Connect this pin to the PVDD supply.
A10	IDAC1	AO	IDAC1 (100 mA).
A9	PVDD_IDAC1	S	Power for IDAC1.
B10	CDAMP_IDAC1	AI	Damping capacitor pin for IDAC1. Connect this pin to the PVDD supply.
B11	IDAC5	AO	IDAC5 (20 mA).
C11	PVDD_IDAC5	S	Power for IDAC5.
C10	CDAMP_IDAC5	AI	Damping capacitor pin for IDAC5. Connect this pin to the PVDD supply.
B1	IDAC4	AO	IDAC4 (20 mA).
C1	PVDD_IDAC4	S	Power for IDAC4.
C2	CDAMP_IDAC4	AI	Damping capacitor pin for IDAC4. Connect this pin to the PVDD supply.
A4, B4	IDAC2	AO	IDAC2 (200 mA).
A5, B5	PVDD_IDAC2	S	Power for IDAC2.
B3	CDAMP_IDAC2	AI	Damping Capacitor for IDAC2. Connect this pin to the PVDD supply.
A6, B6	IDAC3	AO	IDAC3 (250 mA).
A8, B8	PVDD_IDAC3	S	Power for IDAC3.
B9	CDAMP_IDAC3	AI	Damping Capacitor Pin for IDAC3. Connect this pin to the PVDD supply.
A7, B7	PGND	S	Power Supply Ground of the IDACs.
K5, G9, L6, J11, H4, L7	AGND1, AGND2, AGND3, AGND4, AGND5, AGND6	S	Analog Ground Pins.

Pin No.	Mnemonic	Type[1]	Description
J5	DVDD	S	Digital Supply Pin. This pin is the supply for the 16 MHz oscillator, PLL, POR, and digital core, including the flash that requires a regulated 1.8 V supply and a 3 V supply.
F9	$VDACV_{DD}$	S	5 V Analog Supply Pin.
L5, H11	AVDD3, AVDD4	S	Analog Supply Pin (3.3 V).
K3	DVDD_REG1	S	Output of 2.5 V on Chip Low Dropout (LDO) Regulator. Connect a 470 nF capacitor to this pin and DGND. This regulator supplies the inter-die digital interface.
L3	DVDD_REG2	S	Output of 1.8 V on chip LDO regulator. Connect a 470 nF capacitor to this pin and DGND. This regulator supplies flash and the Cortex-M3 processor.
F10	AVDD_REG1	S	Output of 2.5 V on chip LDO regulator. Connect a 470 nF capacitor to this pin and DGND. This regulator supplies the ADC.
G10	AVDD_REG2	S	Output of 2.5 V on chip LDO regulator. Connect a 470 nF capacitor to this pin and DGND. This regulator supplies the IDACs.
K6	AV_{NEG}	S	−5 V Supply Pin.
E1	IOVDD1	S	3.3 V GPIO Supply Pin.
L2, D10	DGND1, DGND2	S	Digital Ground Pins.
E11, K1	IOVDD2, IOVDD3	S	3.3 V GPIO Supply Pins.
F1, F11, L1	IOGND1, IOGND2, IOGND3	S	GPIO Ground Pins.
J2	XTALO	DO	Output from the Crystal Oscillator Inverter. If an external crystal is not used, leave this pin unconnected.
K2	XTALI	DI	Input to the Crystal Oscillator Inverter and Input to the Internal Clock Generator Circuits. If an external crystal is not used, connect this pin to the DGND system ground.
J10	BUF_VREF2.5A	AO	Buffered 2.5 V Bias, Maximum Load = 1.2 mA. Connect this pin to AGND via a 100 nF capacitor.
K11	BUF_VREF2.5B	AO	Buffered 2.5 V Bias, Maximum Load = 1.2 mA. Connect this pin to AGND via a 100 nF capacitor.
K10, L10	ADC_CAPN	S	Decoupling Capacitor Connection for ADC Reference Buffer. Connect this pin to AGND.
L11	ADC_CAPP	S	Decoupling Capacitor Connection for ADC Reference Buffer. Connect this pin to a 4.7 µF capacitor and connect the other side of the capacitor to the AGND and the ADC_CAPN pins.
A1, A11, D1, F4, F8, D6, H6	RESERVED		Reserved. Do not connect to this pin.

[1] I is input, I/O is input/output, AO is analog output, AI is analog input, S is supply, DO is digital output, and DI is digital input.

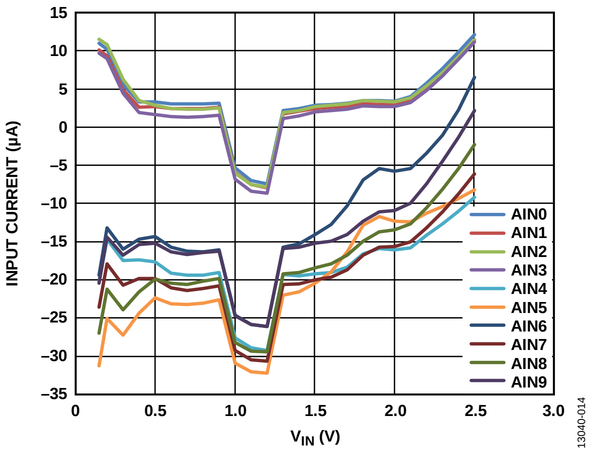


Figure 14. Input Current vs. V_{IN}, V_{DD} = 3.3 V, T_A = 25°C, Buffered Mode, 100 kSPS

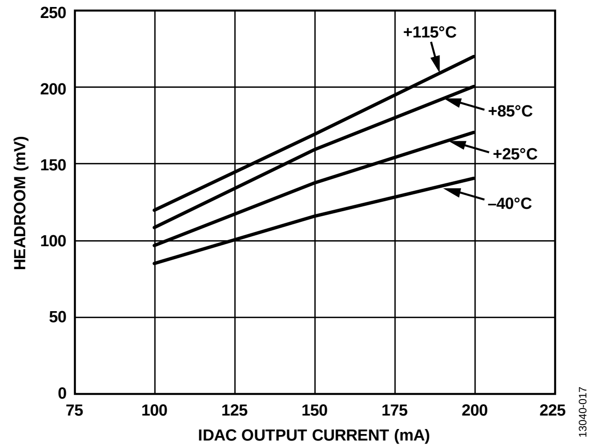


Figure 17. Typical IDAC2 PVDD_IDAC2 Pin Voltage Headroom vs. Output Current for Different Temperatures; PV_{DD} = 1.8 V

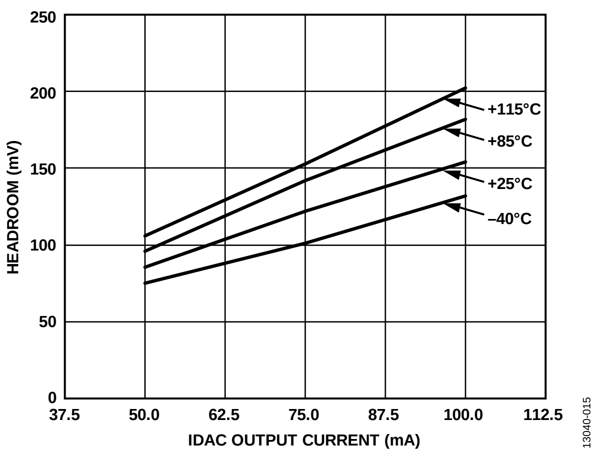


Figure 15. Typical IDAC0 PVDD_IDAC0 Pin Voltage Headroom vs. Output Current for Different Temperatures; PV_{DD} = 1.8 V

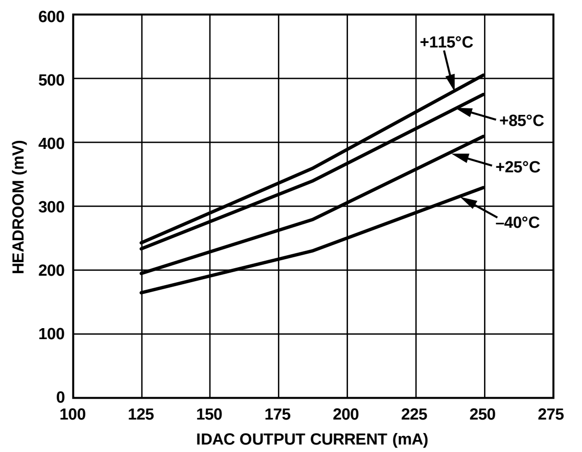


Figure 18. Typical IDAC3 PVDD_IDAC3 Pin Voltage Headroom vs. Output Current for Different Temperatures; PV_{DD} = 1.8 V

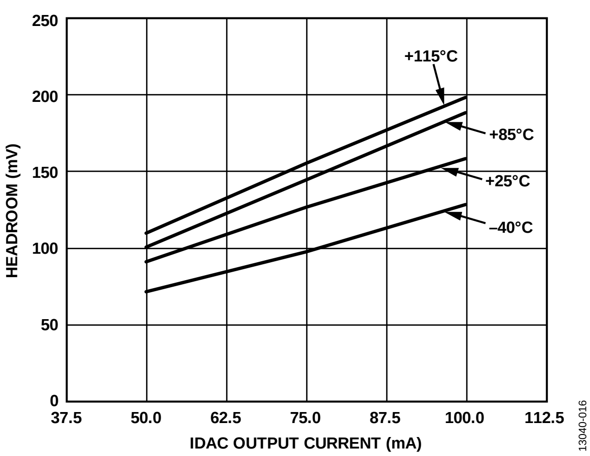


Figure 16. Typical IDAC1 PVDD_IDAC1 Pin Voltage Headroom vs. Output Current for Different Temperatures; PV_{DD} = 1.8 V

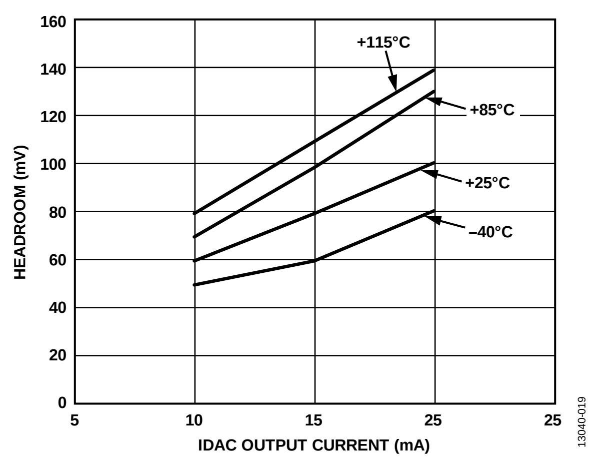


Figure 19. Typical IDAC4 PVDD_IDAC4 Pin Voltage Headroom vs. Output Current for Different Temperatures; PV_{DD} = 1.8 V

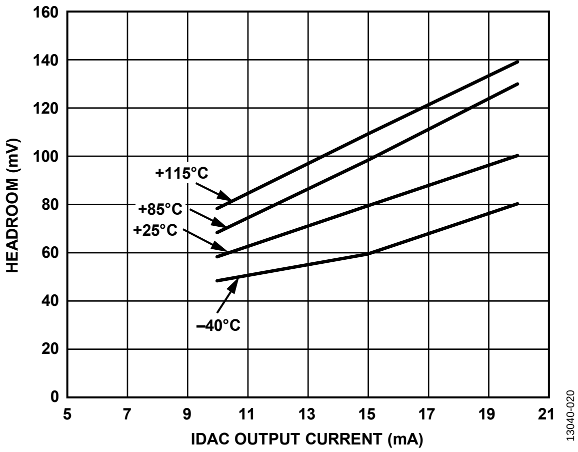


Figure 20. Typical IDAC5 PVDD_IDAC5 Pin Voltage Headroom vs. Output Current for Different Temperatures, PV_{DD} = 1.8 V

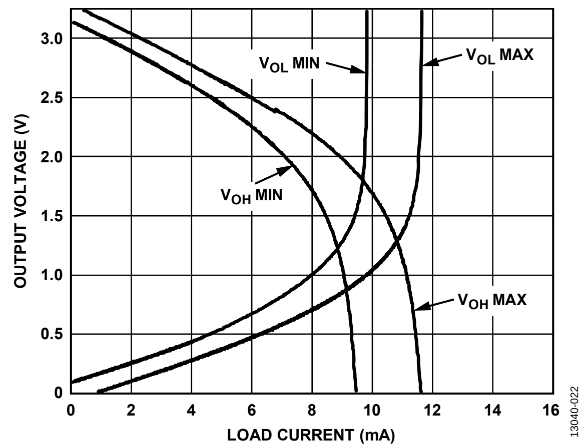


Figure 22. Typical Output Voltage vs. Load Current

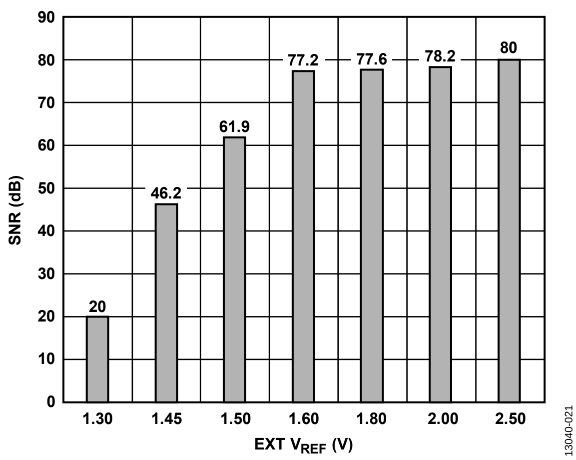


Figure 21. ADC SNR vs. External Reference Voltage (EXT V_{REF})

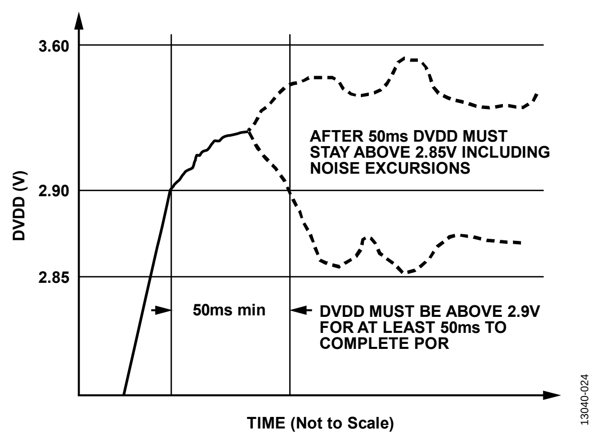


Figure 23. DVDD Power-On Requirements

RECOMMENDED CIRCUIT AND COMPONENT VALUES

Figure 24 shows a typical connection diagram for the ADuCM310.

There are four digital supply balls: IOVDD1, IOVDD2, IOVDD3, and DVDD. Decouple these balls with a 0.1 μF capacitor placed as close as possible to each of the four balls and a 10 μF capacitor at the supply source. Similarly, the analog supply pins, AVDD3 and AVDD4, each require a 0.1 μF capacitor placed as close as possible to each ball with a 10 μF capacitor at the supply source.

The IDACs source their output currents from the PV_{DD} supply balls, PVDD_IDACx. Connect a 100 nF capacitor close to each PVDD supply ball. Place at least one 10 μF capacitor at the source of the PVDD supply (PVDD_IDACx balls).

The IDAC output filters depend on a 10 nF capacitor placed between the CDAMP_IDACx ball and the PVDD_IDACx ball.

The ADC reference requires a 4.7 μF capacitor between the ADC_CAPN and ADC_CAPP balls. Directly connect ADC_CAPN to the analog ground (AGND).

The ADuCM310 contains four internal regulators. These regulators require external decoupling capacitors. The DVDD_REG1 and DVDD_REG2 balls each requires a 0.47 μF capacitor to the digital ground (DGND). The AVDD_REG1 and AVDD_REG2 balls each requires a decoupling capacitor to the AGND.

To generate an accurate and low drift reference current, connect the IREF ball to the analog ground via a low parts per million (ppm) 3.16 kΩ resistor.

Connect the VREF_1.2 ball to AGND via a 0.47 μF capacitor.

See Figure 24 for more details.

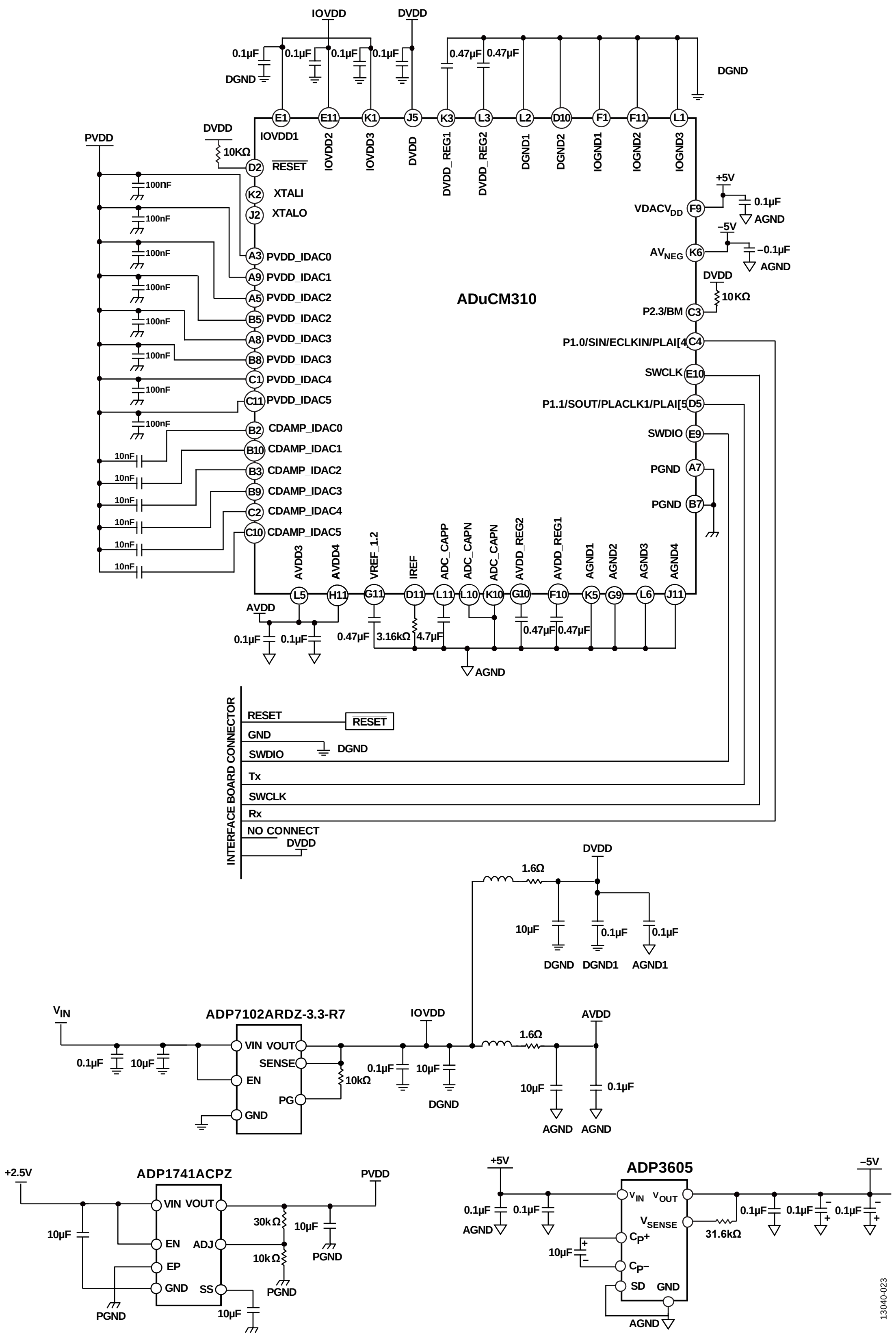


Figure 24. Typical Connection Diagram

OUTLINE DIMENSIONS

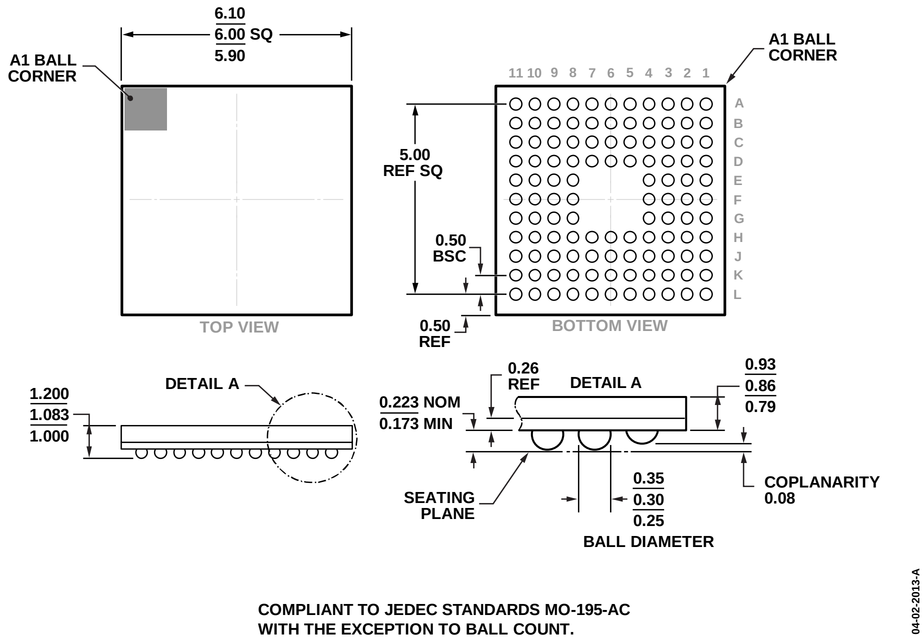


Figure 25. 112-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-112-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADuCM310BBCZ	−10°C to +85°C	112-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-112-4
ADuCM310BBCZ-RL	−10°C to +85°C	112-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-112-4
EVAL-ADuCM310QSPZ		Evaluation Board with QuickStart Development System	

[1] Z = RoHS Compliant Part.

I^2C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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