Renesas Electronics America Inc - R5F2138AWJFP#U0 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	75
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 20x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2138awjfp-u0

Table 1.2 Specifications for R8C/38W Group (2)

Item	Function	Specification
Timer	Timer RA0	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RA1	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits (with 4 capture/compare registers) × 1 Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits (with 4 capture/compare registers) × 2 Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits × 1 Output compare mode
	Timer RF	16 bits × 1 Input capture mode (input capture circuit), output compare mode (output compare circuit)
	Timer RG	16 bits × 1 Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder)
Serial Interface	UART0, 1	2 channels Clock synchronous serial I/O, UART
	UART2	1 channel Clock synchronous serial I/O, UART, I^2C mode (I^2C-bus), IE mode (IEbus), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1 channel
LIN Module		Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1)
CAN Module		1 channel, 16 Mailboxes (conforms to the ISO 11898-1)
A/D Converter		10-bit resolution × 20 channels, includes sample and hold function, with sweep mode
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • Background operation (BGO) function (data flash)
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)
Current Consumption		Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz)
Operating Ambient Temperature		-40 to 85°C (J version) -40 to 125°C (K version) (1)
Package		80-pin LQFP Package code: PLQP0080KB-A (previous code: 80P6Q-A)

Note:
1. Specify the K version if K version functions are to be used.

Table 1.8 Specifications for R8C/38Z Group (2)

Item	Function	Specification
Timer	Timer RA0	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RA1	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode
	Timer RB	8 bits (with 8-bit prescaler) × 1 Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode
	Timer RC	16 bits (with 4 capture/compare registers) × 1 Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin)
	Timer RD	16 bits (with 4 capture/compare registers) × 2 Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period)
	Timer RE	8 bits × 1 Output compare mode
	Timer RF	16 bits × 1 Input capture mode (input capture circuit), output compare mode (output compare circuit)
	Timer RG	16 bits × 1 Timer mode (input capture function, output compare function), PWM mode (output 1 pin), phase counting mode (available automatic measurement for the counts of 2-phase encoder)
Serial Interface	UART0, 1	2 channels Clock synchronous serial I/O, UART
	UART2	1 channel Clock synchronous serial I/O, UART, I^2C mode (I^2C-bus), IE mode (IEbus), multiprocessor communication function
Synchronous Serial Communication Unit (SSU)		1 channel
LIN Module		Hardware LIN: 2 (timer RA0, timer RA1, UART0, UART1)
A/D Converter		10-bit resolution × 20 channels, includes sample and hold function, with sweep mode
Flash Memory		• Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 100 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function
Operating Frequency/Supply Voltage		f(XIN) = 20 MHz (VCC = 2.7 to 5.5 V)
Current Consumption		Typ. 7 mA (VCC = 5.0 V, f(XIN) = 20 MHz)
Operating Ambient Temperature		-40 to 85°C (J version) -40 to 125°C (K version) (1)
Package		80-pin LQFP Package code: PLQP0080KB-A (previous code: 80P6Q-A)

Note:
1. Specify the K version if K version functions are to be used.

1.2 Product List

Table 1.9 lists Product List for R8C/38W Group, Table 1.10 lists Product List for R8C/38X Group, Table 1.11 lists Product List for R8C/38Y Group, and Table 1.12 lists Product List for R8C/38Z Group.

Table 1.9 Product List for R8C/38W Group **Current of Nov 2010**

Part No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21388WJFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	J version
R5F2138AWJFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080KB-A	
R5F2138CWJFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	
R5F21388WKFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	K version
R5F2138AWKFP	96 Kbytes	1 Kbyte × 4	8 Kbytes	PLQP0080KB-A	
R5F2138CWKFP	128 Kbytes	1 Kbyte × 4	10 Kbytes	PLQP0080KB-A	

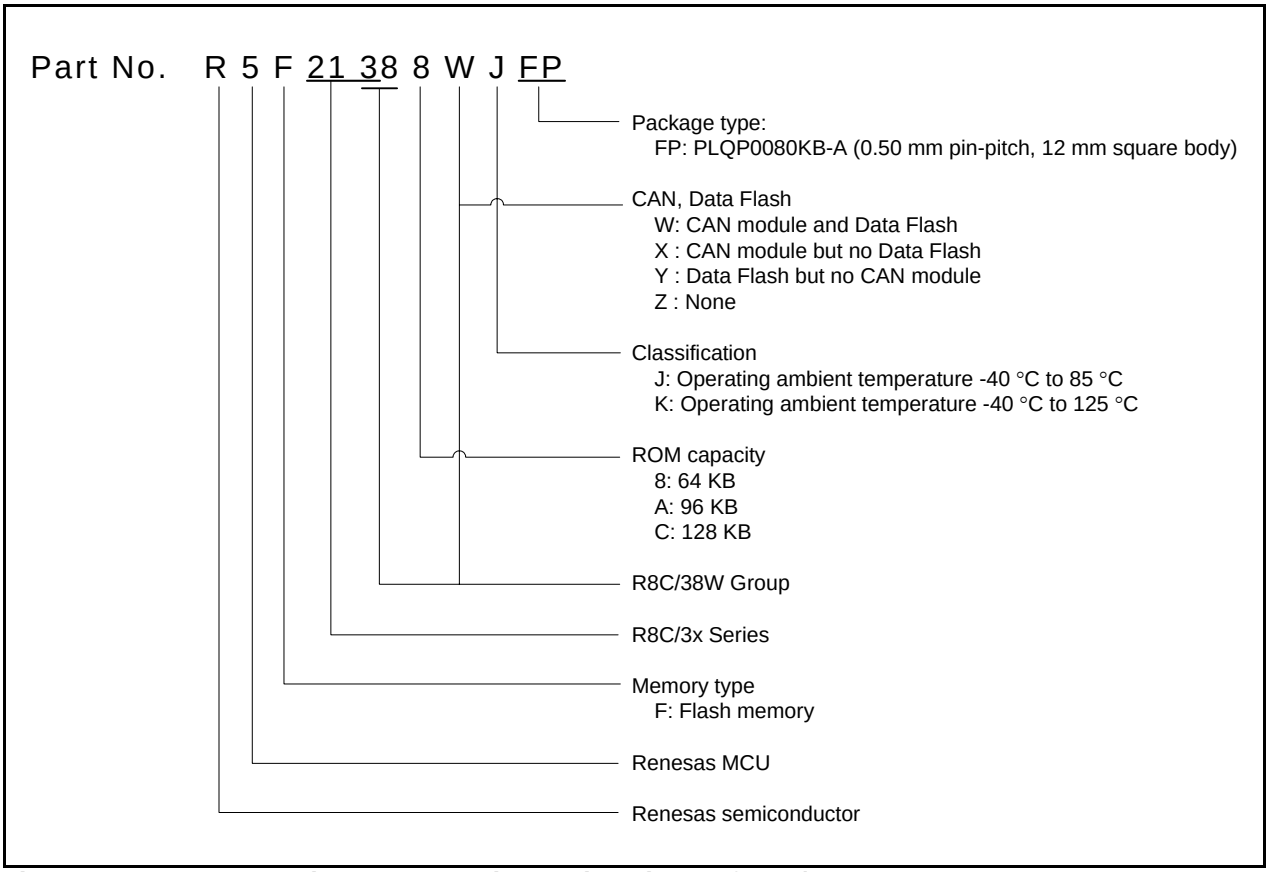


Figure 1.1 Part Number, Memory Size, and Package of R8C/38W Group

1.5 Pin Functions

Tables 1.15 and 1.16 list Pin Functions.

Table 1.15 Pin Functions (1)

Item	Pin Name	I/O Type	Description
Power supply input	VCC, VSS	I	Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins (1). To use an external clock, input it to the XOUT pin and leave the XIN pin open.
XIN clock output	XOUT	I/O	
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT4}}$	I	$\overline{\text{INT}}$ interrupt input pins.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer RA0 Timer RA1	TRAIO0, TRAIO1	I/O	Timer RA I/O pin
	TRAO0, TRAO1	O	Timer RA output pin
Timer RB	TRBO	O	Timer RB output pin
Timer RC	TRCCLK	I	External clock input pin
	TRCTRG	I	External trigger input pin
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Timer RC I/O pins
Timer RD	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1	I/O	Timer RD I/O pins
	TRDCLK	I	External clock input pin
Timer RE	TREO	O	Divided clock output pin
Timer RF	TRFO00, TRFO10, TRFO01, TRFO11, TRFO02, TRFO12	O	Timer RF output pins.
	TRFI	I	Timer RF input pin.
Timer RG	TRGIOA, TRGIOB	I/O	Timer RG I/O ports.
	TRGCLKA, TRGCLKB	I	External clock input pins.
Serial interface	CLK0, CLK1, CLK2	I/O	Transfer clock I/O pins
	RXD0, RXD1, RXD2	I	Serial data input pins
	TXD0, TXD1, TXD2	O	Serial data output pins
	$\overline{\text{CTS2}}$	I	Transmission control input pin
	$\overline{\text{RTS2}}$	O	Reception control output pin
	SCL2	I/O	I^2C mode clock I/O pin
	SDA2	I/O	I^2C mode data I/O pin
SSU	SSI	I/O	Data I/O pin
	$\overline{\text{SCS}}$	I/O	Chip-select signal I/O pin
	SSCK	I/O	Clock I/O pin
	SSO	I/O	Data I/O pin

I: Input O: Output I/O: Input and output

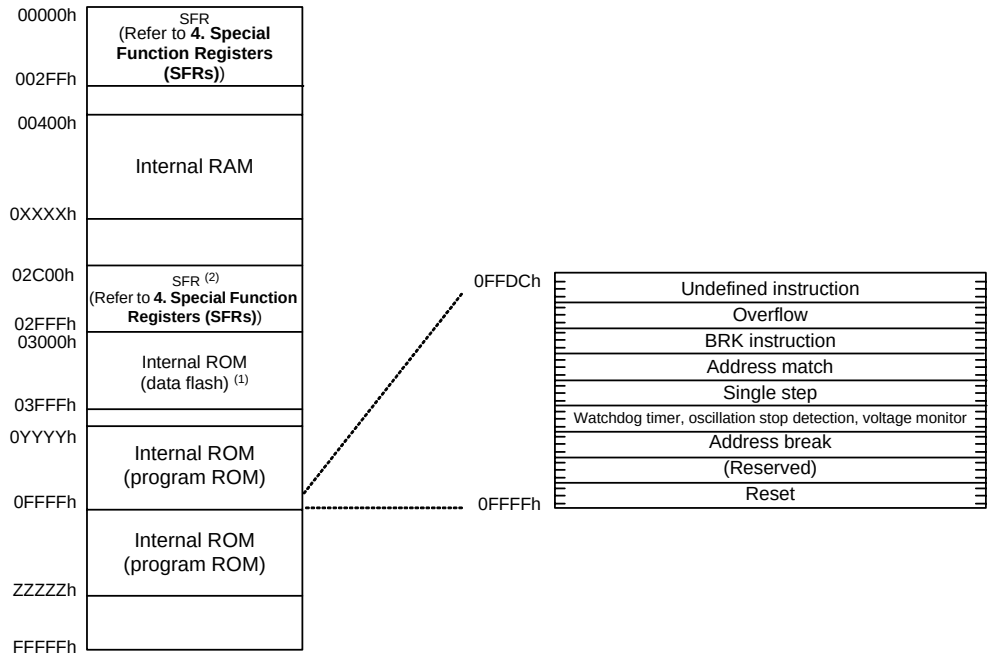
Note:

1. Refer to the oscillator manufacturer for oscillation characteristics.

3. Memory

3.1 R8C/38W Group

Figure 3.1 is a Memory Map of R8C/38W Group. The R8C/38W Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the CAN, DTC, and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



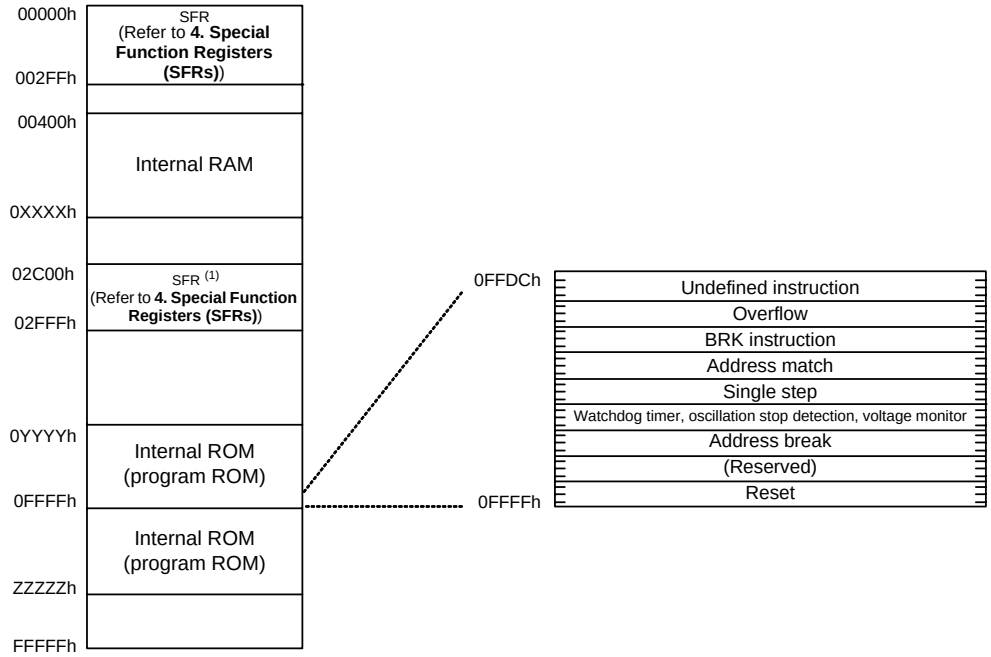
Notes:
1. The Data Flash memory indicates blocks A (1 Kbyte), B (1 Kbyte), C (1 Kbyte), and D (1 Kbyte).
2. The SFR areas for the CAN, DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21388WJFP, R5F21388WKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2138AWJFP, R5F2138AWKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2138CWJFP, R5F2138CWKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.1 Memory Map of R8C/38W Group

3.2 R8C/38X Group

Figure 3.2 is a Memory Map of R8C/38X Group. The R8C/38X Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the CAN, DTC, and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



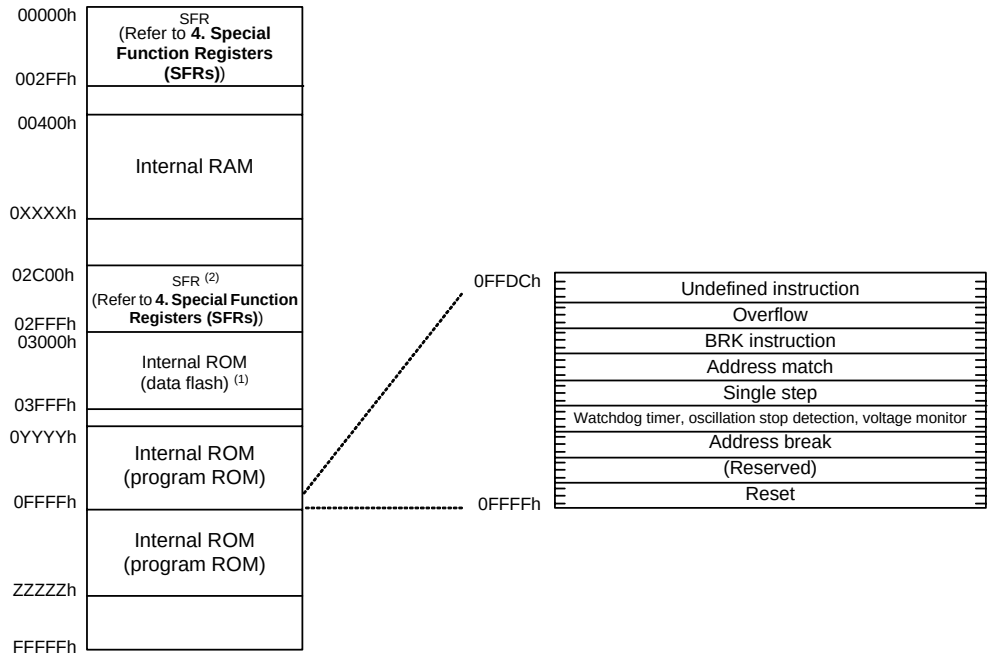
Notes:
1. The SFR areas for the CAN, DTC and other modules are allocated to addresses 02C00h to 02FFFh.
2. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21388XJFP, R5F21388XKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2138AXJFP, R5F2138AXKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2138CXJFP, R5F2138CXKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.2 Memory Map of R8C/38X Group

3.3 R8C/38Y Group

Figure 3.3 is a Memory Map of R8C/38Y Group. The R8C/38Y Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



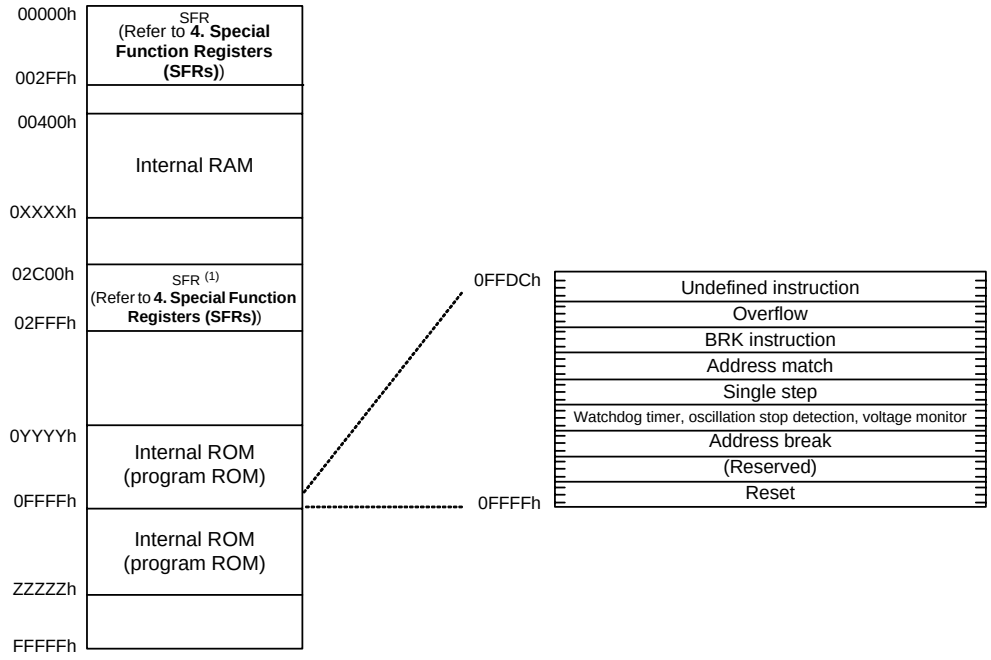
Notes:
1. The Data Flash memory indicates blocks A (1 Kbyte), B (1 Kbyte), C (1 Kbyte), and D (1 Kbyte).
2. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
3. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21388YJFP, R5F21388YKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2138AYJFP, R5F2138AYKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2138CYJFP, R5F2138CYKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.3 Memory Map of R8C/38Y Group

3.4 R8C/38Z Group

Figure 3.4 is a Memory Map of R8C/38Z Group. The R8C/38Z Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 64-Kbyte internal ROM area is allocated addresses 04000h to 13FFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 6-Kbyte internal RAM area is allocated addresses 00400h to 01BFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh (the SFR areas for the DTC and other modules). Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. The SFR areas for the DTC and other modules are allocated to addresses 02C00h to 02FFFh.
2. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21388ZJFP, R5F21388ZKFP	64 Kbytes	04000h	13FFFh	6 Kbytes	01BFFh
R5F2138AZJFP, R5F2138AZKFP	96 Kbytes	04000h	1BFFFh	8 Kbytes	023FFh
R5F2138CZJFP, R5F2138CZKFP	128 Kbytes	04000h	23FFFh	10 Kbytes	02BFFh

Figure 3.4 Memory Map of R8C/38Z Group

Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	After reset
2C70h	DTC Control Data 6	DTCD6	XXh
2C71h			XXh
2C72h			XXh
2C73h			XXh
2C74h			XXh
2C75h			XXh
2C76h			XXh
2C77h			XXh
2C78h	DTC Control Data 7	DTCD7	XXh
2C79h			XXh
2C7Ah			XXh
2C7Bh			XXh
2C7Ch			XXh
2C7Dh			XXh
2C7Eh			XXh
2C7Fh			XXh
2C80h	DTC Control Data 8	DTCD8	XXh
2C81h			XXh
2C82h			XXh
2C83h			XXh
2C84h			XXh
2C85h			XXh
2C86h			XXh
2C87h			XXh
2C88h	DTC Control Data 9	DTCD9	XXh
2C89h			XXh
2C8Ah			XXh
2C8Bh			XXh
2C8Ch			XXh
2C8Dh			XXh
2C8Eh			XXh
2C8Fh			XXh
2C90h	DTC Control Data 10	DTCD10	XXh
2C91h			XXh
2C92h			XXh
2C93h			XXh
2C94h			XXh
2C95h			XXh
2C96h			XXh
2C97h			XXh
2C98h	DTC Control Data 11	DTCD11	XXh
2C99h			XXh
2C9Ah			XXh
2C9Bh			XXh
2C9Ch			XXh
2C9Dh			XXh
2C9Eh			XXh
2C9Fh			XXh
2CA0h	DTC Control Data 12	DTCD12	XXh
2CA1h			XXh
2CA2h			XXh
2CA3h			XXh
2CA4h			XXh
2CA5h			XXh
2CA6h			XXh
2CA7h			XXh
2CA8h	DTC Control Data 13	DTCD13	XXh
2CA9h			XXh
2CAAh			XXh
2CABh			XXh
2CACh			XXh
2CADh			XXh
2CAEh			XXh
2CAFh			XXh

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	After reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
2D01h			
:			
2E00h	CAN0 Mailbox 0: Message ID	C0MB0	XXh
2E01h			XXh
2E02h			XXh
2E03h			XXh
2E04h			
2E05h	CAN0 Mailbox 0: Data length		XXh
2E06h	CAN0 Mailbox 0: Data field		XXh
2E07h			XXh
2E08h			XXh
2E09h			XXh
2E0Ah			XXh
2E0Bh			XXh
2E0Ch			XXh
2E0Dh			XXh
2E0Eh	CAN0 Mailbox 0: Time stamp		XXh
2E0Fh			XXh
2E10h	CAN0 Mailbox 1: Message ID	C0MB1	XXh
2E11h			XXh
2E12h			XXh
2E13h			XXh
2E14h			
2E15h	CAN0 Mailbox 1: Data length		XXh
2E16h	CAN0 Mailbox 1: Data field		XXh
2E17h			XXh
2E18h			XXh
2E19h			XXh
2E1Ah			XXh
2E1Bh			XXh
2E1Ch			XXh
2E1Dh			XXh
2E1Eh	CAN0 Mailbox 1: Time stamp		XXh
2E1Fh			XXh
2E20h	CAN0 Mailbox 2: Message ID	C0MB2	XXh
2E21h			XXh
2E22h			XXh
2E23h			XXh
2E24h			
2E25h	CAN0 Mailbox 2: Data length		XXh
2E26h	CAN0 Mailbox 2: Data field		XXh
2E27h			XXh
2E28h			XXh
2E29h			XXh
2E2Ah			XXh
2E2Bh			XXh
2E2Ch			XXh
2E2Dh			XXh
2E2Eh	CAN0 Mailbox 2: Time stamp		XXh
2E2Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.13 SFR Information (13) (1)

Address	Register	Symbol	After reset
2E30h	CAN0 Mailbox 3: Message ID	C0MB3	XXh
2E31h			XXh
2E32h			XXh
2E33h			XXh
2E34h			
2E35h	CAN0 Mailbox 3: Data length		XXh
2E36h	CAN0 Mailbox 3: Data field		XXh
2E37h			XXh
2E38h			XXh
2E39h			XXh
2E3Ah			XXh
2E3Bh			XXh
2E3Ch			XXh
2E3Dh			XXh
2E3Eh	CAN0 Mailbox 3: Time stamp		XXh
2E3Fh			XXh
2E40h	CAN0 Mailbox 4: Message ID	C0MB4	XXh
2E41h			XXh
2E42h			XXh
2E43h			XXh
2E44h			
2E45h	CAN0 Mailbox 4: Data length		XXh
2E46h	CAN0 Mailbox 4: Data field		XXh
2E47h			XXh
2E48h			XXh
2E49h			XXh
2E4Ah			XXh
2E4Bh			XXh
2E4Ch			XXh
2E4Dh			XXh
2E4Eh	CAN0 Mailbox 4: Time stamp		XXh
2E4Fh			XXh
2E50h	CAN0 Mailbox 5: Message ID	C0MB5	XXh
2E51h			XXh
2E52h			XXh
2E53h			XXh
2E54h			
2E55h	CAN0 Mailbox 5: Data length		XXh
2E56h	CAN0 Mailbox 5: Data field		XXh
2E57h			XXh
2E58h			XXh
2E59h			XXh
2E5Ah			XXh
2E5Bh			XXh
2E5Ch			XXh
2E5Dh			XXh
2E5Eh	CAN0 Mailbox 5: Time stamp		XXh
2E5Fh			XXh
2E60h	CAN0 Mailbox 6: Message ID	C0MB6	XXh
2E61h			XXh
2E62h			XXh
2E63h			XXh
2E64h			
2E65h	CAN0 Mailbox 6: Data length		XXh
2E66h	CAN0 Mailbox 6: Data field		XXh
2E67h			XXh
2E68h			XXh
2E69h			XXh
2E6Ah			XXh
2E6Bh			XXh
2E6Ch			XXh
2E6Dh			XXh
2E6Eh	CAN0 Mailbox 6: Time stamp		XXh
2E6Fh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.14 SFR Information (14) (1)

Address	Register	Symbol	After reset
2E70h	CAN0 Mailbox 7: Message ID	C0MB7	XXh
2E71h			XXh
2E72h			XXh
2E73h			XXh
2E74h			
2E75h	CAN0 Mailbox 7: Data length		XXh
2E76h	CAN0 Mailbox 7: Data field		XXh
2E77h			XXh
2E78h			XXh
2E79h			XXh
2E7Ah			XXh
2E7Bh			XXh
2E7Ch			XXh
2E7Dh			XXh
2E7Eh	CAN0 Mailbox 7: Time stamp		XXh
2E7Fh			XXh
2E80h	CAN0 Mailbox 8: Message ID	C0MB8	XXh
2E81h			XXh
2E82h			XXh
2E83h			XXh
2E84h			
2E85h	CAN0 Mailbox 8: Data length		XXh
2E86h	CAN0 Mailbox 8: Data field		XXh
2E87h			XXh
2E88h			XXh
2E89h			XXh
2E8Ah			XXh
2E8Bh			XXh
2E8Ch			XXh
2E8Dh			XXh
2E8Eh	CAN0 Mailbox 8: Time stamp		XXh
2E8Fh			XXh
2E90h	CAN0 Mailbox 9: Message ID	C0MB9	XXh
2E91h			XXh
2E92h			XXh
2E93h			XXh
2E94h			
2E95h	CAN0 Mailbox 9: Data length		XXh
2E96h	CAN0 Mailbox 9: Data field		XXh
2E97h			XXh
2E98h			XXh
2E99h			XXh
2E9Ah			XXh
2E9Bh			XXh
2E9Ch			XXh
2E9Dh			XXh
2E9Eh	CAN0 Mailbox 9: Time stamp		XXh
2E9Fh			XXh
2EA0h	CAN0 Mailbox 10: Message ID	C0MB10	XXh
2EA1h			XXh
2EA2h			XXh
2EA3h			XXh
2EA4h			
2EA5h	CAN0 Mailbox 10: Data length		XXh
2EA6h	CAN0 Mailbox 10: Data field		XXh
2EA7h			XXh
2EA8h			XXh
2EA9h			XXh
2EAAh			XXh
2EABh			XXh
2EACh			XXh
2EADh			XXh
2EAEh	CAN0 Mailbox 10: Time stamp		XXh
2EAFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 5.2 Recommended Operating Conditions (1)

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage					2.7	–	5.5	V
V_{SS}/AV_{SS}	Supply voltage					–	0	–	V
V_{IH}	Input “H” voltage	Other than CMOS input				0.8 V_{CC}	–	V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.5 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.55 V_{CC}	–	V_{CC}	V
				Input level selection : 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.65 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.7 V_{CC}	–	V_{CC}	V
				Input level selection : 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.85 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.85 V_{CC}	–	V_{CC}	V
		External clock input (XOUT)				1.2	–	V_{CC}	V
V_{IL}	Input “L” voltage	Other than CMOS input				0	–	0.2 V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.2 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.2 V_{CC}	V
				Input level selection : 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.4 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.3 V_{CC}	V
				Input level selection : 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.55 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.45 V_{CC}	V
		External clock input (XOUT)				0	–	0.4	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$				–	–	–80	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$				–	–	–40	mA
$I_{OH(peak)}$	Peak output “H” current					–	–	–10	mA
$I_{OH(avg)}$	Average output “H” current					–	–	–5	mA
$I_{OL(sum)}$	Peak sum output “L” current	Sum of all pins $I_{OL(peak)}$				–	–	80	mA
$I_{OL(sum)}$	Average sum output “L” current	Sum of all pins $I_{OL(avg)}$				–	–	40	mA
$I_{OL(peak)}$	Peak output “L” current					–	–	10	mA
$I_{OL(avg)}$	Average output “L” current					–	–	5	mA
$f_{(XIN)}$	XIN clock input oscillation frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
fOCO40M	Count source for timer RC, timer RD, or timer RG				2.7 V ≤ V_{CC} ≤ 5.5 V	32	–	40	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
–	System clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
$f_{(BCLK)}$	CPU clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz

Notes:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.

Table 5.4 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		V_{ref} = AV_{CC}		–	–	10	Bit
–	Absolute accuracy	10-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	–	–	±3	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	–	–	±5	LSB
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0 to AN7 input, AN8 to AN11 input, AN12 to AN19 input	–	–	±2	LSB
ϕAD	A/D conversion clock		4.0 ≤ V_{ref} = AV_{CC} = ≤ 5.5 (2)		2	–	20	MHz
			2.7 ≤ V_{ref} = AV_{CC} = ≤ 5.5 (2)		2	–	10	MHz
–	Tolerance level impedance				–	3	–	kΩ
I_{vref}	V_{ref} current		V_{CC} = 5.0 V, XIN = f1 = ϕAD = 20 MHz		–	45	–	µA
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.8	–	–	µs
V_{ref}	Reference voltage				2.7	–	AV_{CC}	V
V_{IA}	Analog input voltage (3)				0	–	V_{ref}	V
OCVREF	On-chip reference voltage		2 MHz ≤ ϕAD ≤ 4 MHz		1.14	1.34	1.54	V

Notes:
1. V_{CC}/AV_{CC} = V_{ref} = 2.7 to 5.5 V, V_{SS} = 0 V at T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-consumption current mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.6 Flash Memory (Data flash Block A to Block D) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance (2)		10,000 (3)	–	–	times
–	Byte program time (program/erase endurance ≤ 1,000 times)		–	160	950	µs
–	Byte program time (program/erase endurance > 1,000 times)		–	300	950	µs
–	Block erase time (program/erase endurance ≤ 1,000 times)		–	0.2	1	s
–	Block erase time (program/erase endurance > 1,000 times)		–	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	3+CPU clock × 3 cycles	ms
–	Interval from erase start/restart until following suspend request		0	–	–	µs
–	Time from suspend until erase restart		–	–	30+CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		–	–	30+CPU clock × 1 cycle	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		–40	–	85 (J version) 125 (K version)	°C
–	Data hold time (7)	Ambient temperature = 55 °C (8)	20	–	–	year

Notes:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version), unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100, 1,000, 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
7. The data hold time includes time that the power supply is off or the clock is not supplied.
8. This data hold time includes 3,000 hours in Ta = 125°C and 7,000 hours in Ta = 85°C.

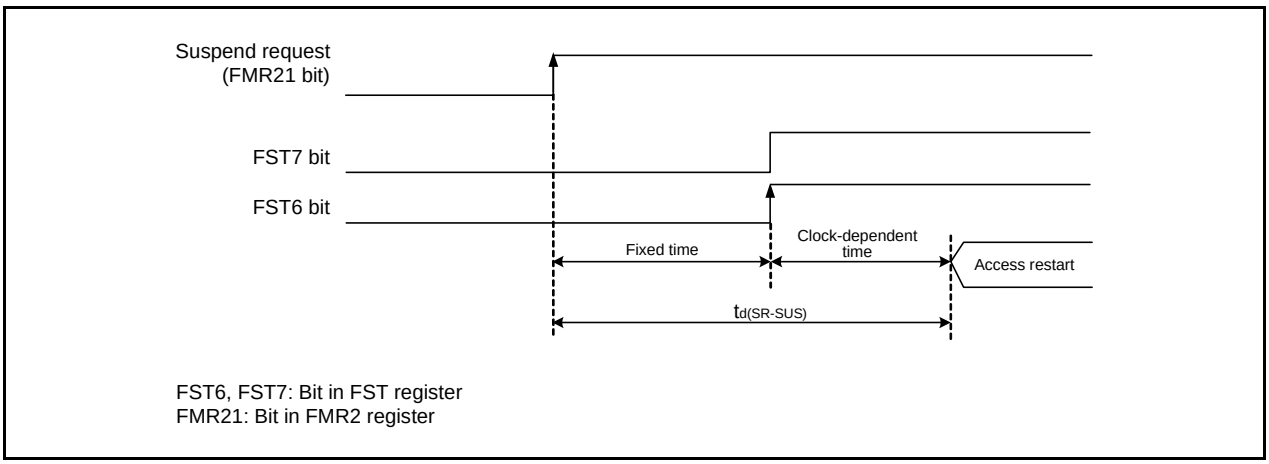


Figure 5.2 Time delay until Suspend

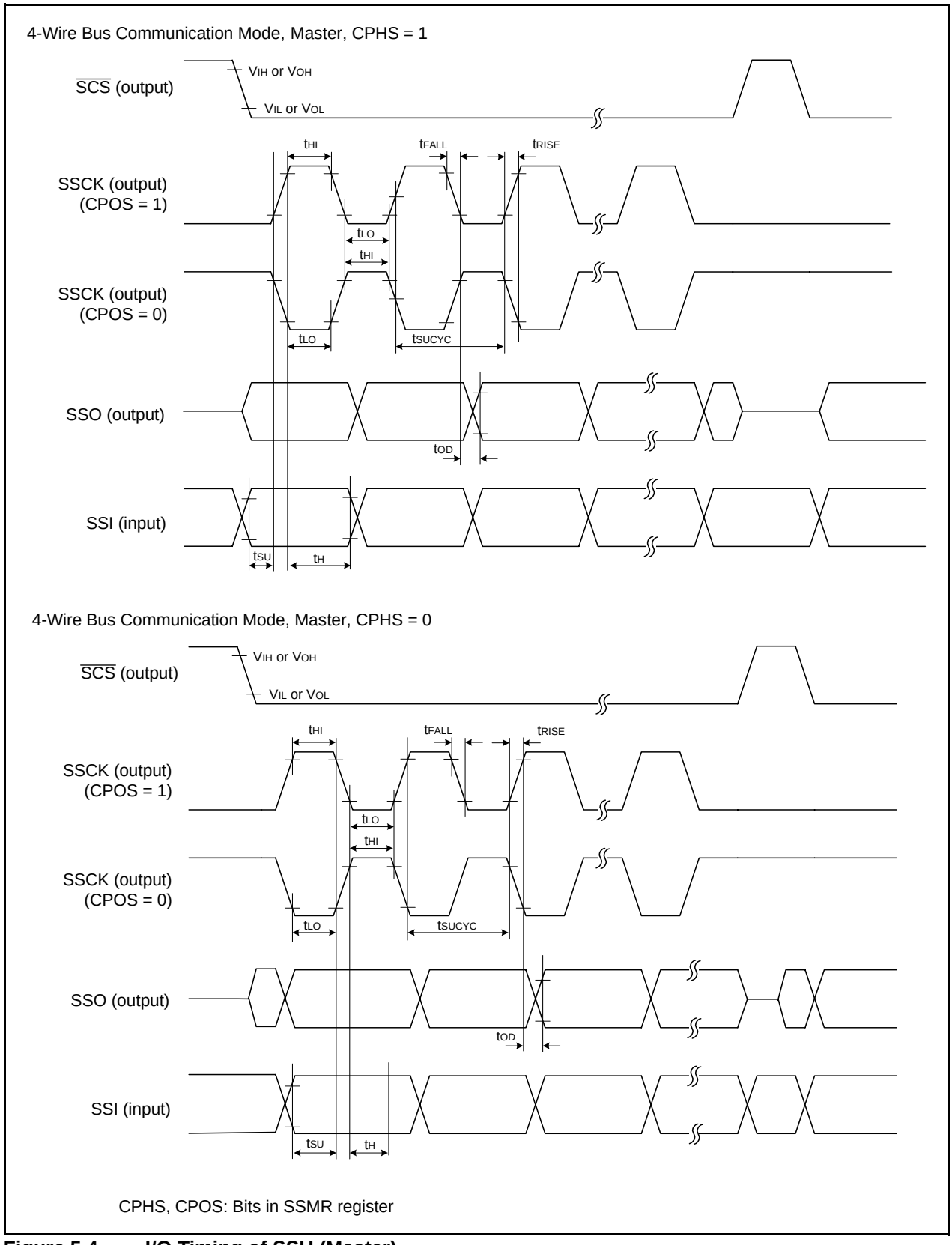


Figure 5.4 I/O Timing of SSU (Master)

Table 5.15 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	I_{OH} = –5 mA	V_{CC} – 2.0	–	V_{CC}	V
			I_{OH} = –200 μA	V_{CC} – 0.3	–	V_{CC}	V
		XOUT	I_{OH} = –200 μA	1.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Other than XOUT	I_{OL} = 5 mA	–	–	2.0	V
			I_{OL} = 200 μA	–	–	0.45	V
		XOUT	I_{OH} = –200 μA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRAIO0, TRAIO1, TRBO, TRCIOA to TRCIOD, TRDIOA0 to TRDIOD0, TRDIOA1 to TRDIOD1, TRFI, TRGIOA, TRGIOB, TRCCLK, TRDCLK, TRGCLKA, $\overline{TRGCLKB}$, TRCTRG, $\overline{ADTRG}$, RXD0 to RXD2, CLK0 to CLK2, SSI, SCL2, SDA2, SSO		0.1	1.2	–	V
		$\overline{RESET}$		0.1	1.2	–	V
I_{IH}	Input “H” current		VI = 5 V, V_{CC} = 5.0 V	–	–	1.0	μA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5.0 V	–	–	–1.0	μA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 5.0 V	25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN		–	0.3	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode	2.0	–	–	V

Note:
1. 4.2 V ≤ V_{CC} ≤ 5.5 V at T_{opr} = –40 to 85°C (J version) / –40 to 125°C (K version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.21 Serial Interface

Symbol	Parameter	Condition	Standard		Unit
			Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	When external clock selected	200	–	ns
$t_{W(CKH)}$	CLKi input “H” width		100	–	ns
$t_{W(CKL)}$	CLKi input “L” width		100	–	ns
$t_{d(C-Q)}$	TXDi output delay time		–	90	ns
$t_{h(C-Q)}$	TXDi hold time		0	–	ns
$t_{su(D-C)}$	RXDi input setup time		10	–	ns
$t_{h(C-D)}$	RXDi input hold time		90	–	ns
$t_{d(C-Q)}$	TXDi output delay time	When internal clock selected	–	10	ns
$t_{su(D-C)}$	RXDi input setup time		90	–	ns
$t_{h(C-D)}$	RXDi input hold time		90	–	ns

i = 0 to 2

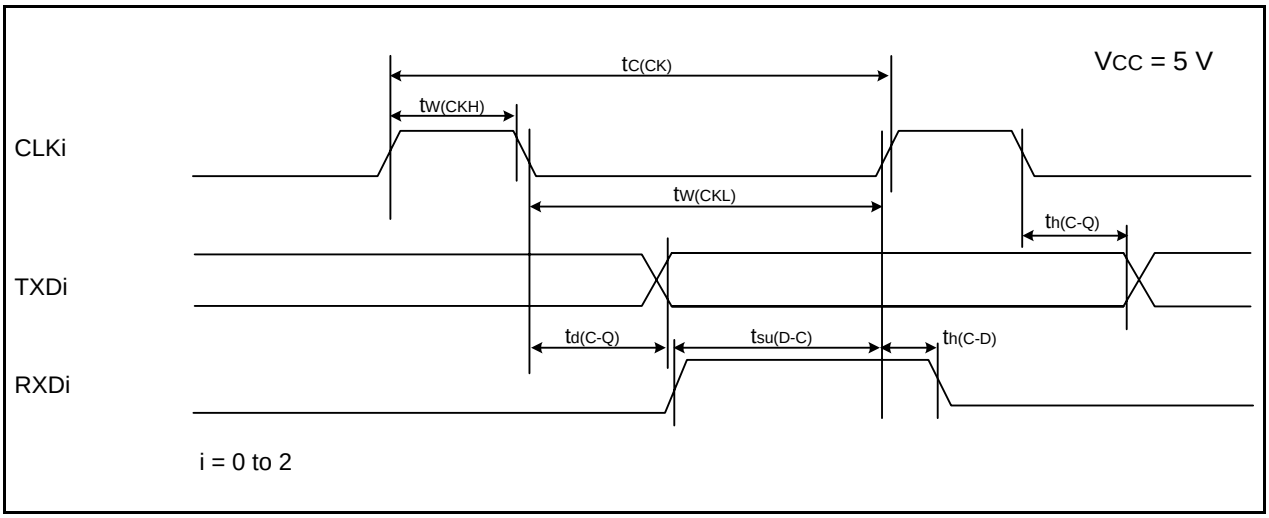


Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.22 External Interrupt $\overline{INTi}$ (i = 0 to 4) Input, Key Input Interrupt $\overline{KIi}$ (i = 0 to 3)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input “H” width, $\overline{KIi}$ input “H” width	250 (1)	–	ns
$t_{W(INL)}$	$\overline{INTi}$ input “L” width, $\overline{KIi}$ input “L” width	250 (2)	–	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

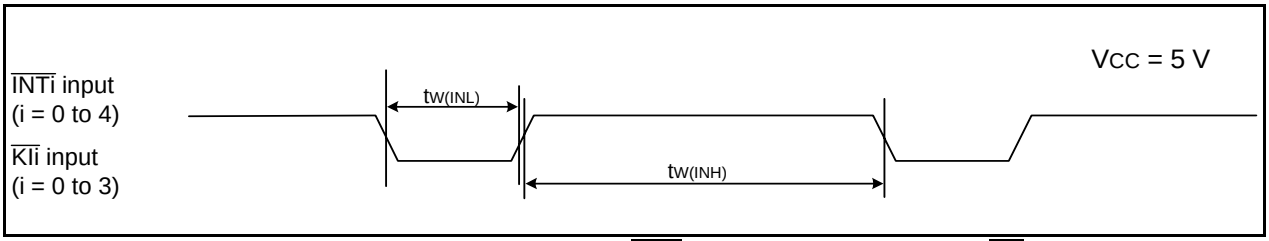


Figure 5.11 Input Timing for External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIi}$ when Vcc = 5 V

REVISION HISTORY	R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	May 31, 2010	—	First Edition issued
1.00	Nov 24, 2010	All	“Preliminary” and “Under development” deleted
		14	Figure 1.5 “Voltage detection circuit” added
		28	Table 4.2 006Ch, 006Dh, 0072h and 0073h revised
		32, 38 to 43	Table 4.6, Tables 4.12 to 4.17 “After Reset” notation revised
		46	Table 5.3 “VI > VSS” → “VI < VSS”, Note 1 revised
		47	Table 5.4 t_{SAMP} revised
		48	Table 5.5 “1,000 times” → “100 times”
		57	Table 5.15 “V_{CC} = 5.0 V” added
		60	Figure 5.9 revised
		61	Table 5.21 revised
		62	Table 5.23 “[2.7 V ≤ Vcc ≤ 4.2 V]” → “[2.7 V ≤ Vcc < 4.2 V]”, “V_{CC} = 3.0 V” added
		63, 64	Tables 5.24 and 5.25 “[2.7 V ≤ Vcc ≤ 3.3 V]” → “[2.7 V ≤ Vcc < 3.3 V]”
		65	Figure 5.14 revised
		66	Table 5.29 revised