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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/20MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LQFP
Supplier Device Package	44-VQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/atmel/at80c32x2-rltum

SFR Mapping

The Special Function Registers (SFRs) of the TS80C52X2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- Interrupt system registers: IE, IP, IPH
- Others: AUXR, CKCON

Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.

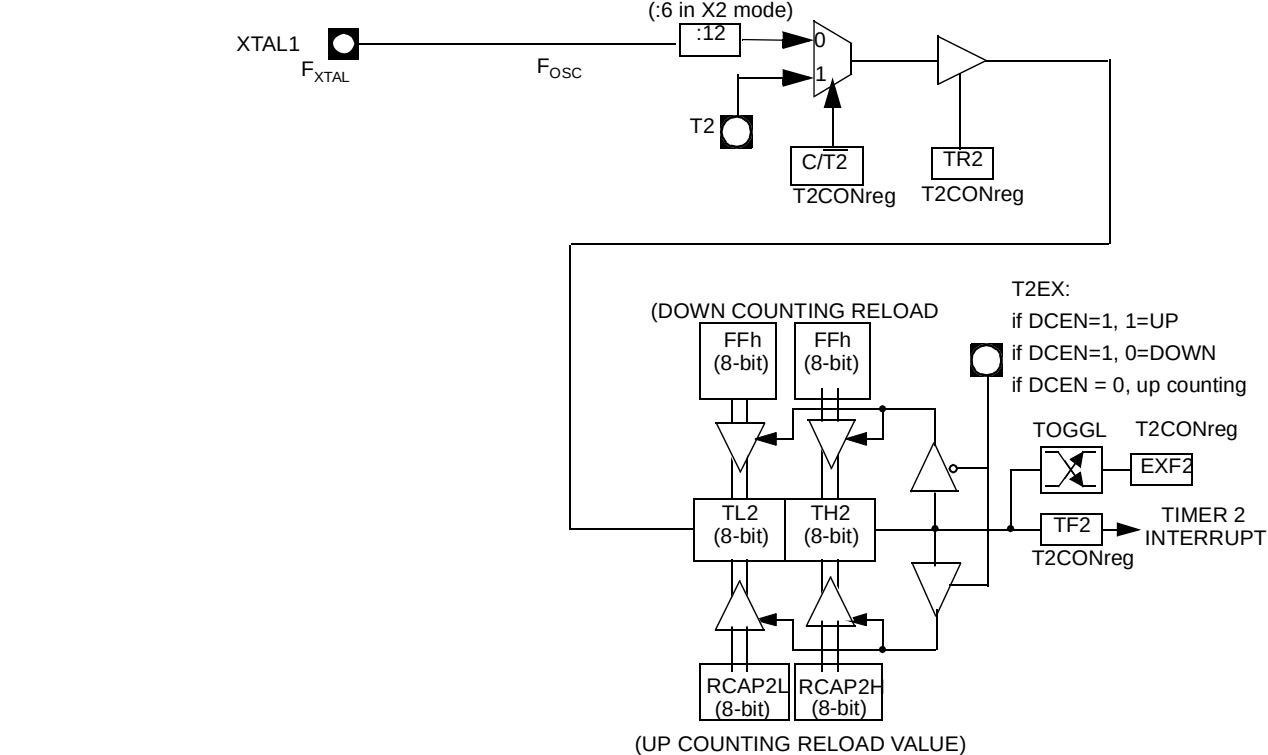
ASSEMBLY LANGUAGE

```

; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2  AUXR1 EQU 0A2H
;
0000 909000 MOV DPTR,#SOURCE ; address of SOURCE
0003 05A2 INC AUXR1 ; switch data pointers
0005 90A000 MOV DPTR,#DEST ; address of DEST
0008  LOOP:
0008 05A2 INC AUXR1 ; switch data pointers
000A E0 MOVX A,atDPTR ; get a byte from SOURCE
000B A3 INC DPTR ; increment SOURCE address
000C 05A2 INC AUXR1 ; switch data pointers
000E F0 MOVX atDPTR,A ; write the byte to DEST
000F A3 INC DPTR ; increment DEST address
0010 70F6 JNZ LOOP ; check for 0 terminator
0012 05A2 INC AUXR1 ; (optional) restore DPS

```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.



Programmable Clock-output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 5) . The input clock increments TL2 at frequency $F_{OSC}/2$. The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers :

$$Clock-OutFrequency = \frac{F_{osc}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz ($F_{OSC}/2^{16}$) to 4 MHz ($F_{OSC}/4$). The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear $C/\overline{T2}$ bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.
- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.

It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.

TS80C52X2 Serial I/O Port

The serial I/O port in the TS80C52X2 is compatible with the serial I/O port in the 80C52. It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

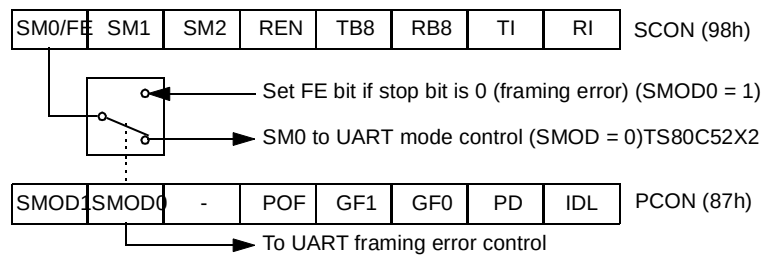
Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 6).

Figure 6. Framing Error Block Diagram



When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 9.) bit is set.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 7. and Figure 8.).

Figure 7. UART Timings in Mode 1

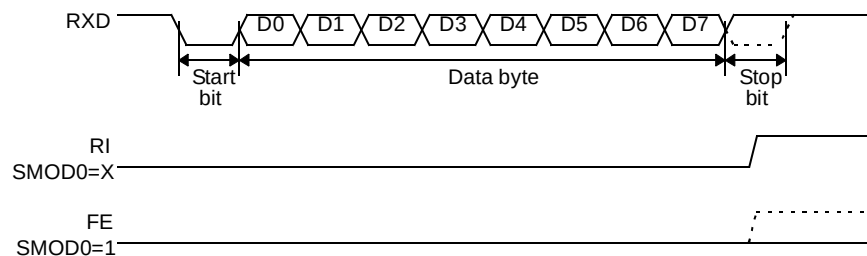


Table 10. PCON Register
PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
Bit Number	Bit Mnemonic	Description					
7	SMOD1	Serial port Mode bit 1 Set to select double baud rate in mode 1, 2 or 3.					
6	SMOD0	Serial port Mode bit 0 Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.					
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.					
4	POF	Power-off Flag Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.					
3	GF1	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.					
2	GF0	General purpose Flag Cleared by user for general purpose usage. Set by user for general purpose usage.					
1	PD	Power-down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.					
0	IDL	Idle mode bit Clear by hardware when interrupt or reset occurs. Set to enter idle mode.					

Reset Value = 00X1 0000b

Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

The TS80C52X2 has a total of 6 interrupt vectors: two external interrupts ($\overline{\text{INT0}}$ and $\overline{\text{INT1}}$), three timer interrupts (timers 0, 1 and 2) and the serial port interrupt. These interrupts are shown in Figure 9.

The diagram illustrates the Interrupt Control System. It shows the flow of interrupt signals from various sources (INT0, TF0, INT1, TF1, RI, TI, TF2, EXF2) through a central control unit (labeled IPH, IP) to a priority interrupt stack. The stack shows a polling sequence from high to low priority, with labels for 'High priority interrupt' and 'Low priority interrupt'.

Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 12.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 13.) and in the Interrupt Priority High register (See Table 14.). shows the bit values and priority levels associated with each combination.

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level

are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Table 12. IE Register
IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	-	ET2	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	Enable All interrupt bit Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	ET2	Timer 2 overflow interrupt Enable bit Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	Serial port Enable bit Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	Timer 1 overflow interrupt Enable bit Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	External interrupt 1 Enable bit Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	Timer 0 overflow interrupt Enable bit Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	External interrupt 0 Enable bit Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0X00 0000b

Bit addressable

Table 13. IP Register
IP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	-	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	PT2	Timer 2 overflow interrupt Priority bit Refer to PT2H for priority level.
4	PS	Serial port Priority bit Refer to PSH for priority level.
3	PT1	Timer 1 overflow interrupt Priority bit Refer to PT1H for priority level.
2	PX1	External interrupt 1 Priority bit Refer to PX1H for priority level.
1	PT0	Timer 0 overflow interrupt Priority bit Refer to PT0H for priority level.
0	PX0	External interrupt 0 Priority bit Refer to PX0H for priority level.

Reset Value = XX00 0000b
Bit addressable

Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does not affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

Note: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

Table 15. The State of Ports During Idle and Power-down Modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data ⁽¹⁾	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data ⁽¹⁾	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

Note: 1. Port 0 can force a "zero" level. A "one" will leave port floating.

Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 18. AUXR Register
AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	AO

Bit Number	Bit Mnemonic	Description
7	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
6	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
5	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
4	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
3	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
1	-	Reserved The value read from this bit is indeterminate. Do not set this bit.
0	AO	ALE Output bit Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = XXXX XXX0b
Not bit addressable

TS80C52X2

ROM Structure

The TS80C52X2 ROM memory is divided in three different arrays:

- the code array:8 Kbytes.
- the encryption array:64 bytes.
- the signature array:4 bytes.

ROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

Encryption Array

Within the ROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

Program Lock Bits

The lock bits when programmed according to Table 19. will provide different level of protection for the on-chip code and data.

Table 19. Program Lock bits

Program Lock Bits				Protection Description
Security level	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	P	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset.

U: unprogrammed

P: programmed

Signature bytes

The TS80C52X2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 9.

Verify Algorithm

Refer to Section "Verify Algorithm".

EPROM Structure

The TS87C52X2 is divided in two different arrays:

- the code array: 8 Kbytes
- the encryption array: 64 bytes

In addition a third non programmable array is implemented:

- the signature array: 4 bytes

EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

Program Lock Bits

The three lock bits, when programmed according to Table 1., will provide different level of protection for the on-chip code and data.

Program Lock Bits				Protection Description
Security level	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	P	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the EPROM is disabled.
3	U	P	U	Same as 2, also verify is disabled.
4	U	U	P	Same as 3, also external execution is disabled.

U: unprogrammed

P: programmed

WARNING: Security level 2 and 3 should only be programmed after EPROM and Core verification.

Signature Bytes

The TS80/87C52X2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 9.

EPROM Programming

Set-up modes

In order to program and verify the EPROM or to read the signature bytes, the TS87C52X2 is placed in specific set-up modes (See Figure 11.).

Control and program signals must be held at the levels indicated in Table 35.

Definition of terms

Address Lines: P1.0-P1.7, P2.0-P2.4 respectively for A0-A12

Data Lines: P0.0-P0.7 for D0-D7

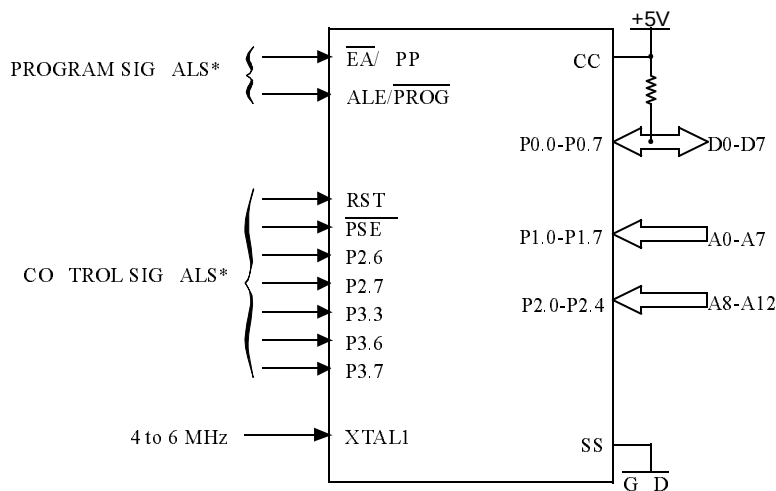
Control Signals: RST, $\overline{\text{PSEN}}$, P2.6, P2.7, P3.3, P3.6, P3.7.

Program Signals: ALE/ $\overline{\text{PROG}}$, $\overline{\text{EA}}$ /VPP.

Table 20. EPROM Set-up Modes

Mode	RST	PSEN	ALE/ PROG	$\overline{\text{EA}}$ / VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code data	1	0		12.75V	0	1	1	1	1
Verify Code data	1	0	1	1	0		0	1	1
Program Encryption Array Address 0-3Fh	1	0		12.75V	0	1	1	0	1
Read Signature Bytes	1	0	1	1	0		0	0	0
Program Lock bit 1	1	0		12.75V	1	1	1	1	1
Program Lock bit 2	1	0		12.75V	1	1	1	0	0
Program Lock bit 3	1	0		12.75V	1	0	1	1	0

Figure 11. Set-Up Modes Configuration



* See Table 31. for proper value on these inputs

Table 28., Table 31. and Table 34. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

Table 25. Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20	40	30	30	20
T (ns)	25	50	25	33.3	33.3	50

Example:

T_{LLIV} in X2 mode for a -V part at 20 MHz ($T = 1/20^{E6} = 50$ ns):

x= 22 (Table 28.)

T= 50ns

$T_{LLIV} = 2T - x = 2 \times 50 - 22 = 78$ ns

External Program Memory Characteristics

Table 26. Symbol Description

Symbol	Parameter
T	Oscillator clock period
T_{LHLL}	ALE pulse width
T_{AVLL}	Address Valid to ALE
T_{LLAX}	Address Hold After ALE
T_{LLIV}	ALE to Valid Instruction In
T_{LLPL}	ALE to $\overline{PSEN}$
T_{PLPH}	$\overline{PSEN}$ Pulse Width
T_{PLIV}	$\overline{PSEN}$ to Valid Instruction In
T_{PXIX}	Input Instruction Hold After $\overline{PSEN}$
T_{PXIZ}	Input Instruction FloatAfter $\overline{PSEN}$
T_{PXAV}	$\overline{PSEN}$ to Address Valid
T_{AVIV}	Address to Valid Instruction In
T_{PLAZ}	$\overline{PSEN}$ Low to Address Float

Table 27. AC Parameters for Fix Clock

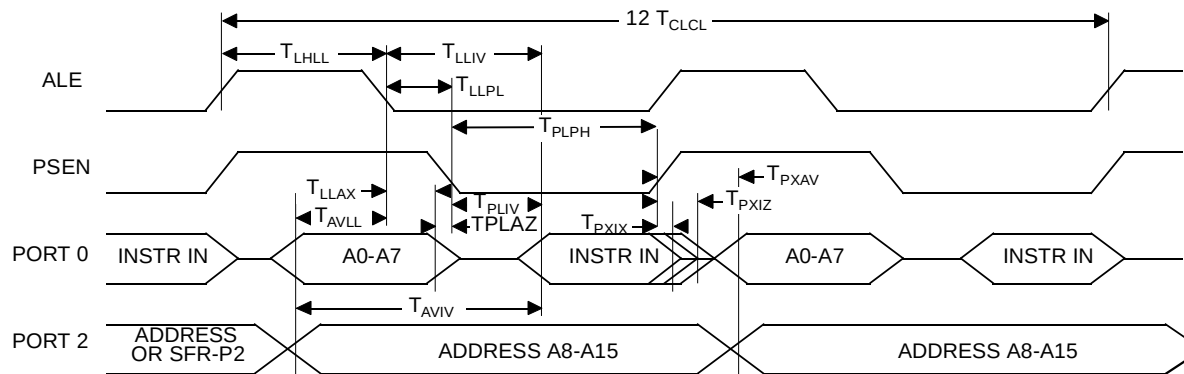
Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T	25		33		25		50		33		ns
T _{LHLL}	40		25		42		35		52		ns
T _{AVLL}	10		4		12		5		13		ns
T _{LLAX}	10		4		12		5		13		ns
T _{LLIV}		70		45		78		65		98	ns
T _{LLPL}	15		9		17		10		18		ns
T _{PLPH}	55		35		60		50		75		ns
T _{PLIV}		35		25		50		30		55	ns
T _{PXIX}	0		0		0		0		0		ns
T _{PXIZ}		18		12		20		10		18	ns
T _{AVIV}		85		53		95		80		122	ns
T _{PLAZ}		10		10		10		10		10	ns

Table 28. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T _{LHLL}	Min	2 T - x	T - x	10	8	15	ns
T _{AVLL}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLAX}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLIV}	Max	4 T - x	2 T - x	30	22	35	ns
T _{LLPL}	Min	T - x	0.5 T - x	10	8	15	ns
T _{PLPH}	Min	3 T - x	1.5 T - x	20	15	25	ns
T _{PLIV}	Max	3 T - x	1.5 T - x	40	25	45	ns
T _{PXIX}	Min	x	x	0	0	0	ns
T _{PXIZ}	Max	T - x	0.5 T - x	7	5	15	ns
T _{AVIV}	Max	5 T - x	2.5 T - x	40	30	45	ns
T _{PLAZ}	Max	x	x	10	10	10	ns

External Program Memory Read Cycle

Figure 18. External Program Memory Read Cycle



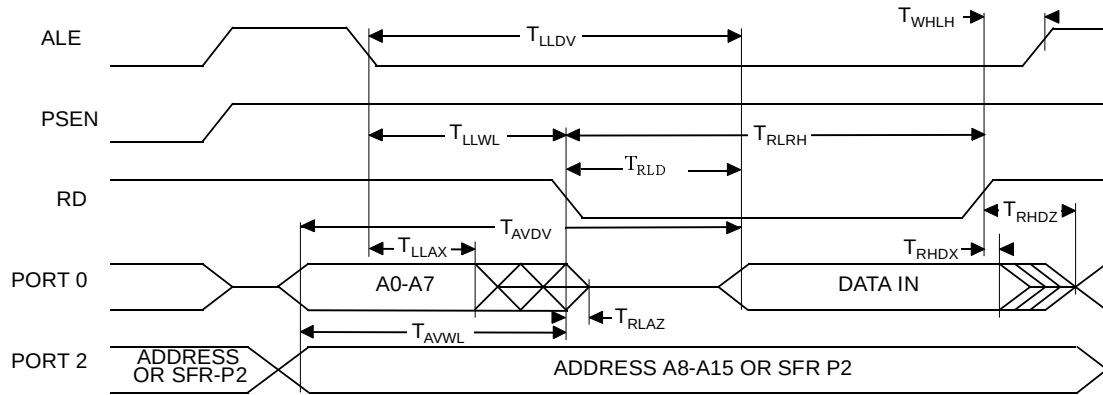
External Data Memory Characteristics

Table 29. Symbol Description

Symbol	Parameter
T_{RLRH}	$\overline{RD}$ Pulse Width
T_{WLWH}	$\overline{WR}$ Pulse Width
T_{RLDV}	$\overline{RD}$ to Valid Data In
T_{RHDZ}	Data Hold After $\overline{RD}$
T_{RHDZ}	Data Float After $\overline{RD}$
T_{LLDV}	ALE to Valid Data In
T_{AVDV}	Address to Valid Data In
T_{LLWL}	ALE to $\overline{WR}$ or $\overline{RD}$
T_{AVWL}	Address to $\overline{WR}$ or $\overline{RD}$
T_{QVWX}	Data Valid to $\overline{WR}$ Transition
T_{QVWH}	Data set-up to $\overline{WR}$ High
T_{WHQX}	Data Hold After $\overline{WR}$
T_{RLAZ}	$\overline{RD}$ Low to Address Float
T_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE high

External Data Memory Read Cycle

Figure 20. External Data Memory Read Cycle



Serial Port Timing - Shift Register Mode

Table 32. Symbol Description

Symbol	Parameter
T_{XLXL}	Serial port clock cycle time
T_{QVHX}	Output data set-up to clock rising edge
T_{XHGX}	Output data hold after clock rising edge
T_{XHDX}	Input data hold after clock rising edge
T_{XHDV}	Clock rising edge to input data valid

Table 33. AC Parameters for a Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T_{XLXL}	300		200		300		300		400		ns
T_{QVHX}	200		117		200		200		283		ns
T_{XHGX}	30		13		30		30		47		ns
T_{XHDX}	0		0		0		0		0		ns
T_{XHDV}		117		34		117		117		200	ns

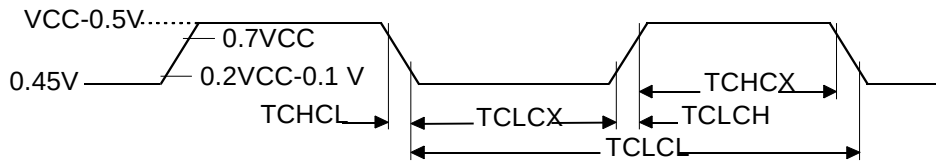
External Clock Drive Characteristics (XTAL1)

Table 36. AC Parameters

Symbol	Parameter	Min	Max	Units
T_{CLCL}	Oscillator Period	25		ns
T_{CHCX}	High Time	5		ns
T_{CLCX}	Low Time	5		ns
T_{CLCH}	Rise Time		5	ns
T_{CHCL}	Fall Time		5	ns
T_{CHCX}/T_{CLCX}	Cyclic ratio in X2 mode	40	60	%

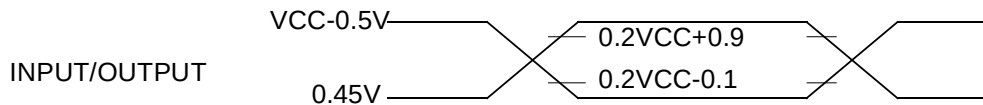
External Clock Drive Waveforms

Figure 23. External Clock Drive Waveforms



AC Testing Input/Output Waveforms

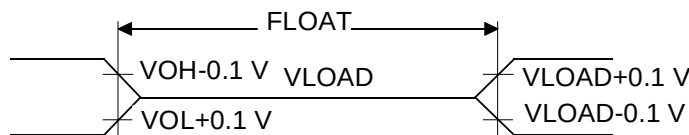
Figure 24. AC Testing Input/Output Waveforms



AC inputs during testing are driven at $V_{CC} - 0.5$ for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at V_{IH} min for a logic “1” and V_{IL} max for a logic “0”.

Float Waveforms

Figure 25. Float Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20mA$.

Ordering Information

Table 37. Possible Ordering Entries

Part Number ⁽³⁾	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS80C32X2-MCA	ROMLess	5V $\pm$ 10%	Commercial	40 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-MCB	ROMLess	5V $\pm$ 10%	Commercial	40 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-MCC	ROMLess	5V $\pm$ 10%	Commercial	40 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-MCE	ROMLess	5V $\pm$ 10%	Commercial	40 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-LCA	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-LCB	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-LCC	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-LCE	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-VCA	ROMLess	5V $\pm$ 10%	Commercial	60 MHz ⁽³⁾	PDIL40	Stick
TS80C32X2-VCB	ROMLess	5V $\pm$ 10%	Commercial	60 MHz ⁽³⁾	PLCC44	Stick
TS80C32X2-VCC	ROMLess	5V $\pm$ 10%	Commercial	60 MHz ⁽³⁾	PQFP44	Tray
TS80C32X2-VCE	ROMLess	5V $\pm$ 10%	Commercial	60 MHz ⁽³⁾	VQFP44	Tray
TS80C32X2-MIA	ROMLess	5V $\pm$ 10%	Industrial	40 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-MIB	ROMLess	5V $\pm$ 10%	Industrial	40 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-MIC	ROMLess	5V $\pm$ 10%	Industrial	40 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-MIE	ROMLess	5V $\pm$ 10%	Industrial	40 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-LIA	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-LIB	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-LIC	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-LIE	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-VIA	ROMLess	5V $\pm$ 10%	Industrial	60 MHz ⁽³⁾	PDIL40	Stick
TS80C32X2-VIB	ROMLess	5V $\pm$ 10%	Industrial	60 MHz ⁽³⁾	PLCC44	Stick
TS80C32X2-VIC	ROMLess	5V $\pm$ 10%	Industrial	60 MHz ⁽³⁾	PQFP44	Tray
TS80C32X2-VIE	ROMLess	5V $\pm$ 10%	Industrial	60 MHz ⁽³⁾	VQFP44	Tray
AT80C32X2-3CSUM	ROMLess	5V $\pm$ 10%	Industrial & Green	40 MHz ⁽¹⁾	PDIL40	Stick
AT80C32X2-SLSUM	ROMLess	5V $\pm$ 10%	Industrial & Green	40 MHz ⁽¹⁾	PLCC44	Stick
AT80C32X2-RLTUM	ROMLess	5V $\pm$ 10%	Industrial & Green	40 MHz ⁽¹⁾	VQFP44	Tray
AT80C32X2-RLTUM	ROMLess	5V $\pm$ 10%	Industrial & Green	40 MHz ⁽¹⁾	VQFP44	Tape & Reel
AT80C32X2-3CSUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PDIL40	Stick
AT80C32X2-SLSUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PLCC44	Stick