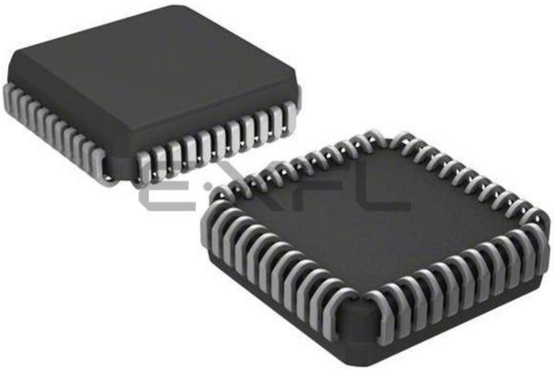

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 80C51 |
| Core Size | 8-Bit |
| Speed | 30/20MHz |
| Connectivity | UART/USART |
| Peripherals | POR |
| Number of I/O | 32 |
| Program Memory Size | - |
| Program Memory Type | ROMless |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-LCC (J-Lead) |
| Supplier Device Package | 44-PLCC (16.6x16.6) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/at80c32x2-slrul |

| Mnemonic | Pin Number | | | Type | Name and Function |
|---|---|---|---|---|---|
| | DIL | LCC | VQFP 1.4 | | |
| $V_{SS}$ | 20 | 22 | 16 | I | **Ground:** 0V reference |
| Vss1 | | 1 | 39 | I | Optional Ground: **Contact the Sales Office for ground connection.** |
| $V_{CC}$ | 40 | 44 | 38 | I | **Power Supply:** This is the power supply voltage for normal, idle and power-down operation |
| P0.0-P0.7 | 39-32 | 43-36 | 37-30 | I/O | **Port 0**: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs.Port 0 pins must be polarized to Vcc or Vss in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes. |
| P1.0-P1.7 | 1-8 | 2-9 | 40-44<br>1-3 | I/O | Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification.<br>Alternate functions for Port 1 include: |
| | 1 | 2 | 40 | I/O | **T2 (P1.0):** Timer/Counter 2 external count input/Clockout |
| | 2 | 3 | 41 | I | **T2EX (P1.1):** Timer/Counter 2 Reload/Capture/Direction Control |
| P2.0-P2.7 | 21-28 | 24-31 | 18-25 | I/O | **Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX atDPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX atRi), port 2 emits the contents of the P2 SFR. Some Port 2 pins receive the high order address bits during EPROM programming and verification: P2.0 to P2.4 |
| P3.0-P3.7 | 10-17 | 11,<br>13-19 | 5,<br>7-13 | I/O | Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below. |
| | 10 | 11 | 5 | I | **RXD (P3.0):** Serial input port |
| | 11 | 13 | 7 | O | **TXD (P3.1):** Serial output port |
| | 12 | 14 | 8 | I | **$\overline{\text{INT0}}$ (P3.2):** External interrupt 0 |

| Mnemonic | Pin Number | | | Type | Name and Function |
|---|---|---|---|---|---|
| | DIL | LCC | VQFP 1.4 | | |
| | 13 | 15 | 9 | I | **$\overline{\text{INT1}}$ (P3.3):** External interrupt 1 |
| | 14 | 16 | 10 | I | **T0 (P3.4):** Timer 0 external input |
| | 15 | 17 | 11 | I | **T1 (P3.5):** Timer 1 external input |
| | 16 | 18 | 12 | O | **$\overline{\text{WR}}$ (P3.6):** External data memory write strobe |
| | 17 | 19 | 13 | O | **$\overline{\text{RD}}$ (P3.7):** External data memory read strobe |
| Reset | 9 | 10 | 4 | I | **Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to $V_{SS}$ permits a power-on reset using only an external capacitor to $V_{CC.}$ |
| ALE/$\overline{\text{PROG}}$ | 30 | 33 | 27 | O (I) | **Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during EPROM programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches. |
| PSEN | 29 | 32 | 26 | O | **Program Store ENable:** The read strobe to external program memory. When executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory. |
| $\overline{\text{EA}}$/$V_{PP}$ | 31 | 35 | 29 | I | **External Access Enable/Programming Supply Voltage:** $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH (RB) or 7FFFH (RC), or FFFFH (RD). If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (RB) or 7FFFH (RC) $\overline{\text{EA}}$ must be held low for ROMless devices. This pin also receives the 12.75V programming supply voltage ($V_{PP}$) during EPROM programming. If security level 1 is programmed, $\overline{\text{EA}}$ will be internally latched on Reset. |
| XTAL1 | 19 | 21 | 15 | I | **Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits. |
| XTAL2 | 18 | 20 | 14 | O | **Crystal 2:** Output from the inverting oscillator amplifier |

## Dual Data Pointer Register (Ddptr)

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called
DPS = AUXR1/bit0 (See Table 5.) that allows the program code to switch between them (Refer to Figure 3).

**Figure 3.** Use of Dual Pointer

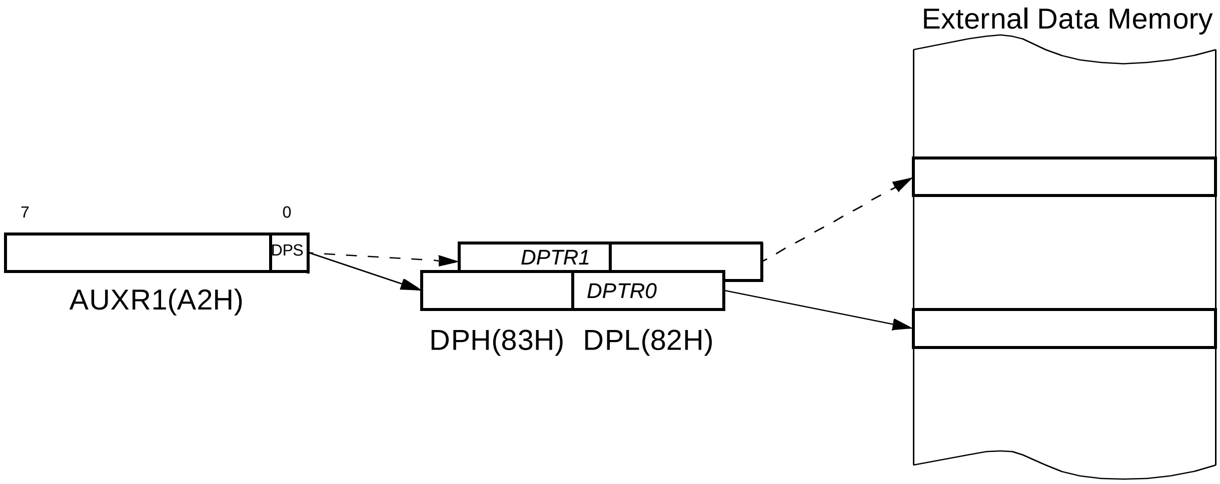


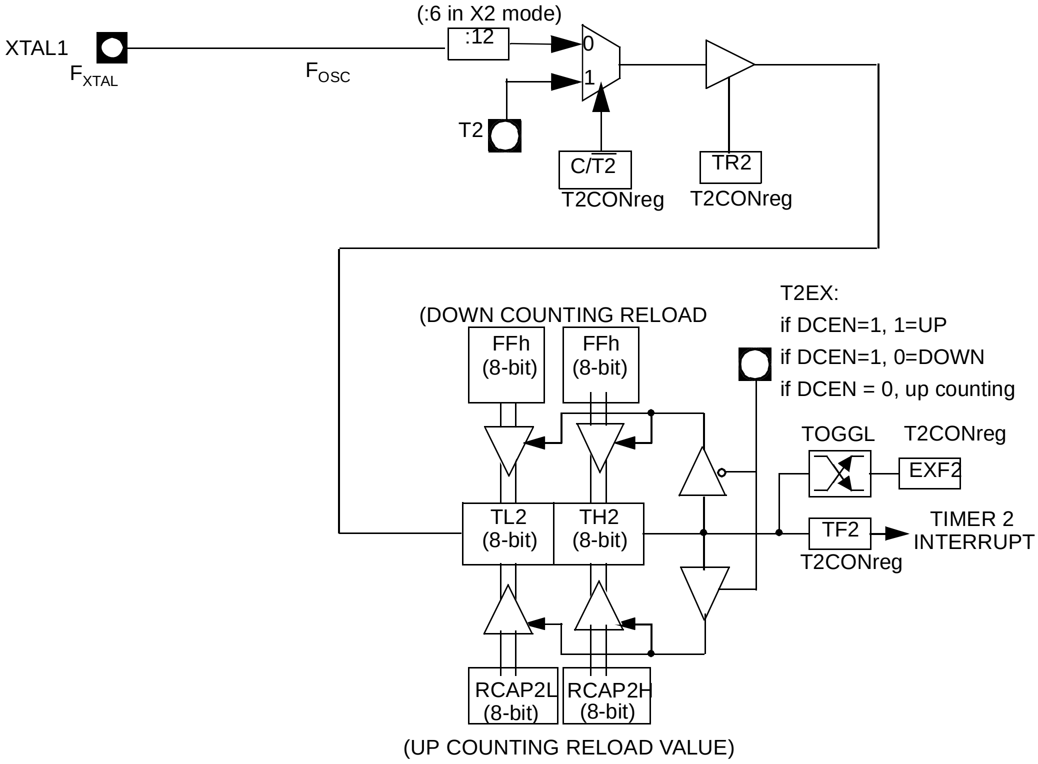
**Table 4.** AUXR1: Auxiliary Register 1

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **-** | **-** | **-** | **-** | **GF3** | **0** | **-** | **DPS** |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 4 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 3 | GF3 | This bit is a general purpose user flag |
| 2 | 0 | **Reserved**<br>Always stuck at 0 |
| 1 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 0 | DPS | **Data Pointer Selection**<br>Clear to select DPTR0.<br>Set to select DPTR1. |

Reset Value = XXXX XXX0
Not bit addressable

**Figure 4.** Auto-reload Mode Up/Down Counter (DCEN = 1)



## Programmable Clock-output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 5) . The input clock increments TL2 at frequency $F_{OSC}/2$. The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers :

$$Clock - OutFrequency = \frac{F_{osc}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz ($F_{OSC}/2^{16)}$ to 4 MHz ($F_{OSC}/4$). The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear C/$\overline{T2}$ bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.
- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.

It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.

**Table 5.** T2CON Register

T2CON - Timer 2 Control Register (C8h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| **TF2** | **EXF2** | **RCLK** | **TCLK** | **EXEN2** | **TR2** | **C/T2#** | **CP/RL2#** |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | TF2 | **Timer 2 overflow Flag**<br>Must be cleared by software.<br>Set by hardware on timer 2 overflow, if RCLK = 0 and TCLK = 0. |
| 6 | EXF2 | **Timer 2 External Flag**<br>Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1.<br>When set, causes the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled.<br>Must be cleared by software. EXF2 doesn’t cause an interrupt in Up/down counter mode (DCEN = 1) |
| 5 | RCLK | **Receive Clock bit**<br>Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3.<br>Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3. |
| 4 | TCLK | **Transmit Clock bit**<br>Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3.<br>Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3. |
| 3 | EXEN2 | **Timer 2 External Enable bit**<br>Clear to ignore events on T2EX pin for timer 2 operation.<br>Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port. |
| 2 | TR2 | **Timer 2 Run control bit**<br>Clear to turn off timer 2.<br>Set to turn on timer 2. |
| 1 | C/T2# | **Timer/Counter 2 select bit**<br>Clear for timer operation (input from internal clock system: $F_{OSC}$).<br>Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode. |
| 0 | CP/RL2# | **Timer 2 Capture/Reload bit**<br>If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to Auto-reload on timer 2 overflow.<br>Clear to Auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1.<br>Set to capture on negative transitions on T2EX pin if EXEN2=1. |

Reset Value = 0000 0000b

Bit addressable

Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

Note: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

**Table 15.** The State of Ports During Idle and Power-down Modes

| Mode | Program Memory | ALE | PSEN | PORT0 | PORT1 | PORT2 | PORT3 |
|---|---|---|---|---|---|---|---|
| Idle | Internal | 1 | 1 | Port Data[1] | Port Data | Port Data | Port Data |
| Idle | External | 1 | 1 | Floating | Port Data | Address | Port Data |
| Power Down | Internal | 0 | 0 | Port Data[1] | Port Data | Port Data | Port Data |
| Power Down | External | 0 | 0 | Floating | Port Data | Port Data | Port Data |

Note: 1. Port 0 can force a "zero" level. A "one" will leave port floating.

## EPROM Structure

The TS87C52X2 is divided in two different arrays:

- the code array: 8 Kbytes
- the encryption array: 64 bytes

In addition a third non programmable array is implemented:

- the signature array: 4 bytes

## EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

### Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

### Program Lock Bits

The three lock bits, when programmed according to Table 1., will provide different level of protection for the on-chip code and data.

| Program Lock Bits | | | | |
|---|---|---|---|---|
| **Security level** | **LB1** | **LB2** | **LB3** | **Protection Description** |
| 1 | U | U | U | No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data. |
| 2 | P | U | U | MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the EPROM is disabled. |
| 3 | U | P | U | Same as 2, also verify is disabled. |
| 4 | U | U | P | Same as 3, also external execution is disabled. |

U: unprogrammed
P: programmed

WARNING: Security level 2 and 3 should only be programmed after EPROM and Core verification.

### Signature Bytes

The TS80/87C52X2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 9.

## EPROM Programming

### Set-up modes

In order to program and verify the EPROM or to read the signature bytes, the TS87C52X2 is placed in specific set-up modes (See Figure 11.).

Control and program signals must be held at the levels indicated in Table 35.

### Definition of terms

**Address Lines:** P1.0-P1.7, P2.0-P2.4 respectively for A0-A12

**Data Lines:** P0.0-P0.7 for D0-D7

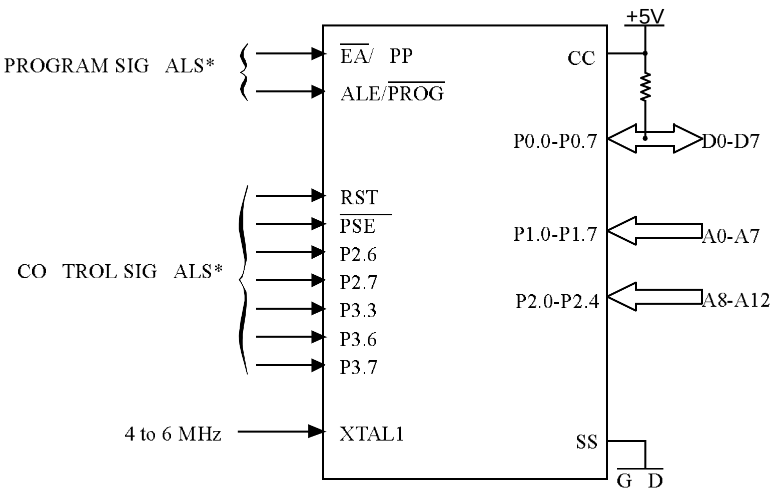
**Control Signals:** RST, $\overline{\text{PSEN}}$, P2.6, P2.7, P3.3, P3.6, P3.7.

**Program Signals:** ALE/$\overline{\text{PROG}}$, $\overline{\text{EA}}$/VPP.

**Table 20.** EPROM Set-up Modes

| Mode | RST | PSEN | ALE/ $\overline{\text{PROG}}$ | $\overline{\text{EA}}$/ VPP | P2.6 | P2.7 | P3.3 | P3.6 | P3.7 |
|---|---|---|---|---|---|---|---|---|---|
| Program Code data | 1 | 0 | ⊔ | 12.75V | 0 | 1 | 1 | 1 | 1 |
| Verify Code data | 1 | 0 | 1 | 1 | 0 | ⊔ | 0 | 1 | 1 |
| Program Encryption Array Address 0-3Fh | 1 | 0 | ⊔ | 12.75V | 0 | 1 | 1 | 0 | 1 |
| Read Signature Bytes | 1 | 0 | 1 | 1 | 0 | ⊔ | 0 | 0 | 0 |
| Program Lock bit 1 | 1 | 0 | ⊔ | 12.75V | 1 | 1 | 1 | 1 | 1 |
| Program Lock bit 2 | 1 | 0 | ⊔ | 12.75V | 1 | 1 | 1 | 0 | 0 |
| Program Lock bit 3 | 1 | 0 | ⊔ | 12.75V | 1 | 0 | 1 | 1 | 0 |

**Figure 11.** Set-Up Modes Configuration



* See Table 31. for proper value on these inputs

12,000 µW/cm$^2$ rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

## Signature Bytes

The TS80/87C52X2 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 31. for Read Signature Bytes. Table 35. shows the content of the signature byte for the TS80/87C52X2.

**Table 21.** Signature Bytes Content

| Location | Contents | Comment |
|---|---|---|
| 30h | 58h | Manufacturer Code: Atmel |
| 31h | 57h | Family Code: C51 X2 |
| 60h | 2Dh | Product name: TS80C52X2 |
| 60h | ADh | Product name:TS87C52X2 |
| 60h | 20h | Product name: TS80C32X2 |
| 61h | FFh | Product revision number |

# Electrical Characteristics

## Absolute Maximum Ratings[1]

Ambiant Temperature Under Bias:
C = commercial......................................................0°C to 70°C
I = industrial .........................................................-40°C to 85°C
Storage Temperature .................................... -65°C to + 150°C
Voltage on $V_{CC}$ to $V_{SS}$ .........................................-0.5V to + 7 V
Voltage on $V_{PP}$ to $V_{SS}$ .......................................-0.5V to + 13 V
Voltage on Any Pin to $V_{SS}$..........................-0.5V to $V_{CC}$ + 0.5V
Power Dissipation ............................................................ 1 W[2]

Notes:

1. Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

## Power Consumption Measurement

Since the introduction of the first C51 devices, every manufacturer made operating Icc measurements under reset, which made sense for the designs were the CPU was running under reset. In Atmel new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That's why, while keeping measurements under Reset, Atmel presents a new way to measure the operating Icc:

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = Vcc, RST = Vss, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating Icc.

## DC Parameters for Standard Voltage

TA = 0°C to +70°C; $V_{SS}$ = 0 V; $V_{CC}$ = 5V ± 10%; F = 0 to 40 MHz.
TA = -40°C to +85°C; $V_{SS}$ = 0 V; $V_{CC}$ = 5V ± 10%; F = 0 to 40 MHz.

**Table 22.** DC Parameters in Standard Voltage

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.5 | | 0.2 $V_{CC}$ - 0.1 | V | |
| $V_{IH}$ | Input High Voltage except XTAL1, RST | 0.2 $V_{CC}$ + 0.9 | | $V_{CC}$ + 0.5 | V | |
| $V_{IH1}$ | Input High Voltage, XTAL1, RST | 0.7 $V_{CC}$ | | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage, ports 1, 2, 3 (6) | | | 0.3<br>0.45<br>1.0 | V<br>V<br>V | $I_{OL}$ = 100 µA[4]<br>$I_{OL}$ = 1.6 mA[4]<br>$I_{OL}$ = 3.5 mA[4] |
| $V_{OL1}$ | Output Low Voltage, port 0 (6) | | | 0.3<br>0.45<br>1.0 | V<br>V<br>V | $I_{OL}$ = 200 µA[4]<br>$I_{OL}$ = 3.2 mA[4]<br>$I_{OL}$ = 7.0 mA[4] |
| $V_{OL2}$ | Output Low Voltage, ALE, $\overline{PSEN}$ | | | 0.3<br>0.45<br>1.0 | V<br>V<br>V | $I_{OL}$ = 100 µA[4]<br>$I_{OL}$ = 1.6 mA[4]<br>$I_{OL}$ = 3.5 mA[4] |

## DC Parameters for Low Voltage

$T_A = 0°C$ to $+70°C$; $V_{SS} = 0$ V; $V_{CC} = 2.7$ V to 5.5V ; F = 0 to 30 MHz.
$T_A = -40°C$ to $+85°C$; $V_{SS} = 0$ V; $V_{CC} = 2.7$ V to 5.5V ; F = 0 to 30 MHz.

**Table 23.** DC Parameters for Low Voltage

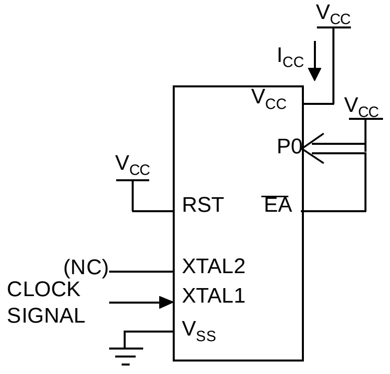
| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | -0.5 | | 0.2 $V_{CC}$ - 0.1 | V | |
| $V_{IH}$ | Input High Voltage except XTAL1, RST | 0.2 $V_{CC}$ + 0.9 | | $V_{CC}$ + 0.5 | V | |
| $V_{IH1}$ | Input High Voltage, XTAL1, RST | 0.7 $V_{CC}$ | | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output Low Voltage, ports 1, 2, 3 $^{(6)}$ | | | 0.45 | V | $I_{OL} = 0.8$ mA$^{(4)}$ |
| $V_{OL1}$ | Output Low Voltage, port 0, ALE, $\overline{\text{PSEN}}$ $^{(6)}$ | | | 0.45 | V | $I_{OL} = 1.6$ mA$^{(4)}$ |
| $V_{OH}$ | Output High Voltage, ports 1, 2, 3 | 0.9 $V_{CC}$ | | | V | $I_{OH} = -10$ µA |
| $V_{OH1}$ | Output High Voltage, port 0, ALE, $\overline{\text{PSEN}}$ | 0.9 $V_{CC}$ | | | V | $I_{OH} = -40$ µA |
| $I_{IL}$ | Logical 0 Input Current ports 1, 2 and 3 | | | -50 | µA | Vin = 0.45V |
| $I_{LI}$ | Input Leakage Current | | | ±10 | µA | 0.45V < Vin < $V_{CC}$ |
| $I_{TL}$ | Logical 1 to 0 Transition Current, ports 1, 2, 3 | | | -650 | µA | Vin = 2.0 V |
| $R_{RST}$ | RST Pulldown Resistor | 50 | 90 $^{(5)}$ | 200 | kΩ | |
| CIO | Capacitance of I/O Buffer | | | 10 | pF | Fc = 1 MHz<br>$T_A = 25°C$ |
| $I_{PD}$ | Power Down Current | | 20 $^{(5)}$<br>10 $^{(5)}$ | 50<br>30 | µA | $V_{CC} = 2.0$ V to 5.5V$^{(3)}$<br>$V_{CC} = 2.0$ V to 3.3 V$^{(3)}$ |
| $I_{CC}$<br>under<br>RESET | Power Supply Current Maximum values, X1 mode: $^{(7)}$ | | | 1 + 0.2 Freq (MHz)<br>at12MHz 3.4<br>at16MHz 4.2 | mA | $V_{CC} = 3.3$ V$^{(1)}$ |
| $I_{CC}$<br>operating | Power Supply Current Maximum values, X1 mode: $^{(7)}$ | | | 1 + 0.3 Freq (MHz)<br>at12MHz 4.6<br>at16MHz 5.8 | mA | $V_{CC} = 3.3$ V$^{(8)}$ |
| $I_{CC}$<br>idle | Power Supply Current Maximum values, X1 mode: $^{(7)}$ | | | 0.15 Freq (MHz) + 0.2<br>at12MHz 2<br>at16MHz 2.6 | mA | $V_{CC} = 3.3$ V$^{(2)}$ |

Notes:
1. $I_{CC}$ under reset is measured with all output pins disconnected; XTAL1 driven with $T_{CLCH}$, $T_{CHCL} = 5$ ns (see Figure 17.), $V_{IL} = V_{SS} + 0.5V$,
   $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; $\overline{\text{EA}}$ = RST = Port 0 = $V_{CC}$. $I_{CC}$ would be slightly higher if a crystal oscillator used..
2. Idle $I_{CC}$ is measured with all output pins disconnected; XTAL1 driven with $T_{CLCH}$, $T_{CHCL} = 5$ ns, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C; Port 0 = $V_{CC}$; $\overline{\text{EA}}$ = RST = $V_{SS}$ (see Figure 15.).
3. Power Down $I_{CC}$ is measured with all output pins disconnected; $\overline{\text{EA}} = V_{SS}$, PORT 0 = $V_{CC}$; XTAL2 NC.; RST = $V_{SS}$ (see Figure 16.).
4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the $V_{OL}$s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi $V_{OL}$ peak 0.6V. A Schmitt Trigger use is not necessary.
5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
6. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:
   Maximum $I_{OL}$ per port pin: 10 mA
   Maximum $I_{OL}$ per 8-bit port:

Port 0: 26 mA
Ports 1, 2 and 3: 15 mA
Maximum total $I_{OL}$ for all output pins: 71 mA
If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

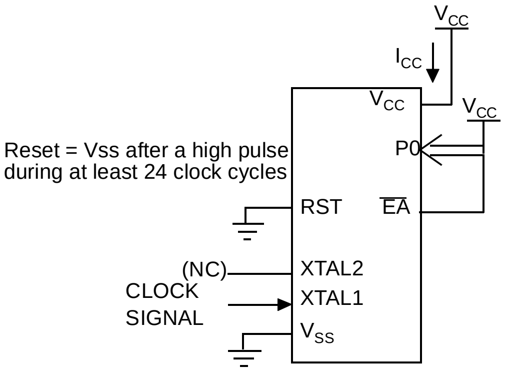
7. For other values, please contact your sales office.
8. Operating $I_{CC}$ is measured with all output pins disconnected; XTAL1 driven with $T_{CLCH}$, $T_{CHCL}$ = 5 ns (see Figure 17.), $V_{IL} = V_{SS} + 0.5V$,
   $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; $\overline{EA}$ = Port 0 = $V_{CC}$; RST = $V_{SS}$. The internal ROM runs the code 80 FE (label: SJMP label). $I_{CC}$ would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.

**Figure 13.** $I_{CC}$ Test Condition, under reset



All other pins are disconnected.

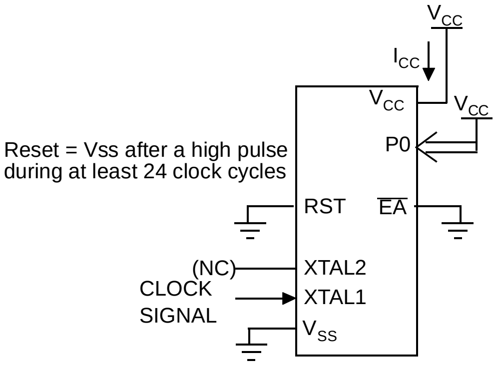
**Figure 14.** Operating $I_{CC}$ Test Condition



Reset = Vss after a high pulse during at least 24 clock cycles

All other pins are disconnected.

**Figure 15.** $I_{CC}$ Test Condition, Idle Mode



Reset = Vss after a high pulse during at least 24 clock cycles

All other pins are disconnected.

**Table 27.** AC Parameters for Fix Clock

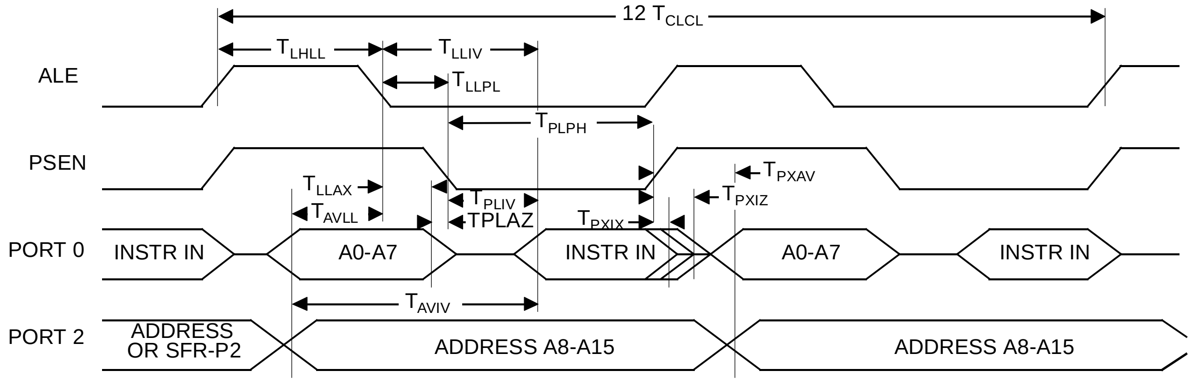
| Speed | -M<br>40 MHz | | -V<br>X2 mode<br>30 MHz<br>60 MHz equiv. | | -V<br>standard mode 40 MHz | | -L<br>X2 mode<br>20 MHz<br>40 MHz equiv. | | -L<br>standard mode<br>30 MHz | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| T | 25 | | 33 | | 25 | | 50 | | 33 | | ns |
| $T_{LHLL}$ | 40 | | 25 | | 42 | | 35 | | 52 | | ns |
| $T_{AVLL}$ | 10 | | 4 | | 12 | | 5 | | 13 | | ns |
| $T_{LLAX}$ | 10 | | 4 | | 12 | | 5 | | 13 | | ns |
| $T_{LLIV}$ | | 70 | | 45 | | 78 | | 65 | | 98 | ns |
| $T_{LLPL}$ | 15 | | 9 | | 17 | | 10 | | 18 | | ns |
| $T_{PLPH}$ | 55 | | 35 | | 60 | | 50 | | 75 | | ns |
| $T_{PLIV}$ | | 35 | | 25 | | 50 | | 30 | | 55 | ns |
| $T_{PXIX}$ | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $T_{PXIZ}$ | | 18 | | 12 | | 20 | | 10 | | 18 | ns |
| $T_{AVIV}$ | | 85 | | 53 | | 95 | | 80 | | 122 | ns |
| $T_{PLAZ}$ | | 10 | | 10 | | 10 | | 10 | | 10 | ns |

**Table 28.** AC Parameters for a Variable Clock: derating formula

| Symbol | Type | Standard Clock | X2 Clock | -M | -V | -L | Units |
|---|---|---|---|---|---|---|---|
| $T_{LHLL}$ | Min | 2 T - x | T - x | 10 | 8 | 15 | ns |
| $T_{AVLL}$ | Min | T - x | 0.5 T - x | 15 | 13 | 20 | ns |
| $T_{LLAX}$ | Min | T - x | 0.5 T - x | 15 | 13 | 20 | ns |
| $T_{LLIV}$ | Max | 4 T - x | 2 T - x | 30 | 22 | 35 | ns |
| $T_{LLPL}$ | Min | T - x | 0.5 T - x | 10 | 8 | 15 | ns |
| $T_{PLPH}$ | Min | 3 T - x | 1.5 T - x | 20 | 15 | 25 | ns |
| $T_{PLIV}$ | Max | 3 T - x | 1.5 T - x | 40 | 25 | 45 | ns |
| $T_{PXIX}$ | Min | x | x | 0 | 0 | 0 | ns |
| $T_{PXIZ}$ | Max | T - x | 0.5 T - x | 7 | 5 | 15 | ns |
| $T_{AVIV}$ | Max | 5 T - x | 2.5 T - x | 40 | 30 | 45 | ns |
| $T_{PLAZ}$ | Max | x | x | 10 | 10 | 10 | ns |

## External Program Memory Read Cycle

**Figure 18.** External Program Memory Read Cycle



## External Data Memory Characteristics

**Table 29.** Symbol Description

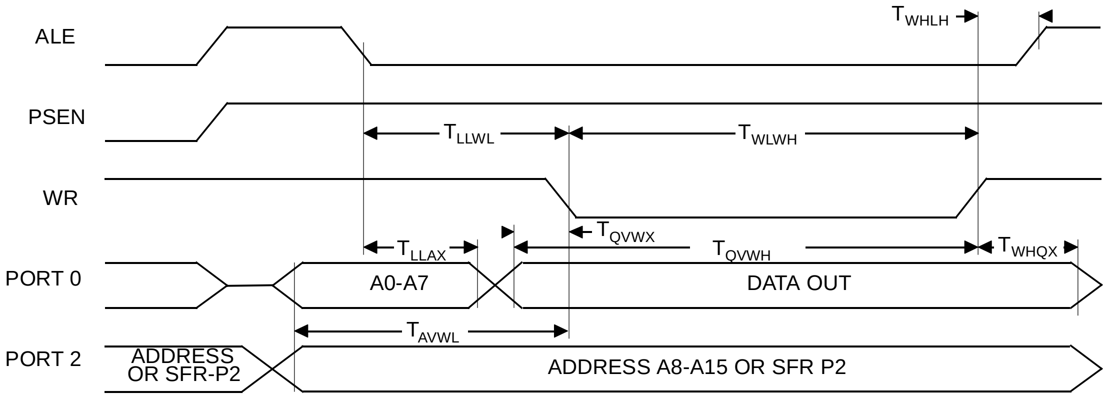
| Symbol | Parameter |
|---|---|
| $T_{RLRH}$ | $\overline{\text{RD}}$ Pulse Width |
| $T_{WLWH}$ | $\overline{\text{WR}}$ Pulse Width |
| $T_{RLDV}$ | $\overline{\text{RD}}$ to Valid Data In |
| $T_{RHDX}$ | Data Hold After $\overline{\text{RD}}$ |
| $T_{RHDZ}$ | Data Float After $\overline{\text{RD}}$ |
| $T_{LLDV}$ | ALE to Valid Data In |
| $T_{AVDV}$ | Address to Valid Data In |
| $T_{LLWL}$ | ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$ |
| $T_{AVWL}$ | Address to $\overline{\text{WR}}$ or $\overline{\text{RD}}$ |
| $T_{QVWX}$ | Data Valid to $\overline{\text{WR}}$ Transition |
| $T_{QVWH}$ | Data set-up to $\overline{\text{WR}}$ High |
| $T_{WHQX}$ | Data Hold After $\overline{\text{WR}}$ |
| $T_{RLAZ}$ | $\overline{\text{RD}}$ Low to Address Float |
| $T_{WHLH}$ | $\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE high |

**Table 31.** AC Parameters for a Variable Clock: Derating Formula

| Symbol | Type | Standard Clock | X2 Clock | -M | -V | -L | Units |
|---|---|---|---|---|---|---|---|
| $T_{RLRH}$ | Min | 6 T - x | 3 T - x | 20 | 15 | 25 | ns |
| $T_{WLWH}$ | Min | 6 T - x | 3 T - x | 20 | 15 | 25 | ns |
| $T_{RLDV}$ | Max | 5 T - x | 2.5 T - x | 25 | 23 | 30 | ns |
| $T_{RHDX}$ | Min | x | x | 0 | 0 | 0 | ns |
| $T_{RHDZ}$ | Max | 2 T - x | T - x | 20 | 15 | 25 | ns |
| $T_{LLDV}$ | Max | 8 T - x | 4T -x | 40 | 35 | 45 | ns |
| $T_{AVDV}$ | Max | 9 T - x | 4.5 T - x | 60 | 50 | 65 | ns |
| $T_{LLWL}$ | Min | 3 T - x | 1.5 T - x | 25 | 20 | 30 | ns |
| $T_{LLWL}$ | Max | 3 T + x | 1.5 T + x | 25 | 20 | 30 | ns |
| $T_{AVWL}$ | Min | 4 T - x | 2 T - x | 25 | 20 | 30 | ns |
| $T_{QVWX}$ | Min | T - x | 0.5 T - x | 15 | 10 | 20 | ns |
| $T_{QVWH}$ | Min | 7 T - x | 3.5 T - x | 15 | 10 | 20 | ns |
| $T_{WHQX}$ | Min | T - x | 0.5 T - x | 10 | 8 | 15 | ns |
| $T_{RLAZ}$ | Max | x | x | 0 | 0 | 0 | ns |
| $T_{WHLH}$ | Min | T - x | 0.5 T - x | 15 | 10 | 20 | ns |
| $T_{WHLH}$ | Max | T + x | 0.5 T + x | 15 | 10 | 20 | ns |

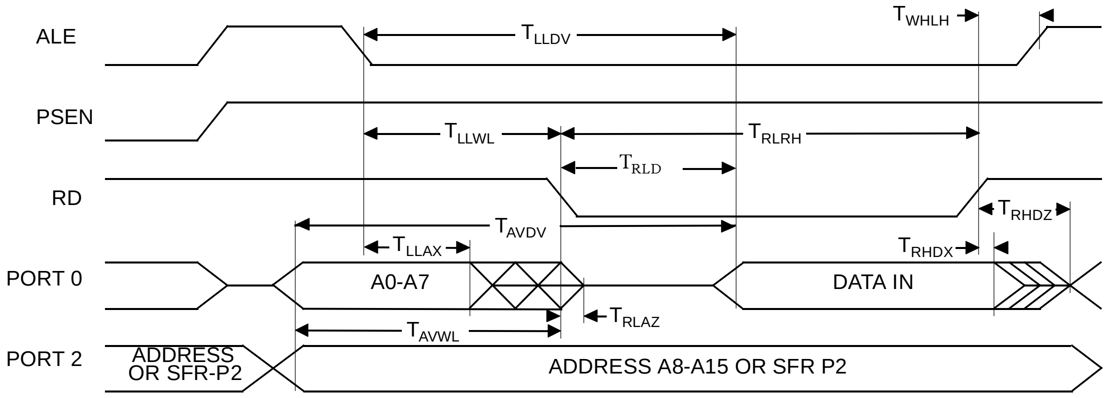
## External Data Memory Write Cycle

**Figure 19.** External Data Memory Write Cycle



## External Data Memory Read Cycle

**Figure 20.** External Data Memory Read Cycle



## Serial Port Timing - Shift Register Mode

**Table 32.** Symbol Description

| Symbol | Parameter |
|---|---|
| $T_{XLXL}$ | Serial port clock cycle time |
| $T_{QVHX}$ | Output data set-up to clock rising edge |
| $T_{XHQX}$ | Output data hold after clock rising edge |
| $T_{XHDX}$ | Input data hold after clock rising edge |
| $T_{XHDV}$ | Clock rising edge to input data valid |

**Table 33.** AC Parameters for a Fix Clock

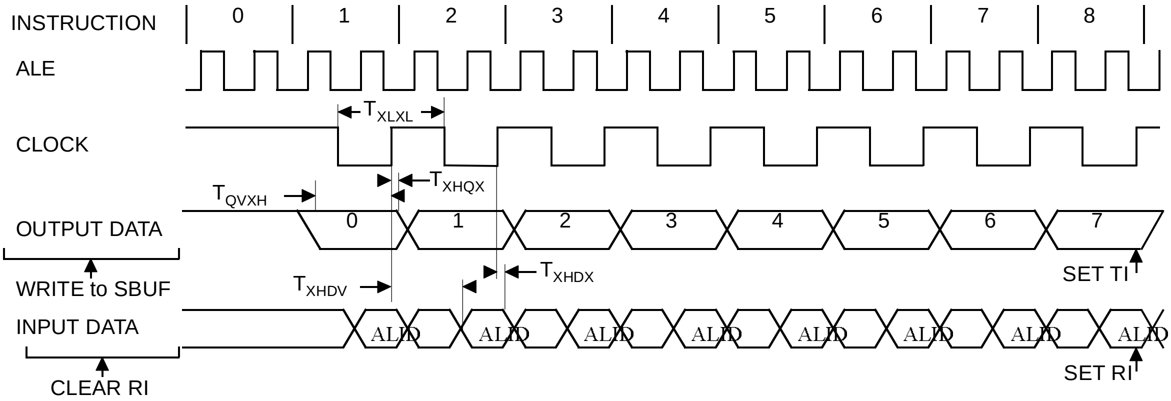
| Speed | -M 40 MHz | | -V X2 mode 30 MHz 60 MHz equiv. | | -V standard mode 40 MHz | | -L X2 mode 20 MHz 40 MHz equiv. | | -L standard mode 30 MHz | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $T_{XLXL}$ | 300 | | 200 | | 300 | | 300 | | 400 | | ns |
| $T_{QVHX}$ | 200 | | 117 | | 200 | | 200 | | 283 | | ns |
| $T_{XHQX}$ | 30 | | 13 | | 30 | | 30 | | 47 | | ns |
| $T_{XHDX}$ | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $T_{XHDV}$ | | 117 | | 34 | | 117 | | 117 | | 200 | ns |

**Table 34.** AC Parameters for a Variable Clock: Derating Formula

| Symbol | Type | Standard Clock | X2 Clock | -M | -V | -L | Units |
|---|---|---|---|---|---|---|---|
| $T_{XLXL}$ | Min | 12 T | 6 T | | | | ns |
| $T_{QVHX}$ | Min | 10 T - x | 5 T - x | 50 | 50 | 50 | ns |
| $T_{XHQX}$ | Min | 2 T - x | T - x | 20 | 20 | 20 | ns |
| $T_{XHDX}$ | Min | x | x | 0 | 0 | 0 | ns |
| $T_{XHDV}$ | Max | 10 T - x | 5 T- x | 133 | 133 | 133 | ns |

## Shift Register Timing Waveforms

**Figure 21.** Shift Register Timing Waveforms



## EPROM Programming and Verification Characteristics

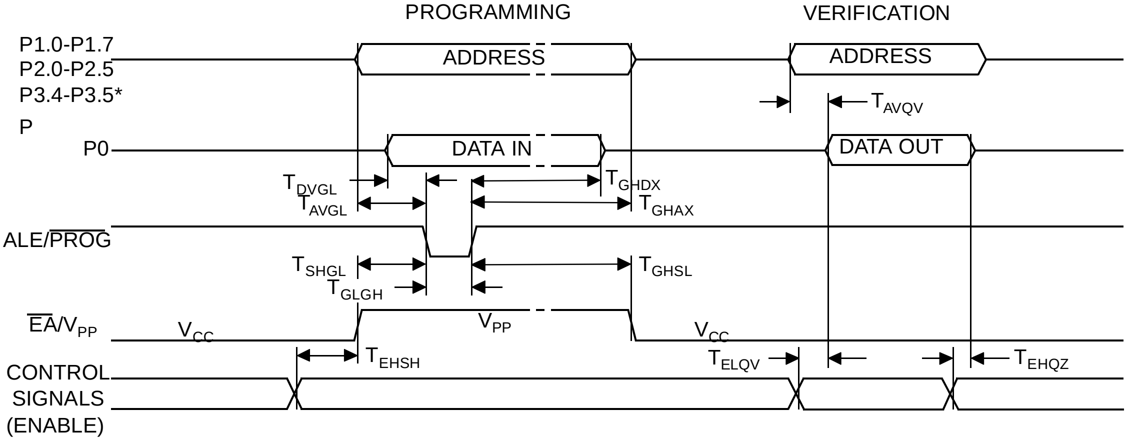
$T_A = 21°C$ to $27°C$; $V_{SS} = 0V$; $V_{CC} = 5V \pm 10\%$ while programming. $V_{CC}$ = operating range while verifying.

**Table 35.** EPROM Programming Parameters

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $V_{PP}$ | Programming Supply Voltage | 12.5 | 13 | V |
| $I_{PP}$ | Programming Supply Current | | 75 | mA |
| $1/T_{CLCL}$ | Oscillator Frquency | 4 | 6 | MHz |
| $T_{AVGL}$ | Address Setup to $\overline{\text{PROG}}$ Low | 48 $T_{CLCL}$ | | |
| $T_{GHAX}$ | Adress Hold after $\overline{\text{PROG}}$ | 48 $T_{CLCL}$ | | |
| $T_{DVGL}$ | Data Setup to $\overline{\text{PROG}}$ Low | 48 $T_{CLCL}$ | | |
| $T_{GHDX}$ | Data Hold after $\overline{\text{PROG}}$ | 48 $T_{CLCL}$ | | |
| $T_{EHSH}$ | (Enable) High to $V_{PP}$ | 48 $T_{CLCL}$ | | |
| $T_{SHGL}$ | $V_{PP}$ Setup to $\overline{\text{PROG}}$ Low | 10 | | µs |
| $T_{GHSL}$ | $V_{PP}$ Hold after $\overline{\text{PROG}}$ | 10 | | µs |
| $T_{GLGH}$ | $\overline{\text{PROG}}$ Width | 90 | 110 | µs |
| $T_{AVQV}$ | Address to Valid Data | | 48 $T_{CLCL}$ | |
| $T_{ELQV}$ | ENABLE Low to Data Valid | | 48 $T_{CLCL}$ | |
| $T_{EHQZ}$ | Data Float after ENABLE | 0 | 48 $T_{CLCL}$ | |

## EPROM Programming and Verification Waveforms

**Figure 22.** EPROM Programming and Verification Waveforms



* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

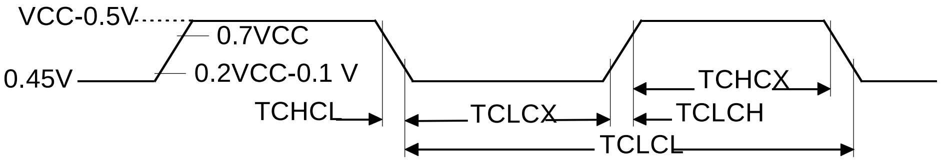
## External Clock Drive Characteristics (XTAL1)

**Table 36.** AC Parameters

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $T_{CLCL}$ | Oscillator Period | 25 |  | ns |
| $T_{CHCX}$ | High Time | 5 |  | ns |
| $T_{CLCX}$ | Low Time | 5 |  | ns |
| $T_{CLCH}$ | Rise Time |  | 5 | ns |
| $T_{CHCL}$ | Fall Time |  | 5 | ns |
| $T_{CHCX}/T_{CLCX}$ | Cyclic ratio in X2 mode | 40 | 60 | % |

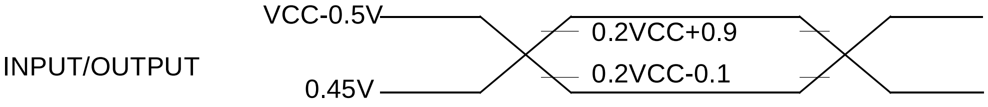
## External Clock Drive Waveforms

**Figure 23.** External Clock Drive Waveforms



## AC Testing Input/Output Waveforms

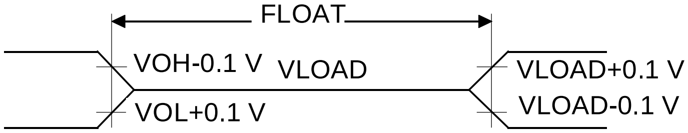
**Figure 24.** AC Testing Input/Output Waveforms



AC inputs during testing are driven at $V_{CC}$ - 0.5 for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at $V_{IH}$ min for a logic “1” and $V_{IL}$ max for a logic “0”.

## Float Waveforms

**Figure 25.** Float Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded $V_{OH}/V_{OL}$ level occurs. $I_{OL}/I_{OH} \geq \pm$ 20mA.

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