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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

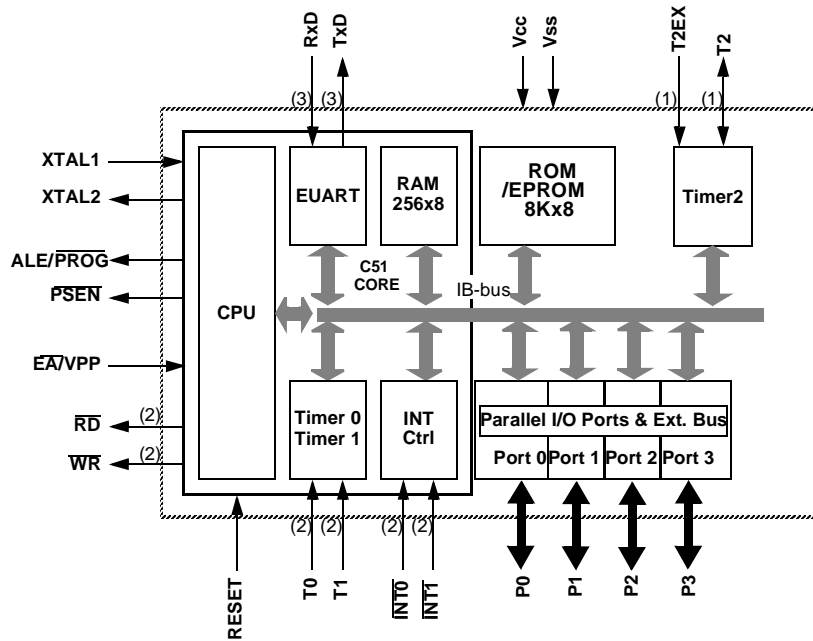
#### Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/atmel/at80c32x2-slsul">https://www.e-xfl.com/product-detail/atmel/at80c32x2-slsul</a>

**Table 1. Memory Size**

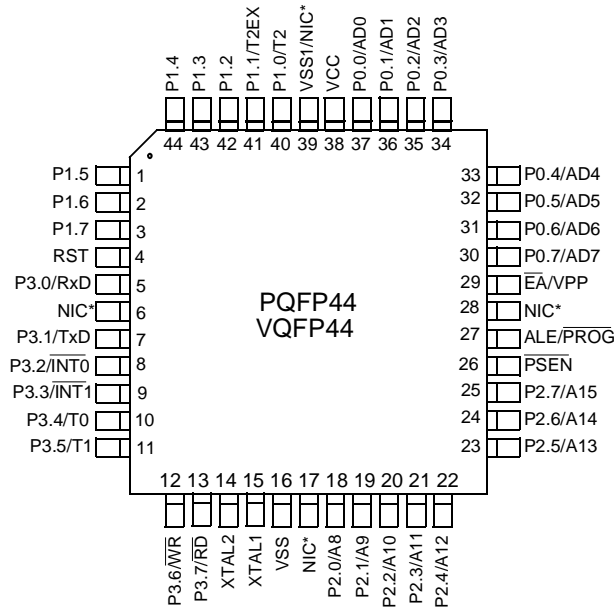
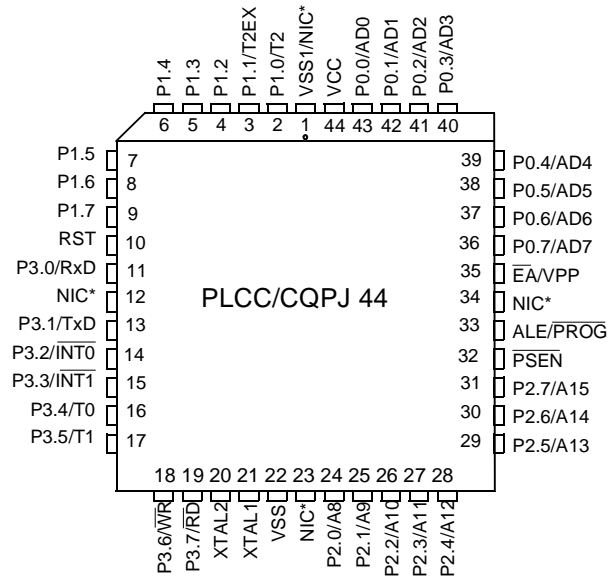
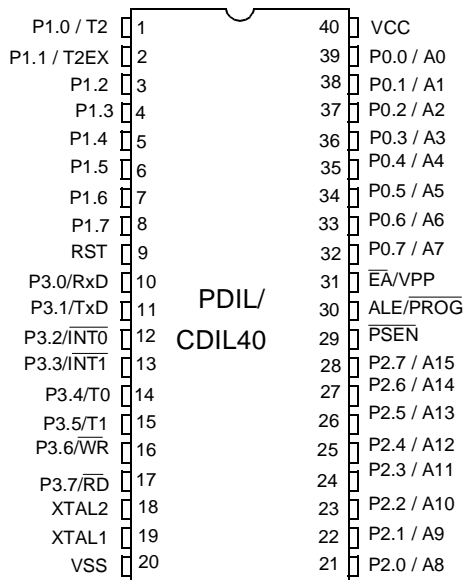
	ROM (bytes)	EPROM (bytes)	TOTAL RAM (bytes)
TS80C32X2	0	0	256
TS80C52X2	8k	0	256
TS87C52X2	0	8k	256

## Block Diagram



- Notes: 1. Alternate function of Port 1  
2. Alternate function of Port 3

# Pin Configuration



\*NIC: No Internal Connection

Mnemonic	Pin Number			Type	Name and Function
	DIL	LCC	VQFP 1.4		
V <sub>SS</sub>	20	22	16	I	<b>Ground:</b> 0V reference
V <sub>SS1</sub>		1	39	I	Optional Ground: <b>Contact the Sales Office for ground connection.</b>
V <sub>CC</sub>	40	44	38	I	<b>Power Supply:</b> This is the power supply voltage for normal, idle and power-down operation
P0.0-P0.7	39-32	43-36	37-30	I/O	<b>Port 0:</b> Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to V <sub>CC</sub> or V <sub>SS</sub> in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes.
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	<b>Port 1:</b> Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification.  Alternate functions for Port 1 include:
	1	2	40	I/O	<b>T2 (P1.0):</b> Timer/Counter 2 external count input/Clockout
	2	3	41	I	<b>T2EX (P1.1):</b> Timer/Counter 2 Reload/Capture/Direction Control
P2.0-P2.7	21-28	24-31	18-25	I/O	<b>Port 2:</b> Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX atDPTR). In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX atRi), port 2 emits the contents of the P2 SFR. Some Port 2 pins receive the high order address bits during EPROM programming and verification: P2.0 to P2.4
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	<b>Port 3:</b> Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below.
	10	11	5	I	<b>RXD (P3.0):</b> Serial input port
	11	13	7	O	<b>TXD (P3.1):</b> Serial output port
	12	14	8	I	<b>INT0 (P3.2):</b> External interrupt 0

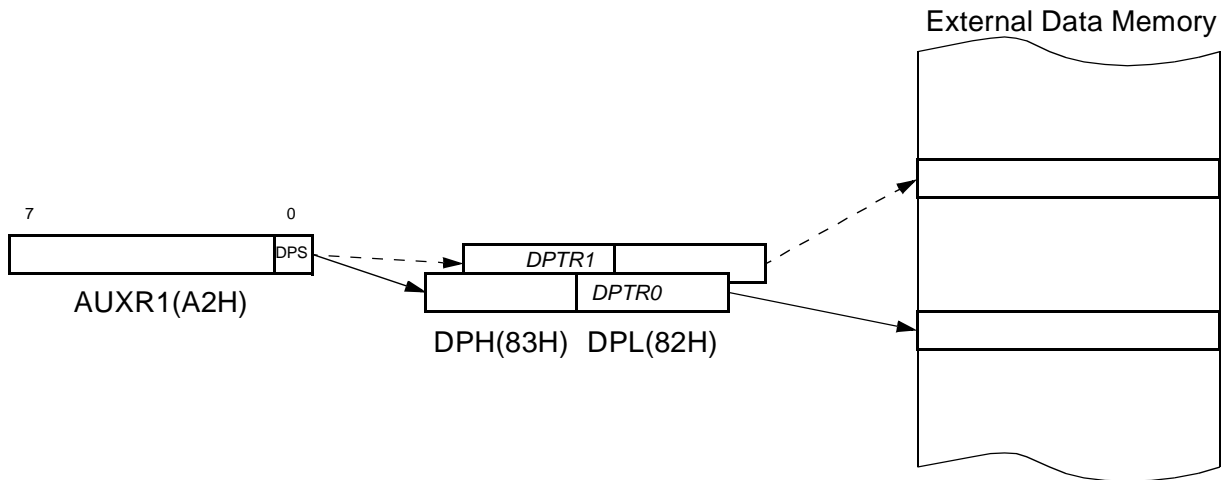
Mnemonic	Pin Number			Type	Name and Function
	DIL	LCC	VQFP 1.4		
	13	15	9	I	$\overline{\text{INT1}}$ (P3.3): External interrupt 1
	14	16	10	I	<b>T0</b> (P3.4): Timer 0 external input
	15	17	11	I	<b>T1</b> (P3.5): Timer 1 external input
	16	18	12	O	$\overline{\text{WR}}$ (P3.6): External data memory write strobe
	17	19	13	O	$\overline{\text{RD}}$ (P3.7): External data memory read strobe
Reset	9	10	4	I	<b>Reset:</b> A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to $V_{SS}$ permits a power-on reset using only an external capacitor to $V_{CC}$ .
ALE/ $\overline{\text{PROG}}$	30	33	27	O (I)	<b>Address Latch Enable/Program Pulse:</b> Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ( $\overline{\text{PROG}}$ ) during EPROM programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
PSEN	29	32	26	O	<b>Program Store Enable:</b> The read strobe to external program memory. When executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.
$\overline{\text{EA}}/V_{PP}$	31	35	29	I	<b>External Access Enable/Programming Supply Voltage:</b> $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH (RB) or 7FFFH (RC), or FFFFH (RD). If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (RB) or 7FFFH (RC) $\overline{\text{EA}}$ must be held low for ROMless devices. This pin also receives the 12.75V programming supply voltage ( $V_{PP}$ ) during EPROM programming. If security level 1 is programmed, $\overline{\text{EA}}$ will be internally latched on Reset.
XTAL1	19	21	15	I	<b>Crystal 1:</b> Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	<b>Crystal 2:</b> Output from the inverting oscillator amplifier

## Dual Data Pointer Register (Ddptr)

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called DPS = AUXR1/bit0 (See Table 5.) that allows the program code to switch between them (Refer to Figure 3).

**Figure 3.** Use of Dual Pointer



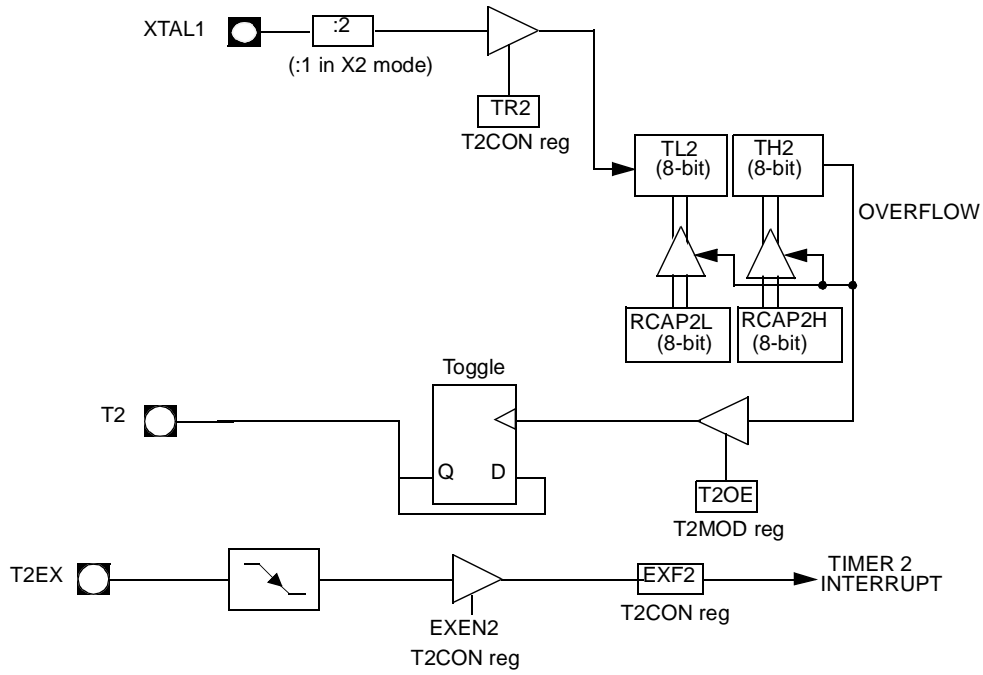
**Table 4.** AUXR1: Auxiliary Register 1

7	6	5	4	3	2	1	0
-	-	-	-	GF3	0	-	DPS
Bit Number	Bit Mnemonic	Description					
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
3	GF3	This bit is a general purpose user flag					
2	0	<b>Reserved</b> Always stuck at 0					
1	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
0	DPS	<b>Data Pointer Selection</b> Clear to select DPTR0. Set to select DPTR1.					

Reset Value = XXXX XXX0

Not bit addressable

**Figure 5.** Clock-Out Mode  $C/\overline{T2} = 0$



**Table 6.** T2MOD Register  
T2MOD - Timer 2 Mode Control Register (C9h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN
Bit Number	Bit Mnemonic	Description					
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
4	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
3	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
2	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
1	T2OE	<b>Timer 2 Output Enable bit</b> Clear to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.					
0	DCEN	<b>Down Counter Enable bit</b> Clear to disable timer 2 as up/down counter. Set to enable timer 2 as up/down counter.					

Reset Value = XXXX XX00b

Not bit addressable



**TS80C52X2 Serial I/O Port**

The serial I/O port in the TS80C52X2 is compatible with the serial I/O port in the 80C52. It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

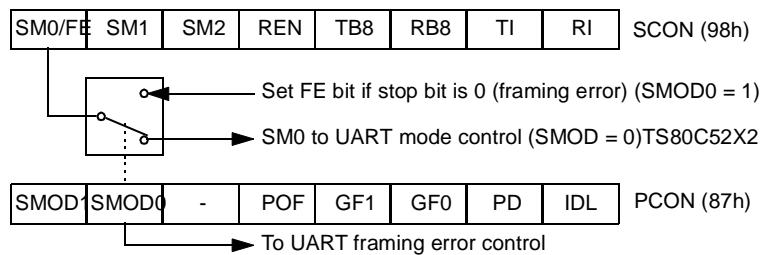
Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

**Framing Error Detection**

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 6).

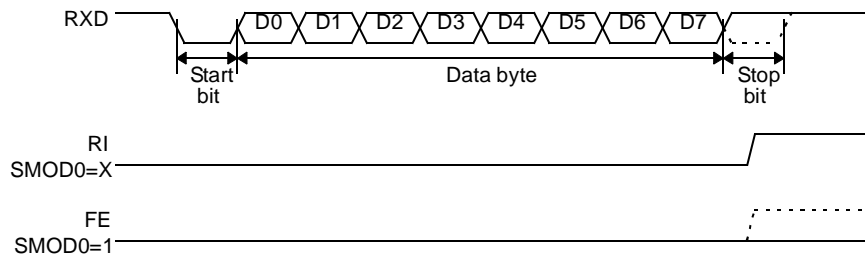
**Figure 6. Framing Error Block Diagram**



When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 9.) bit is set.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 7. and Figure 8.).

**Figure 7. UART Timings in Mode 1**



**Table 10.** PCON Register  
PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
Bit Number	Bit Mnemonic	Description					
7	SMOD1	<b>Serial port Mode bit 1</b> Set to select double baud rate in mode 1, 2 or 3.					
6	SMOD0	<b>Serial port Mode bit 0</b> Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.					
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
4	POF	<b>Power-off Flag</b> Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.					
3	GF1	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.					
2	GF0	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.					
1	PD	<b>Power-down mode bit</b> Cleared by hardware when reset occurs. Set to enter power-down mode.					
0	IDL	<b>Idle mode bit</b> Clear by hardware when interrupt or reset occurs. Set to enter idle mode.					

Reset Value = 00X1 0000b

Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

**Table 13.** IP Register  
IP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	-	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	PT2	<b>Timer 2 overflow interrupt Priority bit</b> Refer to PT2H for priority level.
4	PS	<b>Serial port Priority bit</b> Refer to PSH for priority level.
3	PT1	<b>Timer 1 overflow interrupt Priority bit</b> Refer to PT1H for priority level.
2	PX1	<b>External interrupt 1 Priority bit</b> Refer to PX1H for priority level.
1	PT0	<b>Timer 0 overflow interrupt Priority bit</b> Refer to PT0H for priority level.
0	PX0	<b>External interrupt 0 Priority bit</b> Refer to PX0H for priority level.

Reset Value = XX00 0000b  
Bit addressable

**Table 14.** IPH Register  
IPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0															
-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H															
Bit Number	Bit Mnemonic	Description																				
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.																				
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.																				
5	PT2H	<b>Timer 2 overflow interrupt Priority High bit</b> <table border="1"> <thead> <tr> <th>PT2H</th> <th>PT2</th> <th>Priority Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </tbody> </table>						PT2H	PT2	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT2H	PT2	Priority Level																				
0	0	Lowest																				
0	1																					
1	0																					
1	1	Highest																				
4	PSH	<b>Serial port Priority High bit</b> <table border="1"> <thead> <tr> <th>PSH</th> <th>PS</th> <th>Priority Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </tbody> </table>						PSH	PS	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PSH	PS	Priority Level																				
0	0	Lowest																				
0	1																					
1	0																					
1	1	Highest																				
3	PT1H	<b>Timer 1 overflow interrupt Priority High bit</b> <table border="1"> <thead> <tr> <th>PT1H</th> <th>PT1</th> <th>Priority Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </tbody> </table>						PT1H	PT1	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT1H	PT1	Priority Level																				
0	0	Lowest																				
0	1																					
1	0																					
1	1	Highest																				
2	PX1H	<b>External interrupt 1 Priority High bit</b> <table border="1"> <thead> <tr> <th>PX1H</th> <th>PX1</th> <th>Priority Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </tbody> </table>						PX1H	PX1	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PX1H	PX1	Priority Level																				
0	0	Lowest																				
0	1																					
1	0																					
1	1	Highest																				
1	PT0H	<b>Timer 0 overflow interrupt Priority High bit</b> <table border="1"> <thead> <tr> <th>PT0H</th> <th>PT0</th> <th>Priority Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </tbody> </table>						PT0H	PT0	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT0H	PT0	Priority Level																				
0	0	Lowest																				
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0	PX0H	<b>External interrupt 0 Priority High bit</b> <table border="1"> <thead> <tr> <th>PX0H</th> <th>PX0</th> <th>Priority Level</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Lowest</td> </tr> <tr> <td>0</td> <td>1</td> <td></td> </tr> <tr> <td>1</td> <td>0</td> <td></td> </tr> <tr> <td>1</td> <td>1</td> <td>Highest</td> </tr> </tbody> </table>						PX0H	PX0	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PX0H	PX0	Priority Level																				
0	0	Lowest																				
0	1																					
1	0																					
1	1	Highest																				

Reset Value = XX00 0000b  
Not bit addressable



## Power-off Flag

The power-off flag allows the user to distinguish between a “cold start” reset and a “warm start” reset.

A cold start reset is the one induced by  $V_{CC}$  switch-on. A warm start reset occurs while  $V_{CC}$  is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 17.). POF is set by hardware when  $V_{CC}$  rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a  $V_{CC}$  range from 4.5V to 5.5V. For lower  $V_{CC}$  value, reading POF bit will return indeterminate value.

**Table 17.** PCON Register  
PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL
Bit Number	Bit Mnemonic	Description					
7	SMOD1	<b>Serial port Mode bit 1</b> Set to select double baud rate in mode 1, 2 or 3.					
6	SMOD0	<b>Serial port Mode bit 0</b> Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.					
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.					
4	POF	<b>Power-off Flag</b> Clear to recognize next reset type. Set by hardware when $V_{CC}$ rises from 0 to its nominal voltage. Can also be set by software.					
3	GF1	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.					
2	GF0	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.					
1	PD	<b>Power-down mode bit</b> Cleared by hardware when reset occurs. Set to enter power-down mode.					
0	IDL	<b>Idle mode bit</b> Clear by hardware when interrupt or reset occurs. Set to enter idle mode.					

Reset Value = 00X1 0000b

Not bit addressable

Control and program signals must be held at the levels indicated in Table 35.

**Definition of terms**

**Address Lines:** P1.0-P1.7, P2.0-P2.4 respectively for A0-A12

**Data Lines:** P0.0-P0.7 for D0-D7

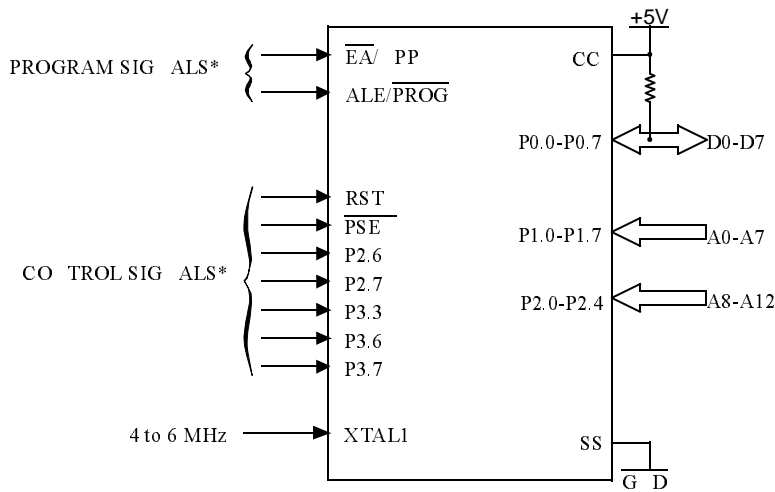
**Control Signals:** RST,  $\overline{\text{PSEN}}$ , P2.6, P2.7, P3.3, P3.6, P3.7.

**Program Signals:** ALE/ $\overline{\text{PROG}}$ ,  $\overline{\text{EA}}$ / $\overline{\text{VPP}}$ .

**Table 20.** EPROM Set-up Modes

Mode	RST	PSEN	ALE/ PROG	$\overline{\text{EA}}$ / VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code data	1	0		12.75V	0	1	1	1	1
Verify Code data	1	0	1	1	0		0	1	1
Program Encryption Array Address 0-3Fh	1	0		12.75V	0	1	1	0	1
Read Signature Bytes	1	0	1	1	0		0	0	0
Program Lock bit 1	1	0		12.75V	1	1	1	1	1
Program Lock bit 2	1	0		12.75V	1	1	1	0	0
Program Lock bit 3	1	0		12.75V	1	0	1	1	0

**Figure 11.** Set-Up Modes Configuration



\* See Table 31. for proper value on these inputs

### Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS87C52X2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise  $\overline{EA}/VPP$  from VCC to VPP (typical 12.75V).
- Step 5: Pulse  $\overline{ALE}/\overline{PROG}$  once.
- Step 6: Lower  $\overline{EA}/VPP$  from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 12.).

### Verify Algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C52X2.

P 2.7 is used to enable data output.

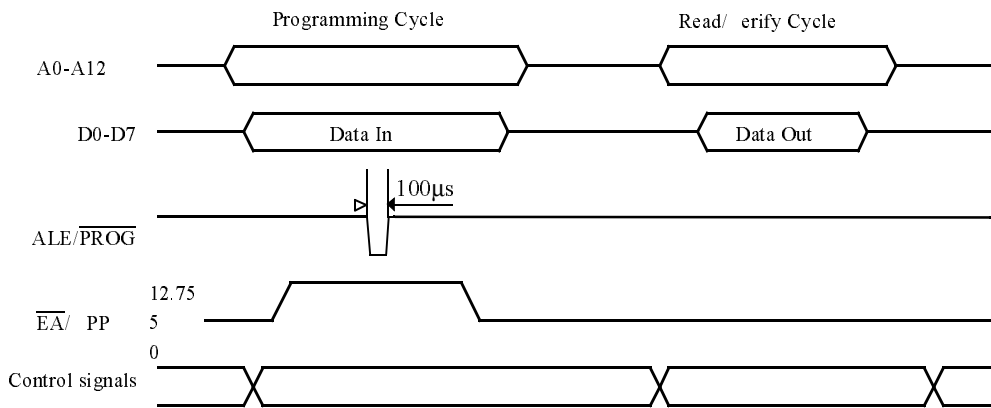
To verify the TS87C52X2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 12.)

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.

**Figure 12.** Programming and Verification Signal's Waveform



### EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

### Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm<sup>2</sup>. Exposing the EPROM to an ultraviolet lamp of



## Electrical Characteristics

### Absolute Maximum Ratings<sup>(1)</sup>

Ambient Temperature Under Bias:	
C = commercial.....	0°C to 70°C
I = industrial.....	-40°C to 85°C
Storage Temperature.....	-65°C to + 150°C
Voltage on V <sub>CC</sub> to V <sub>SS</sub> .....	-0.5V to + 7 V
Voltage on V <sub>PP</sub> to V <sub>SS</sub> .....	-0.5V to + 13 V
Voltage on Any Pin to V <sub>SS</sub> .....	-0.5V to V <sub>CC</sub> + 0.5V
Power Dissipation.....	1 W <sup>(2)</sup>

- Notes:
1. Stresses at or above those listed under “ Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
  2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

### Power Consumption Measurement

Since the introduction of the first C51 devices, every manufacturer made operating I<sub>cc</sub> measurements under reset, which made sense for the designs were the CPU was running under reset. In Atmel new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That’s why, while keeping measurements under Reset, Atmel presents a new way to measure the operating I<sub>cc</sub>:

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = V<sub>cc</sub>, RST = V<sub>ss</sub>, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating I<sub>cc</sub>.

### DC Parameters for Standard Voltage

T<sub>A</sub> = 0°C to +70°C; V<sub>SS</sub> = 0 V; V<sub>CC</sub> = 5V ± 10%; F = 0 to 40 MHz.

T<sub>A</sub> = -40°C to +85°C; V<sub>SS</sub> = 0 V; V<sub>CC</sub> = 5V ± 10%; F = 0 to 40 MHz.

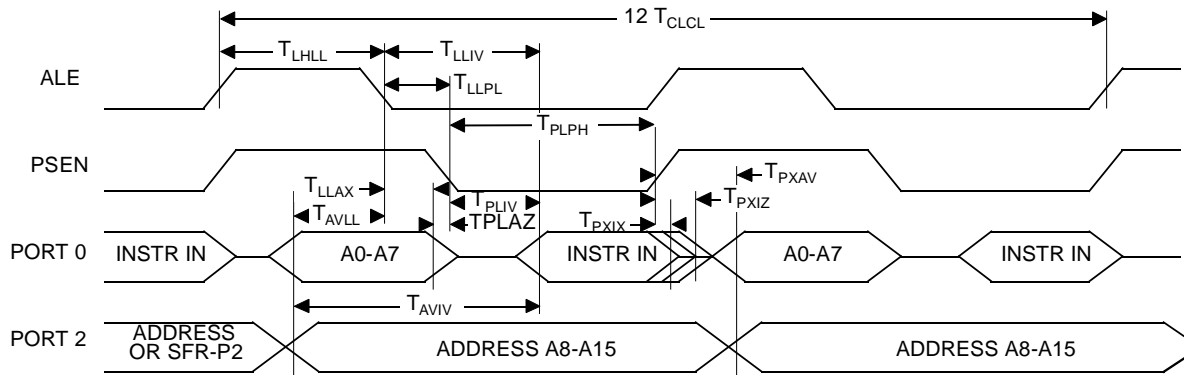
Table 22. DC Parameters in Standard Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V <sub>IL</sub>	Input Low Voltage	-0.5		0.2 V <sub>CC</sub> - 0.1	V	
V <sub>IH</sub>	Input High Voltage except XTAL1, RST	0.2 V <sub>CC</sub> + 0.9		V <sub>CC</sub> + 0.5	V	
V <sub>IH1</sub>	Input High Voltage, XTAL1, RST	0.7 V <sub>CC</sub>		V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage, ports 1, 2, 3 <sup>(6)</sup>			0.3	V	I <sub>OL</sub> = 100 μA <sup>(4)</sup>
				0.45	V	I <sub>OL</sub> = 1.6 mA <sup>(4)</sup>
				1.0	V	I <sub>OL</sub> = 3.5 mA <sup>(4)</sup>
V <sub>OL1</sub>	Output Low Voltage, port 0 <sup>(6)</sup>			0.3	V	I <sub>OL</sub> = 200 μA <sup>(4)</sup>
				0.45	V	I <sub>OL</sub> = 3.2 mA <sup>(4)</sup>
				1.0	V	I <sub>OL</sub> = 7.0 mA <sup>(4)</sup>
V <sub>OL2</sub>	Output Low Voltage, ALE, $\overline{\text{PSEN}}$			0.3	V	I <sub>OL</sub> = 100 μA <sup>(4)</sup>
				0.45	V	I <sub>OL</sub> = 1.6 mA <sup>(4)</sup>
				1.0	V	I <sub>OL</sub> = 3.5 mA <sup>(4)</sup>



**External Program Memory  
Read Cycle**

**Figure 18.** External Program Memory Read Cycle



**External Data Memory  
Characteristics**

**Table 29.** Symbol Description

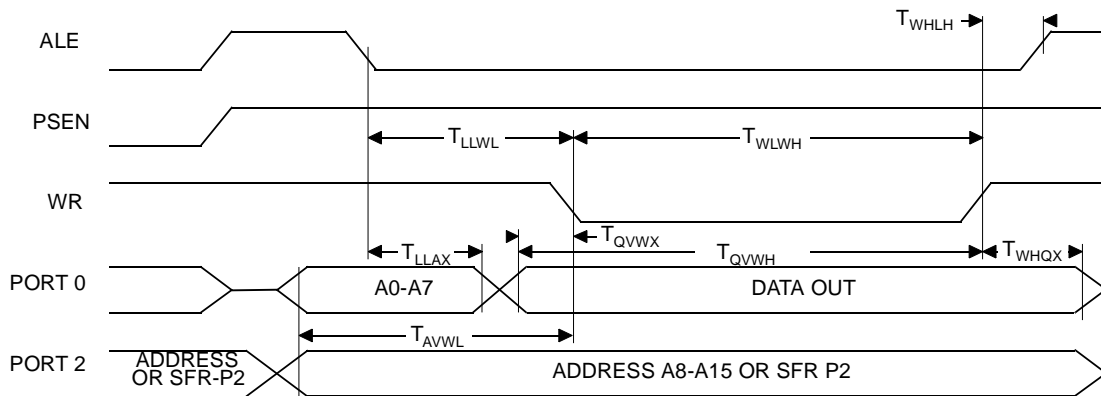
Symbol	Parameter
T <sub>RLRH</sub>	$\overline{RD}$ Pulse Width
T <sub>WLWH</sub>	$\overline{WR}$ Pulse Width
T <sub>RLDV</sub>	$\overline{RD}$ to Valid Data In
T <sub>RHDX</sub>	Data Hold After $\overline{RD}$
T <sub>RHDZ</sub>	Data Float After $\overline{RD}$
T <sub>LLDV</sub>	ALE to Valid Data In
T <sub>AVDV</sub>	Address to Valid Data In
T <sub>LLWL</sub>	ALE to $\overline{WR}$ or $\overline{RD}$
T <sub>AVWL</sub>	Address to $\overline{WR}$ or $\overline{RD}$
T <sub>QVWX</sub>	Data Valid to $\overline{WR}$ Transition
T <sub>QVWH</sub>	Data set-up to $\overline{WR}$ High
T <sub>WHQX</sub>	Data Hold After $\overline{WR}$
T <sub>RLAZ</sub>	$\overline{RD}$ Low to Address Float
T <sub>WHLH</sub>	$\overline{RD}$ or $\overline{WR}$ High to ALE high

**Table 31. AC Parameters for a Variable Clock: Derating Formula**

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
$T_{RLRH}$	Min	6 T - x	3 T - x	20	15	25	ns
$T_{WLWH}$	Min	6 T - x	3 T - x	20	15	25	ns
$T_{RLDV}$	Max	5 T - x	2.5 T - x	25	23	30	ns
$T_{RHDX}$	Min	x	x	0	0	0	ns
$T_{RHDZ}$	Max	2 T - x	T - x	20	15	25	ns
$T_{LLDV}$	Max	8 T - x	4T -x	40	35	45	ns
$T_{AVDV}$	Max	9 T - x	4.5 T - x	60	50	65	ns
$T_{LLWL}$	Min	3 T - x	1.5 T - x	25	20	30	ns
$T_{LLWL}$	Max	3 T + x	1.5 T + x	25	20	30	ns
$T_{AVWL}$	Min	4 T - x	2 T - x	25	20	30	ns
$T_{QVWX}$	Min	T - x	0.5 T - x	15	10	20	ns
$T_{QVWH}$	Min	7 T - x	3.5 T - x	15	10	20	ns
$T_{WHQX}$	Min	T - x	0.5 T - x	10	8	15	ns
$T_{RLAZ}$	Max	x	x	0	0	0	ns
$T_{WHLH}$	Min	T - x	0.5 T - x	15	10	20	ns
$T_{WHLH}$	Max	T + x	0.5 T + x	15	10	20	ns

**External Data Memory Write Cycle**

**Figure 19. External Data Memory Write Cycle**



## EPROM Programming and Verification Characteristics

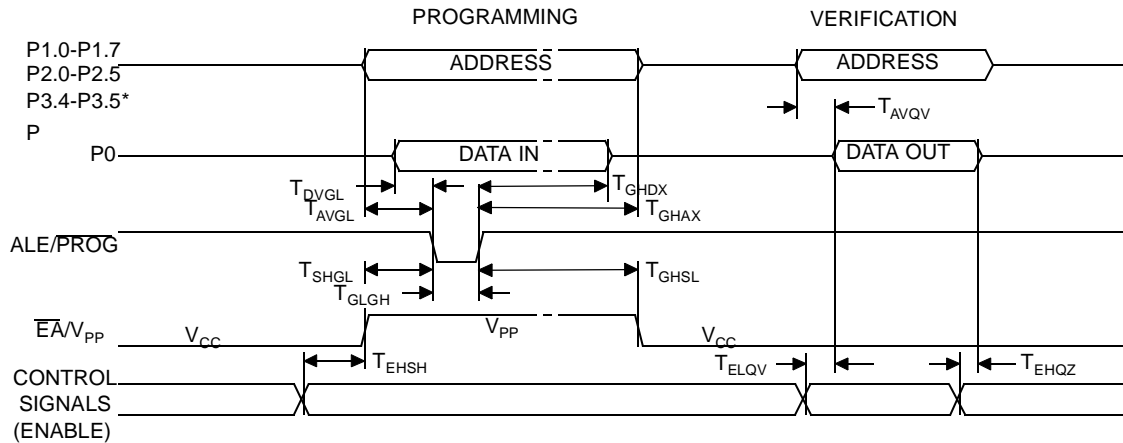
$T_A = 21^\circ\text{C}$  to  $27^\circ\text{C}$ ;  $V_{SS} = 0\text{V}$ ;  $V_{CC} = 5\text{V} \pm 10\%$  while programming.  $V_{CC}$  = operating range while verifying.

**Table 35.** EPROM Programming Parameters

Symbol	Parameter	Min	Max	Units
$V_{PP}$	Programming Supply Voltage	12.5	13	V
$I_{PP}$	Programming Supply Current		75	mA
$1/T_{CLCL}$	Oscillator Frequency	4	6	MHz
$T_{AVGL}$	Address Setup to $\overline{\text{PROG}}$ Low	$48 T_{CLCL}$		
$T_{GHAX}$	Address Hold after $\overline{\text{PROG}}$	$48 T_{CLCL}$		
$T_{DVGL}$	Data Setup to $\overline{\text{PROG}}$ Low	$48 T_{CLCL}$		
$T_{GHDX}$	Data Hold after $\overline{\text{PROG}}$	$48 T_{CLCL}$		
$T_{EHS}$	(Enable) High to $V_{PP}$	$48 T_{CLCL}$		
$T_{SHGL}$	$V_{PP}$ Setup to $\overline{\text{PROG}}$ Low	10		$\mu\text{s}$
$T_{GHSL}$	$V_{PP}$ Hold after $\overline{\text{PROG}}$	10		$\mu\text{s}$
$T_{GLGH}$	$\overline{\text{PROG}}$ Width	90	110	$\mu\text{s}$
$T_{AVQV}$	Address to Valid Data		$48 T_{CLCL}$	
$T_{ELQV}$	ENABLE Low to Data Valid		$48 T_{CLCL}$	
$T_{EHQZ}$	Data Float after ENABLE	0	$48 T_{CLCL}$	

## EPROM Programming and Verification Waveforms

**Figure 22.** EPROM Programming and Verification Waveforms

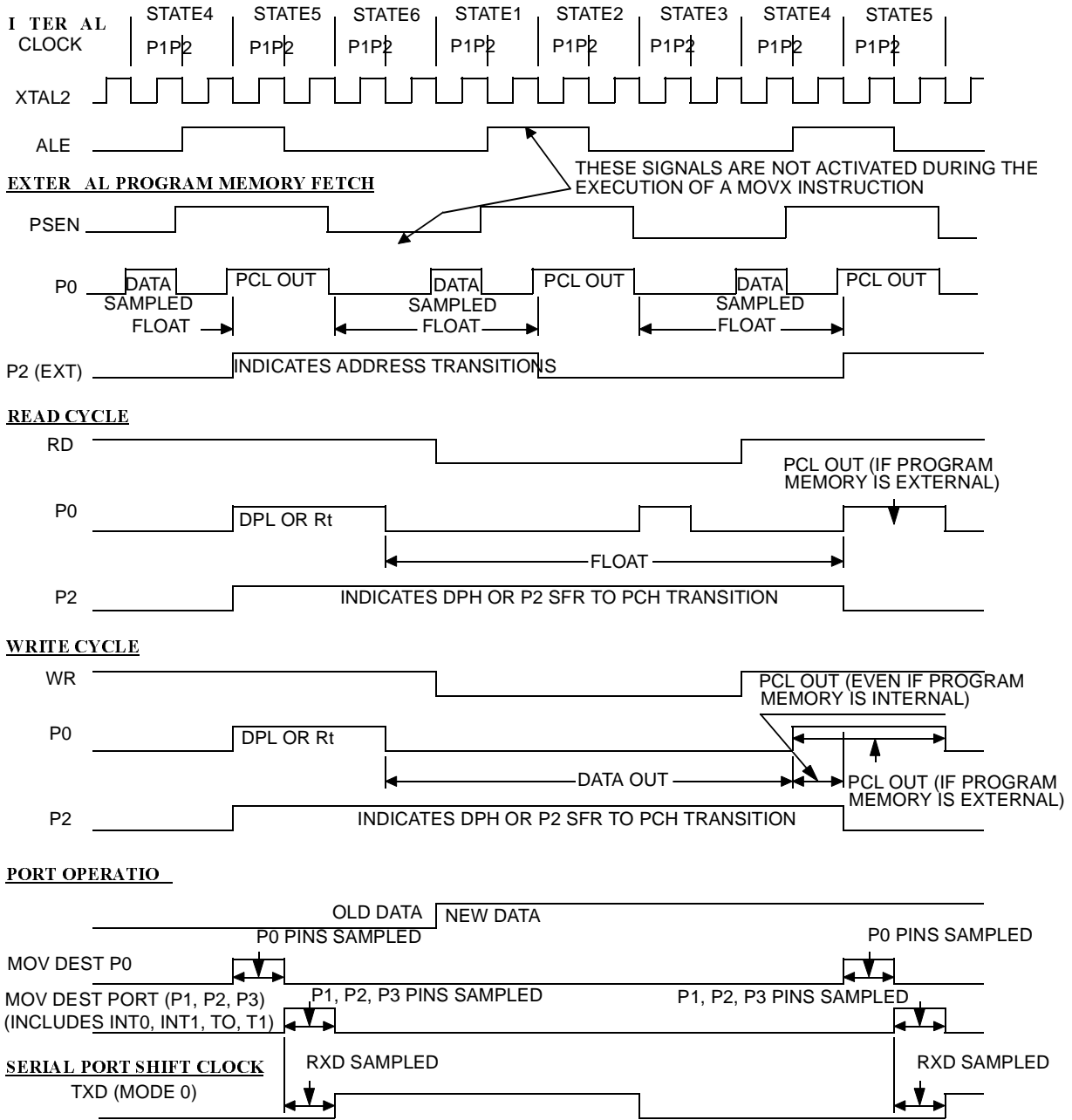


\* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

### Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 signal must be changed to XTAL2 divided by two.

**Figure 26.** Clock Waveforms



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though ( $T_A = 25^\circ\text{C}$  fully loaded)  $\overline{\text{RD}}$  and  $\overline{\text{WR}}$  propagation delays are approximately 50ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.



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