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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

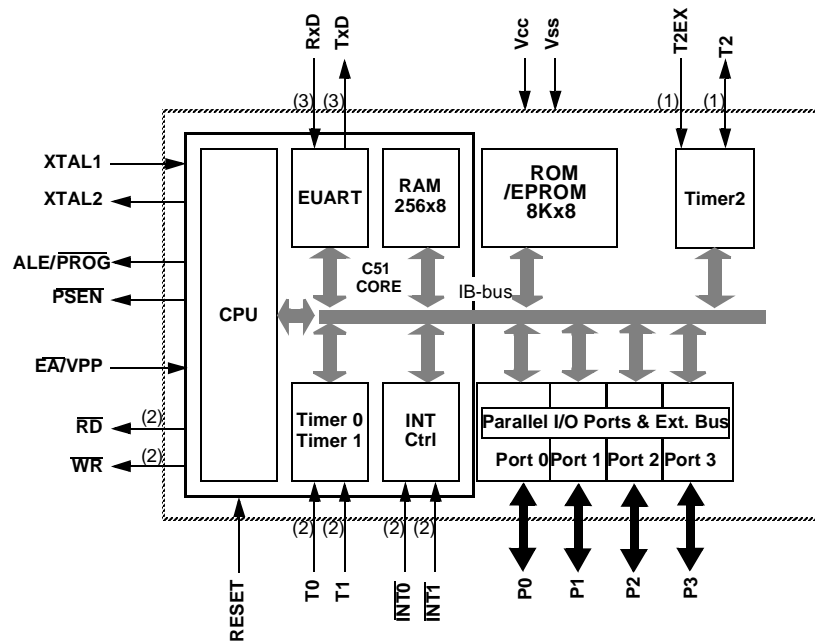
#### Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/ts80c32x2-lia">https://www.e-xfl.com/product-detail/microchip-technology/ts80c32x2-lia</a>

**Table 1. Memory Size**

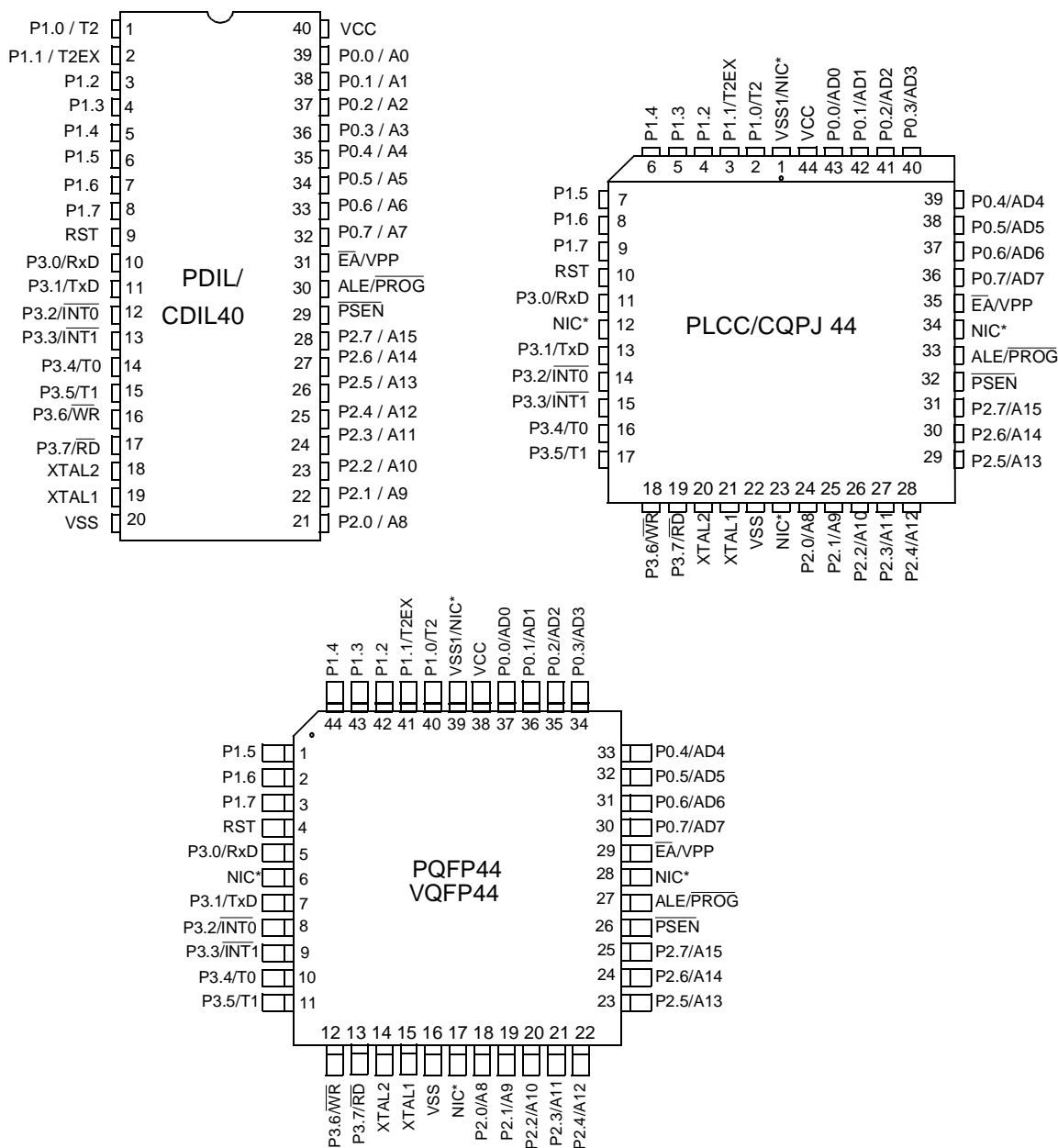
	ROM (bytes)	EPROM (bytes)	TOTAL RAM (bytes)
TS80C32X2	0	0	256
TS80C52X2	8k	0	256
TS87C52X2	0	8k	256

## Block Diagram



- Notes:
1. Alternate function of Port 1
  2. Alternate function of Port 3

## Pin Configuration



\*NIC: No Internal Connection

Mnemonic	Pin Number			Type	Name and Function
	DIL	LCC	VQFP 1.4		
V <sub>SS</sub>	20	22	16	I	<b>Ground:</b> 0V reference
V <sub>SS1</sub>		1	39	I	Optional Ground: <b>Contact the Sales Office for ground connection.</b>
V <sub>CC</sub>	40	44	38	I	<b>Power Supply:</b> This is the power supply voltage for normal, idle and power-down operation
P0.0-P0.7	39-32	43-36	37-30	I/O	<p><b>Port 0:</b> Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs. Port 0 pins must be polarized to V<sub>CC</sub> or V<sub>SS</sub> in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes.</p>
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	
					<p>Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification.</p> <p>Alternate functions for Port 1 include:</p>
	1	2	40	I/O	<b>T2 (P1.0):</b> Timer/Counter 2 external count input/Clockout
	2	3	41	I	<b>T2EX (P1.1):</b> Timer/Counter 2 Reload/Capture/Direction Control
P2.0-P2.7	21-28	24-31	18-25	I/O	<p><b>Port 2:</b> Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX atDPTR). In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX atRi), port 2 emits the contents of the P2 SFR. Some Port 2 pins receive the high order address bits during EPROM programming and verification: P2.0 to P2.4</p>
P3.0-P3.7	10-17	11, 13-19	5, 7-13	I/O	
					<p>Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below.</p>
	10	11	5	I	<b>RXD (P3.0):</b> Serial input port
	11	13	7	O	<b>TXD (P3.1):</b> Serial output port
	12	14	8	I	<b>INT0 (P3.2):</b> External interrupt 0

## Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.

### ASSEMBLY LANGUAGE

```

; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2  AUXR1 EQU 0A2H
;
0000 909000 MOV DPTR,#SOURCE ; address of SOURCE
0003 05A2 INC AUXR1 ; switch data pointers
0005 90A000 MOV DPTR,#DEST ; address of DEST
0008  LOOP:
0008 05A2 INC AUXR1 ; switch data pointers
000A E0 MOVX A,atDPTR ; get a byte from SOURCE
000B A3 INC DPTR ; increment SOURCE address
000C 05A2 INC AUXR1 ; switch data pointers
000E F0 MOVX atDPTR,A ; write the byte to DEST
000F A3 INC DPTR ; increment DEST address
0010 70F6JNZ LOOP ; check for 0 terminator
0012 05A2 INC AUXR1 ; (optional) restore DPS

```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

## Timer 2

The timer 2 in the TS80C52X2 is compatible with the timer 2 in the 80C52.

It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 5) and T2MOD register (See Table 6). Timer 2 operation is similar to Timer 0 and Timer 1. C/T2 selects  $F_{OSC}/12$  (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/RL2 (T2CON), as described in the Atmel 8-bit Microcontroller Hardware description.

Refer to the Atmel 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C52X2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

### Auto-reload Mode

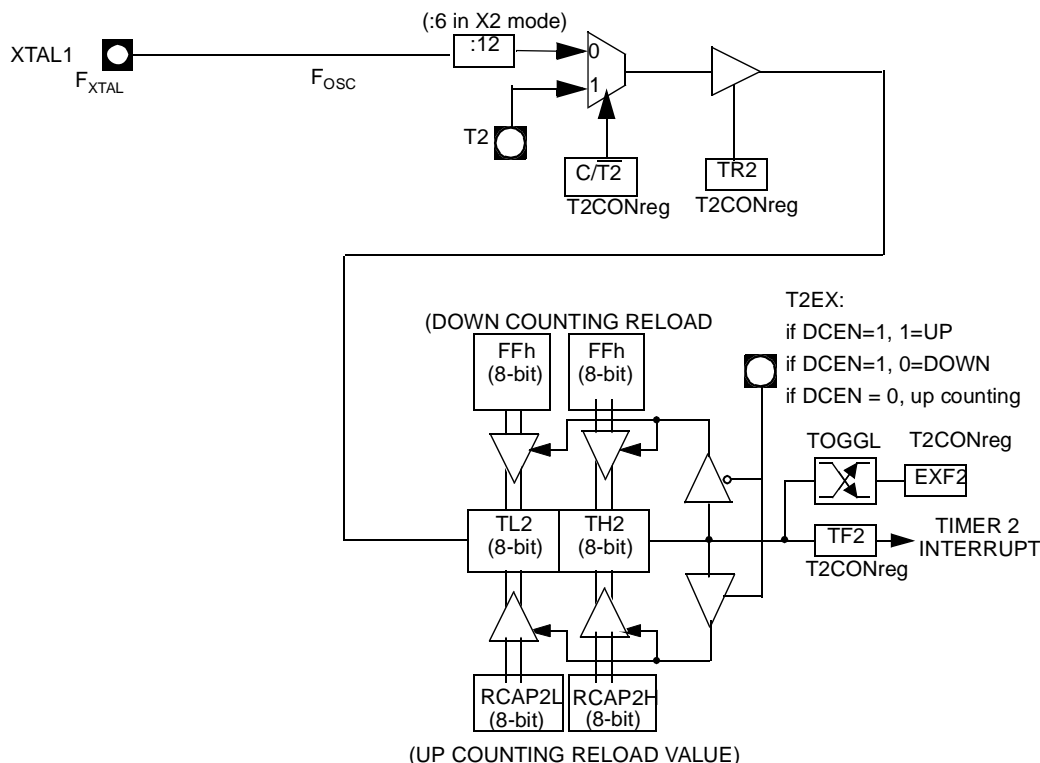
The Auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 4. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.

**Figure 4. Auto-reload Mode Up/Down Counter (DCEN = 1)**



## Programmable Clock-output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 5) . The input clock increments TL2 at frequency  $F_{OSC}/2$ . The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers :

$$Clock-OutFrequency = \frac{F_{osc}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz ( $F_{OSC}/2^{16}$ ) to 4 MHz ( $F_{OSC}/4$ ). The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear  $\overline{C/T2}$  bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.
- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.

It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.

**Table 9.** SCON Register  
SCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0																									
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI																									
Bit Number	Bit Mnemonic	Description																														
7	FE	<b>Framing Error bit (SMOD0=1)</b> Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit																														
	SM0	<b>Serial port Mode bit 0</b> Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit																														
6	SM1	<b>Serial port Mode bit 1</b> <table><thead><tr><th>SM0</th><th>SM1</th><th>Mode</th><th>Description</th><th>Baud Rate</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>Shift Register</td><td><math>F_{XTAL}/12</math> (/6 in X2 mode)</td></tr><tr><td>0</td><td>1</td><td>1</td><td>8-bit UART</td><td>Variable</td></tr><tr><td>1</td><td>0</td><td>2</td><td>9-bit UART</td><td><math>F_{XTAL}/64</math> or <math>F_{XTAL}/32</math> (/32, /16 in X2 mode)</td></tr><tr><td>1</td><td>1</td><td>3</td><td>9-bit UART</td><td>Variable</td></tr></tbody></table>						SM0	SM1	Mode	Description	Baud Rate	0	0	0	Shift Register	$F_{XTAL}/12$ (/6 in X2 mode)	0	1	1	8-bit UART	Variable	1	0	2	9-bit UART	$F_{XTAL}/64$ or $F_{XTAL}/32$ (/32, /16 in X2 mode)	1	1	3	9-bit UART	Variable
SM0	SM1	Mode	Description	Baud Rate																												
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1	1	3	9-bit UART	Variable																												
5	SM2	<b>Serial port Mode 2 bit / Multiprocessor Communication Enable bit</b> Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.																														
4	REN	<b>Reception Enable bit</b> Clear to disable serial reception. Set to enable serial reception.																														
3	TB8	Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3. Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.																														
2	RB8	<b>Receiver Bit 8 / Ninth bit received in modes 2 and 3</b> Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.																														
1	TI	<b>Transmit Interrupt flag</b> Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.																														
0	RI	<b>Receive Interrupt flag</b> Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 7. and Figure 8. in the other modes.																														

Reset Value = 0000 0000b

Bit addressable



are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

**Table 12.** IE Register  
IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	-	ET2	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	<b>Enable All interrupt bit</b> Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	ET2	<b>Timer 2 overflow interrupt Enable bit</b> Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	<b>Serial port Enable bit</b> Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	<b>Timer 1 overflow interrupt Enable bit</b> Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	<b>External interrupt 1 Enable bit</b> Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	<b>Timer 0 overflow interrupt Enable bit</b> Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	<b>External interrupt 0 Enable bit</b> Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0X00 0000b

Bit addressable

## Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirety: the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occurred during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

## Power-down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 10., PCON register).

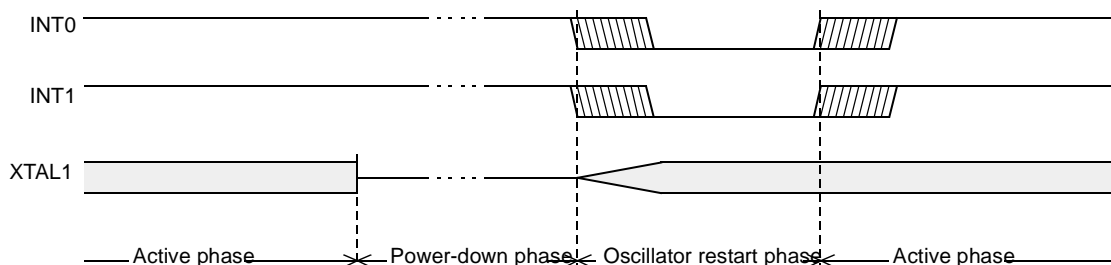
In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated.  $V_{CC}$  can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before  $V_{CC}$  is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts  $\overline{INT0}$  and  $\overline{INT1}$  are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.

Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 10. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.

Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C52X2 into power-down mode.

**Figure 10.** Power-down Exit Waveform



Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does not affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

Note: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

**Table 15.** The State of Ports During Idle and Power-down Modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data <sup>(1)</sup>	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data <sup>(1)</sup>	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

Note: 1. Port 0 can force a "zero" level. A "one" will leave port floating.

## Power-off Flag

The power-off flag allows the user to distinguish between a “cold start” reset and a “warm start” reset.

A cold start reset is the one induced by  $V_{CC}$  switch-on. A warm start reset occurs while  $V_{CC}$  is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 17.). POF is set by hardware when  $V_{CC}$  rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a  $V_{CC}$  range from 4.5V to 5.5V. For lower  $V_{CC}$  value, reading POF bit will return indeterminate value.

**Table 17.** PCON Register  
PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

Bit Number	Bit Mnemonic	Description
7	SMOD1	<b>Serial port Mode bit 1</b> Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	<b>Serial port Mode bit 0</b> Clear to select SM0 bit in SCON register. Set to select FE bit in SCON register.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	POF	<b>Power-off Flag</b> Clear to recognize next reset type. Set by hardware when $V_{CC}$ rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	<b>Power-down mode bit</b> Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	<b>Idle mode bit</b> Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b

Not bit addressable

## EPROM Structure

The TS87C52X2 is divided in two different arrays:

- the code array: 8 Kbytes
- the encryption array: 64 bytes

In addition a third non programmable array is implemented:

- the signature array: 4 bytes

## EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

### Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

### Program Lock Bits

The three lock bits, when programmed according to Table 1., will provide different level of protection for the on-chip code and data.

Program Lock Bits				Protection Description
Security level	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOV C instruction executed from external program memory returns non encrypted data.
2	P	U	U	MOV C instruction executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the EPROM is disabled.
3	U	P	U	Same as 2, also verify is disabled.
4	U	U	P	Same as 3, also external execution is disabled.

U: unprogrammed

P: programmed

**WARNING:** Security level 2 and 3 should only be programmed after EPROM and Core verification.

### Signature Bytes

The TS80/87C52X2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 9.

## EPROM Programming

### Set-up modes

In order to program and verify the EPROM or to read the signature bytes, the TS87C52X2 is placed in specific set-up modes (See Figure 11.).

Control and program signals must be held at the levels indicated in Table 35.

# Definition of terms








**Address Lines:** P1.0-P1.7, P2.0-P2.4 respectively for A0-A12

**Data Lines:** P0.0-P0.7 for D0-D7

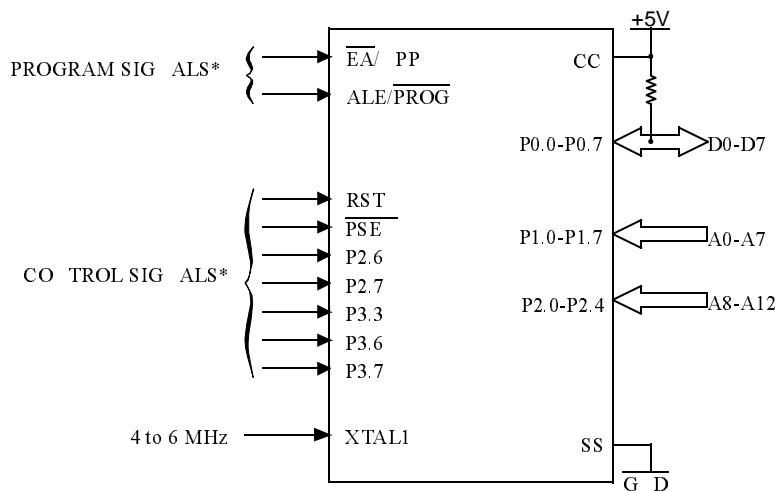
**Control Signals:** RST,  $\overline{\text{PSEN}}$ , P2.6, P2.7, P3.3, P3.6, P3.7.

**Program Signals:** ALE/ $\overline{\text{PROG}}$ ,  $\overline{\text{EA}}$ /VPP.

**Table 20.** EPROM Set-up Modes

Mode	RST	PSEN	ALE/ PROG	$\overline{\text{EA}}$ / VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code data	1	0		12.75V	0	1	1	1	1
Verify Code data	1	0	1	1	0		0	1	1
Program Encryption Array Address 0-3Fh	1	0		12.75V	0	1	1	0	1
Read Signature Bytes	1	0	1	1	0		0	0	0
Program Lock bit 1	1	0		12.75V	1	1	1	1	1
Program Lock bit 2	1	0		12.75V	1	1	1	0	0
Program Lock bit 3	1	0		12.75V	1	0	1	1	0

**Figure 11.** Set-Up Modes Configuration



\* See Table 31. for proper value on these inputs

12,000  $\mu\text{W}/\text{cm}^2$  rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

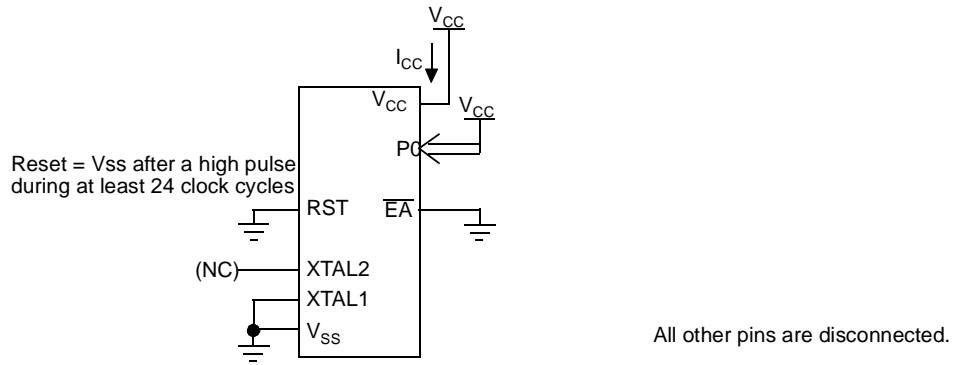
## Signature Bytes

The TS80/87C52X2 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 31. for Read Signature Bytes. Table 35. shows the content of the signature byte for the TS80/87C52X2.

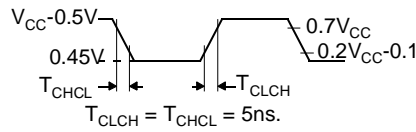
**Table 21.** Signature Bytes Content

Location	Contents	Comment
30h	58h	Manufacturer Code: Atmel
31h	57h	Family Code: C51 X2
60h	2Dh	Product name: TS80C52X2
60h	ADh	Product name: TS87C52X2
60h	20h	Product name: TS80C32X2
61h	FFh	Product revision number

**Figure 16.**  $I_{CC}$  Test Condition, Power-down Mode



**Figure 17.** Clock Signal Waveform for  $I_{CC}$  Tests in Active and Idle Modes



## AC Parameters

### Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example:  $T_{AVLL}$  = Time for Address Valid to ALE Low.

$T_{LLPL}$  = Time for ALE Low to PSEN Low.

$T_A = 0$  to  $+70^{\circ}C$  (commercial temperature range);  $V_{SS} = 0V$ ;  $V_{CC} = 5V \pm 10\%$ ; -M and -V ranges.

$T_A = -40^{\circ}C$  to  $+85^{\circ}C$  (industrial temperature range);  $V_{SS} = 0V$ ;  $V_{CC} = 5V \pm 10\%$ ; -M and -V ranges.

$T_A = 0$  to  $+70^{\circ}C$  (commercial temperature range);  $V_{SS} = 0V$ ;  $2.7V < V_{CC} < 5.5V$ ; -L range.

$T_A = -40^{\circ}C$  to  $+85^{\circ}C$  (industrial temperature range);  $V_{SS} = 0V$ ;  $2.7V < V_{CC} < 5.5V$ ; -L range.

Table 24. gives the maximum applicable load capacitance for Port 0, Port 1, 2 and 3, and ALE and PSEN signals. Timings will be guaranteed if these capacitances are respected. Higher capacitance values can be used, but timings will then be degraded.

**Table 24.** Load Capacitance versus speed range, in pF

	-M	-V	-L
Port 0	100	50	100
Port 1, 2, 3	80	50	80
ALE / PSEN	100	30	100

Table 5., Table 29. and Table 32. give the description of each AC symbols.

Table 27., Table 30. and Table 33. give for each range the AC parameter.





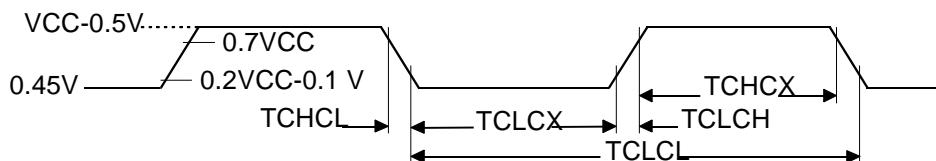
## External Clock Drive Characteristics (XTAL1)

**Table 36.** AC Parameters

Symbol	Parameter	Min	Max	Units
$T_{CLCL}$	Oscillator Period	25		ns
$T_{CHCX}$	High Time	5		ns
$T_{CLCX}$	Low Time	5		ns
$T_{CLCH}$	Rise Time		5	ns
$T_{CHCL}$	Fall Time		5	ns
$T_{CHCX}/T_{CLCX}$	Cyclic ratio in X2 mode	40	60	%

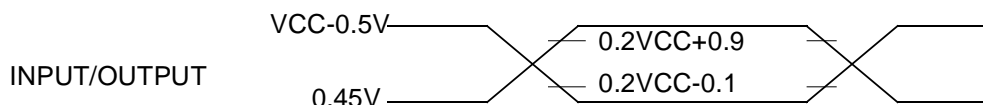
## External Clock Drive Waveforms

**Figure 23.** External Clock Drive Waveforms



## AC Testing Input/Output Waveforms

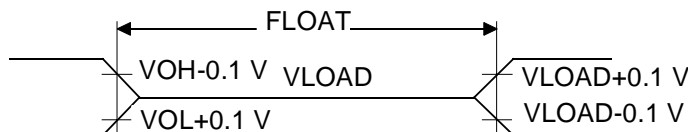
**Figure 24.** AC Testing Input/Output Waveforms



AC inputs during testing are driven at  $V_{CC} - 0.5$  for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at  $V_{IH}$  min for a logic “1” and  $V_{IL}$  max for a logic “0”.

## Float Waveforms

**Figure 25.** Float Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded  $V_{OH}/V_{OL}$  level occurs.  $I_{OL}/I_{OH} \geq \pm 20mA$ .

## Ordering Information

**Table 37. Possible Ordering Entries**

Part Number <sup>(3)</sup>	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
<b>TS80C32X2-MCA</b>	ROMLess	5V $\pm$ 10%	Commercial	40 MHz <sup>(1)</sup>	PDIL40	Stick
<b>TS80C32X2-MCB</b>	ROMLess	5V $\pm$ 10%	Commercial	40 MHz <sup>(1)</sup>	PLCC44	Stick
<b>TS80C32X2-MCC</b>	ROMLess	5V $\pm$ 10%	Commercial	40 MHz <sup>(1)</sup>	PQFP44	Tray
<b>TS80C32X2-MCE</b>	ROMLess	5V $\pm$ 10%	Commercial	40 MHz <sup>(1)</sup>	VQFP44	Tray
<b>TS80C32X2-LCA</b>	ROMLess	2.7 to 5.5V	Commercial	30 MHz <sup>(1)</sup>	PDIL40	Stick
<b>TS80C32X2-LCB</b>	ROMLess	2.7 to 5.5V	Commercial	30 MHz <sup>(1)</sup>	PLCC44	Stick
<b>TS80C32X2-LCC</b>	ROMLess	2.7 to 5.5V	Commercial	30 MHz <sup>(1)</sup>	PQFP44	Tray
<b>TS80C32X2-LCE</b>	ROMLess	2.7 to 5.5V	Commercial	30 MHz <sup>(1)</sup>	VQFP44	Tray
<b>TS80C32X2-VCA</b>	ROMLess	5V $\pm$ 10%	Commercial	60 MHz <sup>(3)</sup>	PDIL40	Stick
<b>TS80C32X2-VCB</b>	ROMLess	5V $\pm$ 10%	Commercial	60 MHz <sup>(3)</sup>	PLCC44	Stick
<b>TS80C32X2-VCC</b>	ROMLess	5V $\pm$ 10%	Commercial	60 MHz <sup>(3)</sup>	PQFP44	Tray
<b>TS80C32X2-VCE</b>	ROMLess	5V $\pm$ 10%	Commercial	60 MHz <sup>(3)</sup>	VQFP44	Tray
<b>TS80C32X2-MIA</b>	ROMLess	5V $\pm$ 10%	Industrial	40 MHz <sup>(1)</sup>	PDIL40	Stick
<b>TS80C32X2-MIB</b>	ROMLess	5V $\pm$ 10%	Industrial	40 MHz <sup>(1)</sup>	PLCC44	Stick
<b>TS80C32X2-MIC</b>	ROMLess	5V $\pm$ 10%	Industrial	40 MHz <sup>(1)</sup>	PQFP44	Tray
<b>TS80C32X2-MIE</b>	ROMLess	5V $\pm$ 10%	Industrial	40 MHz <sup>(1)</sup>	VQFP44	Tray
<b>TS80C32X2-LIA</b>	ROMLess	2.7 to 5.5V	Industrial	30 MHz <sup>(1)</sup>	PDIL40	Stick
<b>TS80C32X2-LIB</b>	ROMLess	2.7 to 5.5V	Industrial	30 MHz <sup>(1)</sup>	PLCC44	Stick
<b>TS80C32X2-LIC</b>	ROMLess	2.7 to 5.5V	Industrial	30 MHz <sup>(1)</sup>	PQFP44	Tray
<b>TS80C32X2-LIE</b>	ROMLess	2.7 to 5.5V	Industrial	30 MHz <sup>(1)</sup>	VQFP44	Tray
<b>TS80C32X2-VIA</b>	ROMLess	5V $\pm$ 10%	Industrial	60 MHz <sup>(3)</sup>	PDIL40	Stick
<b>TS80C32X2-VIB</b>	ROMLess	5V $\pm$ 10%	Industrial	60 MHz <sup>(3)</sup>	PLCC44	Stick
<b>TS80C32X2-VIC</b>	ROMLess	5V $\pm$ 10%	Industrial	60 MHz <sup>(3)</sup>	PQFP44	Tray
<b>TS80C32X2-VIE</b>	ROMLess	5V $\pm$ 10%	Industrial	60 MHz <sup>(3)</sup>	VQFP44	Tray
<b>AT80C32X2-3CSUM</b>	ROMLess	5V $\pm$ 10%	Industrial & Green	40 MHz <sup>(1)</sup>	PDIL40	Stick
<b>AT80C32X2-SLSUM</b>	ROMLess	5V $\pm$ 10%	Industrial & Green	40 MHz <sup>(1)</sup>	PLCC44	Stick
<b>AT80C32X2-RLTUM</b>	ROMLess	5V $\pm$ 10%	Industrial & Green	40 MHz <sup>(1)</sup>	VQFP44	Tray
<b>AT80C32X2-RLTUM</b>	ROMLess	5V $\pm$ 10%	Industrial & Green	40 MHz <sup>(1)</sup>	VQFP44	Tape & Reel
<b>AT80C32X2-3CSUL</b>	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz <sup>(1)</sup>	PDIL40	Stick
<b>AT80C32X2-SLSUL</b>	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz <sup>(1)</sup>	PLCC44	Stick

**Table 37. Possible Ordering Entries (Continued)**

Part Number <sup>(3)</sup>	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT80C32X2-RLTUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz <sup>(1)</sup>	VQFP44	Tray
AT80C32X2-3CSUV	ROMLess	5V ±10%	Industrial & Green	60 MHz <sup>(3)</sup>	PDIL40	Stick
AT80C32X2-SLSUV	ROMLess	5V ±10%	Industrial & Green	60 MHz <sup>(3)</sup>	PLCC44	Stick
AT80C32X2-RLTUV	ROMLess	5V ±10%	Industrial & Green	60 MHz <sup>(3)</sup>	VQFP44	Tray
TS80C52X2zzz-MCA	8K ROM	2.7 to 5.5V	Commercial	40 MHz <sup>(1)</sup>	PDIL40	Stick
TS80C52X2zzz-MCB	8K ROM	2.7 to 5.5V	Commercial	40 MHz <sup>(1)</sup>	PLCC44	Stick
TS80C52X2zzz-MCC	8K ROM	2.7 to 5.5V	Commercial	40 MHz <sup>(1)</sup>	PQFP44	Tray
TS80C52X2zzz-MCE	8K ROM	2.7 to 5.5V	Commercial	40 MHz <sup>(1)</sup>	VQFP44	Tray
TS80C52X2zzz-LCA	8K ROM	2.7 to 5.5V	Commercial	30 MHz <sup>(1)</sup>	PDIL40	Stick
TS80C52X2zzz-LCB	8K ROM	2.7 to 5.5V	Commercial	30 MHz <sup>(1)</sup>	PLCC44	Stick
TS80C52X2zzz-LCC	8K ROM	2.7 to 5.5V	Commercial	30 MHz <sup>(1)</sup>	PQFP44	Tray
TS80C52X2zzz-LCE	8K ROM	2.7 to 5.5V	Commercial	30 MHz <sup>(1)</sup>	VQFP44	Tray
TS80C52X2zzz-VCA	8K ROM	5V ±10%	Commercial	60 MHz <sup>(3)</sup>	PDIL40	Stick
TS80C52X2zzz-VCB	8K ROM	5V ±10%	Commercial	60 MHz <sup>(3)</sup>	PLCC44	Stick
TS80C52X2zzz-VCC	8K ROM	5V ±10%	Commercial	60 MHz <sup>(3)</sup>	PQFP44	Tray
TS80C52X2zzz-VCE	8K ROM	5V ±10%	Commercial	60 MHz <sup>(3)</sup>	VQFP44	Tray
TS80C52X2zzz-MIA	8K ROM	5V ±10%	Industrial	40 MHz <sup>(1)</sup>	PDIL40	Stick
TS80C52X2zzz-MIB	8K ROM	5V ±10%	Industrial	40 MHz <sup>(1)</sup>	PLCC44	Stick
TS80C52X2zzz-MIC	8K ROM	5V ±10%	Industrial	40 MHz <sup>(1)</sup>	PQFP44	Tray
TS80C52X2zzz-MIE	8K ROM	5V ±10%	Industrial	40 MHz <sup>(1)</sup>	VQFP44	Tray
TS80C52X2zzz-LIA	8K ROM	2.7 to 5.5V	Industrial	30 MHz <sup>(1)</sup>	PDIL40	Stick
TS80C52X2zzz-LIB	8K ROM	2.7 to 5.5V	Industrial	30 MHz <sup>(1)</sup>	PLCC44	Stick
TS80C52X2zzz-LIC	8K ROM	2.7 to 5.5V	Industrial	30 MHz <sup>(1)</sup>	PQFP44	Tray
TS80C52X2zzz-LIE	8K ROM	2.7 to 5.5V	Industrial	30 MHz <sup>(1)</sup>	VQFP44	Tray
TS80C52X2zzz-VIA	8K ROM	5V ±10%	Industrial	60 MHz <sup>(3)</sup>	PDIL40	Stick
TS80C52X2zzz-VIB	8K ROM	5V ±10%	Industrial	60 MHz <sup>(3)</sup>	PLCC44	Stick
TS80C52X2zzz-VIC	8K ROM	5V ±10%	Industrial	60 MHz <sup>(3)</sup>	PQFP44	Tray
TS80C52X2zzz-VIE	8K ROM	5V ±10%	Industrial	60 MHz <sup>(3)</sup>	VQFP44	Tray
AT80C52X2zzz-3CSUM	8K ROM	5V ±10%	Industrial & Green	40 MHz <sup>(1)</sup>	PDIL40	Stick
AT80C52X2zzz-SLSUM	8K ROM	5V ±10%	Industrial & Green	40 MHz <sup>(1)</sup>	PLCC44	Stick
AT80C52X2zzz-RLTUM	8K ROM	5V ±10%	Industrial & Green	40 MHz <sup>(1)</sup>	VQFP44	Tray

**Table 37. Possible Ordering Entries (Continued)**

Part Number <sup>(3)</sup>	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
<b>AT87C52X2-3CSUM</b>	8K OTP	5V ±10%	Industrial & Green	40 MHz <sup>(1)</sup>	PDIL40	Stick
<b>AT87C52X2-SLSUM</b>	8K OTP	5V ±10%	Industrial & Green	40 MHz <sup>(1)</sup>	PLCC44	Stick
<b>AT87C52X2-RLTUM</b>	8K OTP	5V ±10%	Industrial & Green	40 MHz <sup>(1)</sup>	VQFP44	Tray
<b>AT87C52X2-3CSUL</b>	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz <sup>(1)</sup>	PDIL40	Stick
<b>AT87C52X2-SLSUL</b>	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz <sup>(1)</sup>	PLCC44	Stick
<b>AT87C52X2-RLTUL</b>	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz <sup>(1)</sup>	VQFP44	Tray
<b>AT87C52X2-3CSUV</b>	8K OTP	5V ±10%	Industrial & Green	60 MHz <sup>(3)</sup>	PDIL40	Stick
<b>AT87C52X2-SLSUV</b>	8K OTP	5V ±10%	Industrial & Green	60 MHz <sup>(3)</sup>	PLCC44	Stick
<b>AT87C52X2-RLTUV</b>	8K OTP	5V ±10%	Industrial & Green	60 MHz <sup>(3)</sup>	VQFP44	Tray

- Notes:
1. 20 MHz in X2 Mode.
  2. Tape and Reel available for SL, PQFP and RL packages
  3. 30 MHz in X2 Mode.