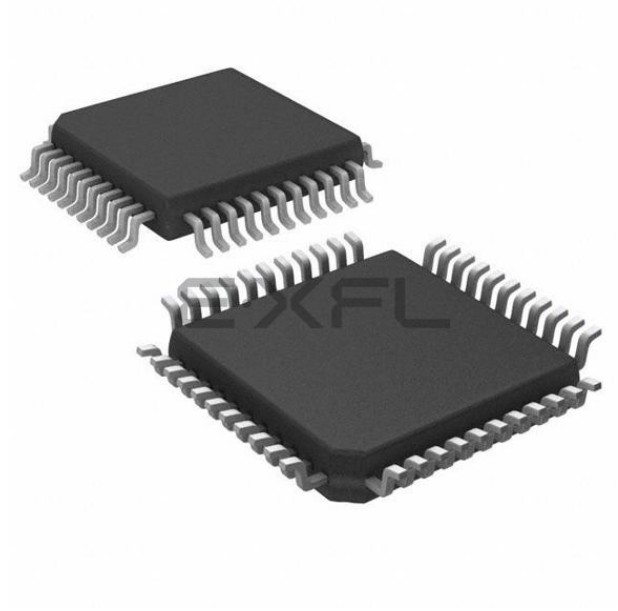

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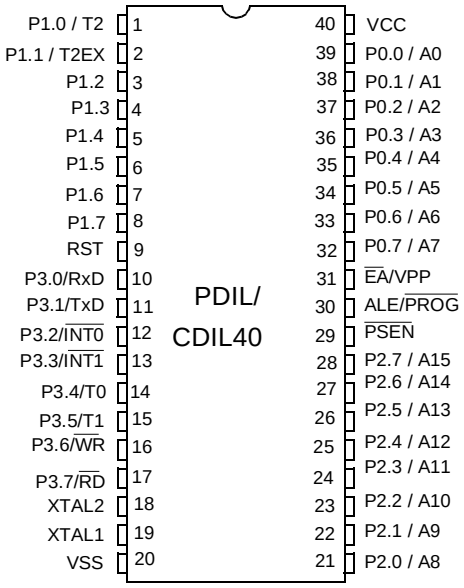
What is "Embedded - Microcontrollers"?

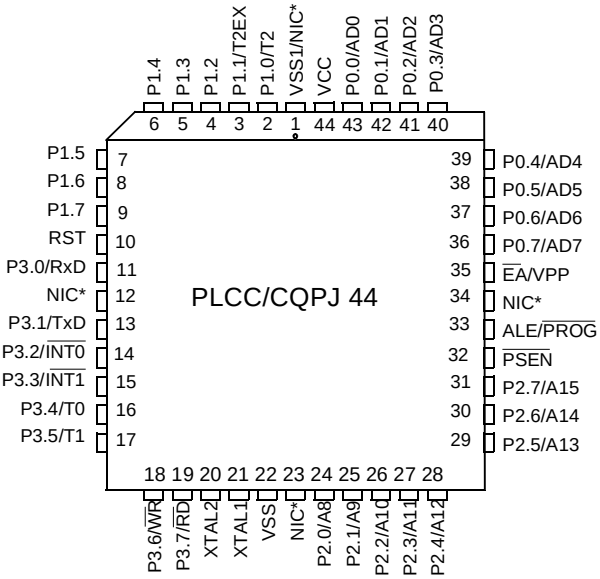
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

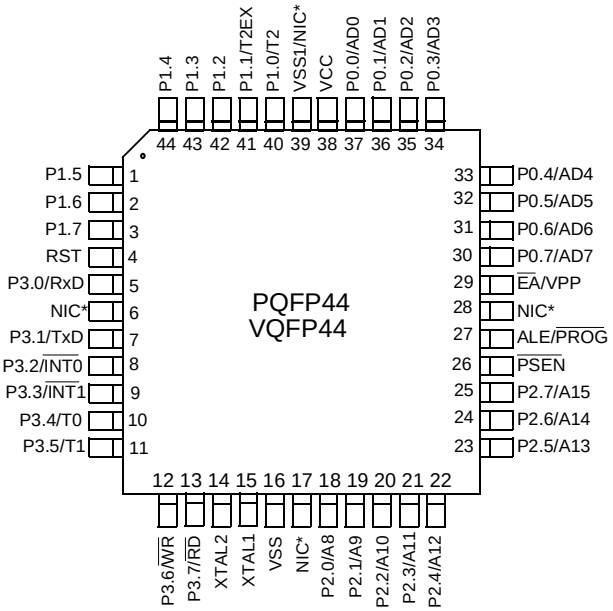
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-PQFP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts80c32x2-lic

Pin Configuration







*NIC: No Internal Connection

Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.

ASSEMBLY LANGUAGE

```
; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2    AUXR1 EQU 0A2H
;
0000 909000MOV DPTR,#SOURCE ; address of SOURCE
0003 05A2 INC AUXR1 ; switch data pointers
0005 90A000 MOV DPTR,#DEST ; address of DEST
0008    LOOP:
0008 05A2 INC AUXR1 ; switch data pointers
000A E0 MOVX A,atDPTR ; get a byte from SOURCE
000B A3 INC DPTR ; increment SOURCE address
000C 05A2 INC AUXR1 ; switch data pointers
000E F0 MOVX atDPTR,A ; write the byte to DEST
000F A3 INC DPTR ; increment DEST address
0010 70F6JNZ LOOP ; check for 0 terminator
0012 05A2 INC AUXR1 ; (optional) restore DPS
```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

Timer 2

The timer 2 in the TS80C52X2 is compatible with the timer 2 in the 80C52.
It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 5) and T2MOD register (See Table 6). Timer 2 operation is similar to Timer 0 and Timer 1. C/$\overline{T2}$ selects $F_{OSC}/12$ (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/$\overline{RL2}$ (T2CON), as described in the Atmel 8-bit Microcontroller Hardware description.

Refer to the Atmel 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C52X2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

Auto-reload Mode

The Auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 4. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.

Table 6. T2MOD Register

T2MOD - Timer 2 Mode Control Register (C9h)

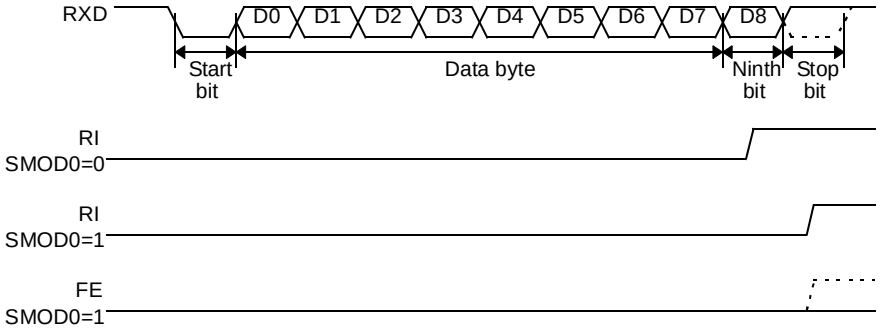
7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	T2OE	**Timer 2 Output Enable bit** Clear to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.
0	DCEN	**Down Counter Enable bit** Clear to disable timer 2 as up/down counter. Set to enable timer 2 as up/down counter.

Reset Value = XXXX XX00b

Not bit addressable

Figure 8. UART Timings in Modes 2 and 3



Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

Note: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be `1111 1111b`.

For example:

```
SADDR0101 0110b
SADEN1111 1100b
Given0101 01XXb
```

The following is an example of how to use given addresses to address different slaves:

```
Slave A:SADDR1111 0001b
    SADEN1111 1010b
    Given1111 0X0Xb


Slave B:SADDR1111 0011b
    SADEN1111 1001b
    Given1111 0XX1b


Slave C:SADDR1111 0010b
    SADEN1111 1101b
    Given1111 00X1b
```

The SADEN byte is selected so that each slave may be addressed separately.

For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g.

Table 9. SCON Register

SCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI

Bit Number	Bit Mnemonic	Description
7	FE	**Framing Error bit (SMOD0=1)** Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit
	SM0	**Serial port Mode bit 0** Refer to SM1 for serial port mode selection. SMOD0 must be cleared to enable access to the SM0 bit
6	SM1	**Serial port Mode bit 1** SM0 SM1 Mode Description Baud Rate 0 0 0 Shift Register F_{XTAL}/12 (/6 in X2 mode) 0 1 1 8-bit UART Variable 1 0 2 9-bit UART F_{XTAL}/64 or F_{XTAL}/32 (/32, /16 in X2 mode) 1 1 3 9-bit UART Variable
5	SM2	**Serial port Mode 2 bit / Multiprocessor Communication Enable bit** Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.
4	REN	**Reception Enable bit** Clear to disable serial reception. Set to enable serial reception.
3	TB8	Transmitter Bit 8 / Ninth bit to transmit in modes 2 and 3. Clear to transmit a logic 0 in the 9th bit. Set to transmit a logic 1 in the 9th bit.
2	RB8	**Receiver Bit 8 / Ninth bit received in modes 2 and 3** Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.
1	TI	**Transmit Interrupt flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.
0	RI	**Receive Interrupt flag** Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 7. and Figure 8. in the other modes.

Reset Value = 0000 0000b

Bit addressable

Table 13. IP Register

IP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	-	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	PT2	**Timer 2 overflow interrupt Priority bit** Refer to PT2H for priority level.
4	PS	**Serial port Priority bit** Refer to PSH for priority level.
3	PT1	**Timer 1 overflow interrupt Priority bit** Refer to PT1H for priority level.
2	PX1	**External interrupt 1 Priority bit** Refer to PX1H for priority level.
1	PT0	**Timer 0 overflow interrupt Priority bit** Refer to PT0H for priority level.
0	PX0	**External interrupt 0 Priority bit** Refer to PX0H for priority level.

Reset Value = XX00 0000b

Bit addressable

Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirely : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occured during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

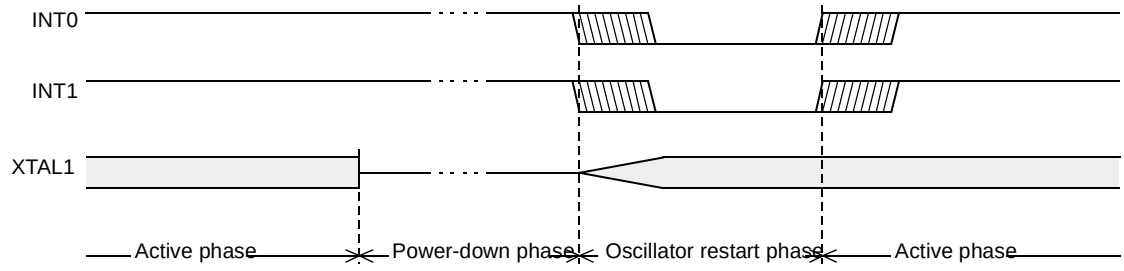
Power-down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 10., PCON register).

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{INT0}$ and $\overline{INT1}$ are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.
Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 10. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.
Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C52X2 into power-down mode.

Figure 10. Power-down Exit Waveform



Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

Note: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

Table 15. The State of Ports During Idle and Power-down Modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data(1)	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data(1)	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

Note: 1. Port 0 can force a "zero" level. A "one" will leave port floating.

Power-off Flag

The power-off flag allows the user to distinguish between a “cold start” reset and a “warm start” reset.

A cold start reset is the one induced by V_{CC} switch-on. A warm start reset occurs while V_{CC} is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 17.). POF is set by hardware when V_{CC} rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a Vcc range from 4.5V to 5.5V. For lower Vcc value, reading POF bit will return indeterminate value.

Table 17. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0** Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-off Flag** Clear to recognize next reset type. Set by hardware when V_{CC} rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b
Not bit addressable

Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS87C52X2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise $\overline{EA}$/VPP from VCC to VPP (typical 12.75V).
- Step 5: Pulse ALE/$\overline{PROG}$ once.
- Step 6: Lower $\overline{EA}$/VPP from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 12.).

Verify Algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C52X2.

P 2.7 is used to enable data output.

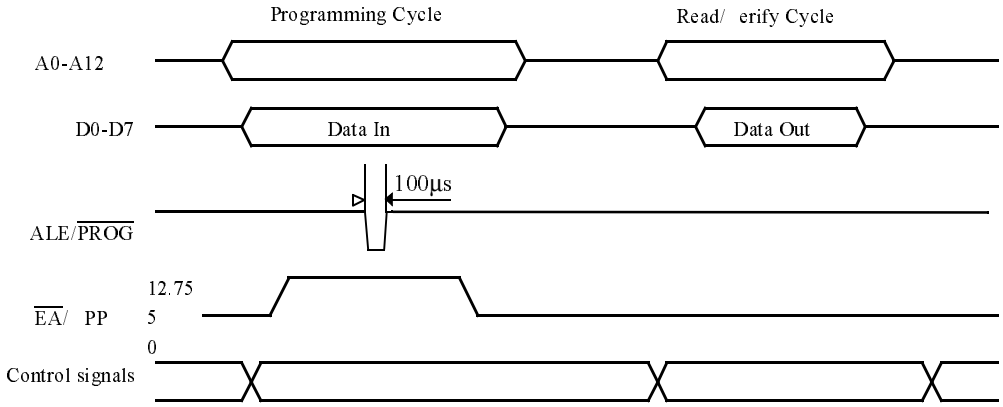
To verify the TS87C52X2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 12.)

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.

Figure 12. Programming and Verification Signal's Waveform



EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of

12,000 µW/cm^2 rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

Signature Bytes

The TS80/87C52X2 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 31. for Read Signature Bytes. Table 35. shows the content of the signature byte for the TS80/87C52X2.

Table 21. Signature Bytes Content

Location	Contents	Comment
30h	58h	Manufacturer Code: Atmel
31h	57h	Family Code: C51 X2
60h	2Dh	Product name: TS80C52X2
60h	ADh	Product name:TS87C52X2
60h	20h	Product name: TS80C32X2
61h	FFh	Product revision number

Electrical Characteristics

Absolute Maximum Ratings[1]

Ambiant Temperature Under Bias:
C = commercial.....0°C to 70°C
I = industrial .....-40°C to 85°C
Storage Temperature ..... -65°C to + 150°C
Voltage on V_{CC} to V_{SS}.....-0.5V to + 7 V
Voltage on V_{PP} to V_{SS} .....-0.5V to + 13 V
Voltage on Any Pin to V_{SS}.....-0.5V to V_{CC} + 0.5V
Power Dissipation ..... 1 W[2]

Notes:
1. Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

Power Consumption Measurement

Since the introduction of the first C51 devices, every manufacturer made operating Icc measurements under reset, which made sense for the designs were the CPU was running under reset. In Atmel new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That's why, while keeping measurements under Reset, Atmel presents a new way to measure the operating Icc:

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = Vcc, RST = Vss, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating Icc.

DC Parameters for Standard Voltage

T_A = 0°C to +70°C; V_{SS} = 0 V; V_{CC} = 5V ± 10%; F = 0 to 40 MHz.
T_A = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 5V ± 10%; F = 0 to 40 MHz.

Table 22. DC Parameters in Standard Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage except XTAL1, RST	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, XTAL1, RST	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage, ports 1, 2, 3 [6]			0.3 0.45 1.0	V V V	I_{OL} = 100 µA[4] I_{OL} = 1.6 mA[4] I_{OL} = 3.5 mA[4]
V_{OL1}	Output Low Voltage, port 0 [6]			0.3 0.45 1.0	V V V	I_{OL} = 200 µA[4] I_{OL} = 3.2 mA[4] I_{OL} = 7.0 mA[4]
V_{OL2}	Output Low Voltage, ALE, $\overline{PSEN}$			0.3 0.45 1.0	V V V	I_{OL} = 100 µA[4] I_{OL} = 1.6 mA[4] I_{OL} = 3.5 mA[4]

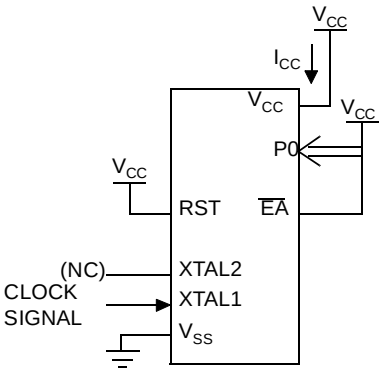
Table 22. DC Parameters in Standard Voltage (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	Output High Voltage, ports 1, 2, 3	V_{CC} - 0.3 V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -10 µA I_{OH} = -30 µA I_{OH} = -60 µA V_{CC} = 5V ± 10%
V_{OH1}	Output High Voltage, port 0	V_{CC} - 0.3 V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA V_{CC} = 5V ± 10%
V_{OH2}	Output High Voltage,ALE, $\overline{PSEN}$	V_{CC} - 0.3 V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -100 µA I_{OH} = -1.6 mA I_{OH} = -3.5 mA V_{CC} = 5V ± 10%
R_{RST}	RST Pulldown Resistor	50	90 (5)	200	kΩ	
I_{IL}	Logical 0 Input Current ports 1, 2 and 3			-50	µA	Vin = 0.45V
I_{LI}	Input Leakage Current			±10	µA	0.45V < Vin < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	µA	Vin = 2.0 V
C_{IO}	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz T_A = 25°C
I_{PD}	Power Down Current		20 (5)	50	µA	2.0 V < V_{CC} < 5.5V(3)
I_{CC} under RESET	Power Supply Current Maximum values, X1 mode: (7)			1 + 0.4 Freq (MHz) at12MHz 5.8 at16MHz 7.4	mA	V_{CC} = 5.5V(1)
I_{CC} operating	Power Supply Current Maximum values, X1 mode: (7)			3 + 0.6 Freq (MHz) at12MHz 10.2 at16MHz 12.6	mA	V_{CC} = 5.5V(8)
I_{CC} idle	Power Supply Current Maximum values, X1 mode: (7)			0.25+0.3 Freq (MHz) at12MHz 3.9 at16MHz 5.1	mA	V_{CC} = 5.5V(2)

Port 0: 26 mA
Ports 1, 2 and 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

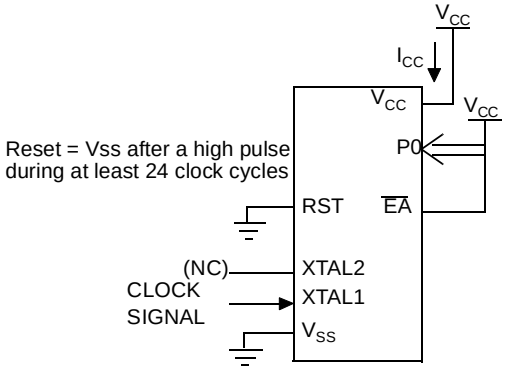
7. For other values, please contact your sales office.
8. Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 17.), V_{IL} = V_{SS} + 0.5V,
V_{IH} = V_{CC} - 0.5V; XTAL2 N.C.; $\overline{EA}$ = Port 0 = V_{CC}; RST = V_{SS}. The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.

Figure 13. I_{CC} Test Condition, under reset



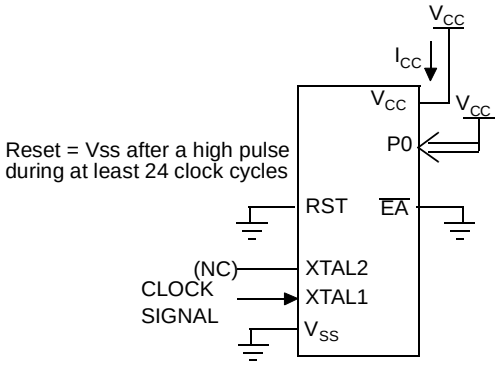
All other pins are disconnected.

Figure 14. Operating I_{CC} Test Condition



All other pins are disconnected.

Figure 15. I_{CC} Test Condition, Idle Mode



All other pins are disconnected.

Table 28., Table 31. and Table 34. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

Table 25. Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20	40	30	30	20
T (ns)	25	50	25	33.3	33.3	50

Example:

T_{LLIV} in X2 mode for a -V part at 20 MHz (T = $1/20^{E6}$ = 50 ns):

x= 22 (Table 28.)

T= 50ns

T_{LLIV}= 2T - x = 2 x 50 - 22 = 78ns

External Program Memory Characteristics

Table 26. Symbol Description

Symbol	Parameter
T	Oscillator clock period
T_{LHLL}	ALE pulse width
T_{AVLL}	Address Valid to ALE
T_{LLAX}	Address Hold After ALE
T_{LLIV}	ALE to Valid Instruction In
T_{LLPL}	ALE to $\overline{PSEN}$
T_{PLPH}	$\overline{PSEN}$ Pulse Width
T_{PLIV}	$\overline{PSEN}$ to Valid Instruction In
T_{PXIX}	Input Instruction Hold After $\overline{PSEN}$
T_{PXIZ}	Input Instruction FloatAfter $\overline{PSEN}$
T_{PXAV}	$\overline{PSEN}$ to Address Valid
T_{AVIV}	Address to Valid Instruction In
T_{PLAZ}	$\overline{PSEN}$ Low to Address Float

Table 30. AC Parameters for a Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
T_{RLRH}	130		85		135		125		175		ns
T_{WLWH}	130		85		135		125		175		ns
T_{RLDV}		100		60		102		95		137	ns
T_{RHDX}	0		0		0		0		0		ns
T_{RHDZ}		30		18		35		25		42	ns
T_{LLDV}		160		98		165		155		222	ns
T_{AVDV}		165		100		175		160		235	ns
T_{LLWL}	50	100	30	70	55	95	45	105	70	130	ns
T_{AVWL}	75		47		80		70		103		ns
T_{QVWX}	10		7		15		5		13		ns
T_{QVWH}	160		107		165		155		213		ns
T_{WHQX}	15		9		17		10		18		ns
T_{RLAZ}		0		0		0		0		0	ns
T_{WHLH}	10	40	7	27	15	35	5	45	13	53	ns

EPROM Programming and Verification Characteristics

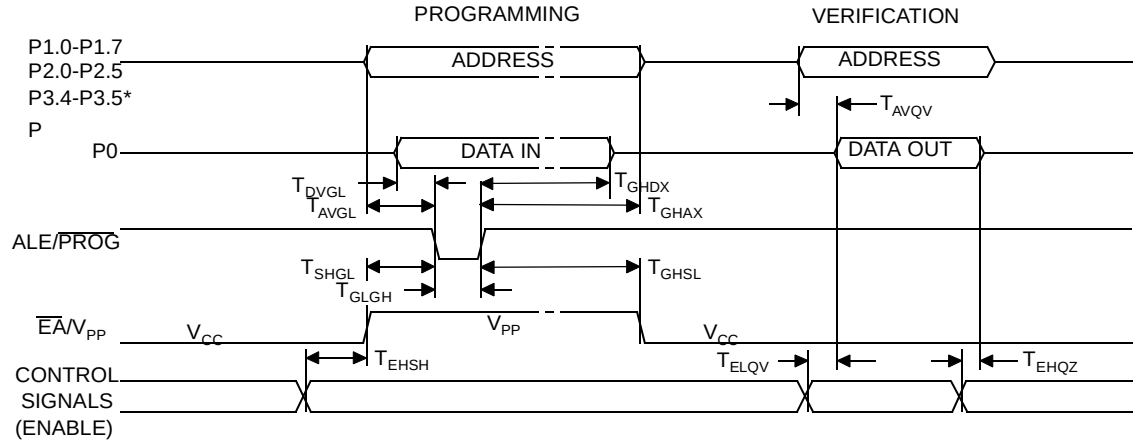
T_A = 21°C to 27°C; V_{SS} = 0V; V_{CC} = 5V ± 10% while programming. V_{CC} = operating range while verifying.

Table 35. EPROM Programming Parameters

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13	V
I_{PP}	Programming Supply Current		75	mA
$1/T_{CLCL}$	Oscillator Frquency	4	6	MHz
T_{AVGL}	Address Setup to $\overline{PROG}$ Low	48 T_{CLCL}		
T_{GHAX}	Adress Hold after $\overline{PROG}$	48 T_{CLCL}		
T_{DVGL}	Data Setup to $\overline{PROG}$ Low	48 T_{CLCL}		
T_{GHDX}	Data Hold after $\overline{PROG}$	48 T_{CLCL}		
T_{EHSH}	(Enable) High to V_{PP}	48 T_{CLCL}		
T_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
T_{GHSL}	V_{PP} Hold after $\overline{PROG}$	10		µs
T_{GLGH}	$\overline{PROG}$ Width	90	110	µs
T_{AVQV}	Address to Valid Data		48 T_{CLCL}	
T_{ELQV}	ENABLE Low to Data Valid		48 T_{CLCL}	
T_{EHQZ}	Data Float after ENABLE	0	48 T_{CLCL}	

EPROM Programming and Verification Waveforms

Figure 22. EPROM Programming and Verification Waveforms



* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

Table 37. Possible Ordering Entries (Continued)

Part Number[3]	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT80C32X2-RLTUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz[1]	VQFP44	Tray
AT80C32X2-3CSUV	ROMLess	5V ±10%	Industrial & Green	60 MHz[3]	PDIL40	Stick
AT80C32X2-SLSUV	ROMLess	5V ±10%	Industrial & Green	60 MHz[3]	PLCC44	Stick
AT80C32X2-RLTUV	ROMLess	5V ±10%	Industrial & Green	60 MHz[3]	VQFP44	Tray
TS80C52X2zzz-MCA	8K ROM	2.7 to 5.5V	Commercial	40 MHz[1]	PDIL40	Stick
TS80C52X2zzz-MCB	8K ROM	2.7 to 5.5V	Commercial	40 MHz[1]	PLCC44	Stick
TS80C52X2zzz-MCC	8K ROM	2.7 to 5.5V	Commercial	40 MHz[1]	PQFP44	Tray
TS80C52X2zzz-MCE	8K ROM	2.7 to 5.5V	Commercial	40 MHz[1]	VQFP44	Tray
TS80C52X2zzz-LCA	8K ROM	2.7 to 5.5V	Commercial	30 MHz[1]	PDIL40	Stick
TS80C52X2zzz-LCB	8K ROM	2.7 to 5.5V	Commercial	30 MHz[1]	PLCC44	Stick
TS80C52X2zzz-LCC	8K ROM	2.7 to 5.5V	Commercial	30 MHz[1]	PQFP44	Tray
TS80C52X2zzz-LCE	8K ROM	2.7 to 5.5V	Commercial	30 MHz[1]	VQFP44	Tray
TS80C52X2zzz-VCA	8K ROM	5V ±10%	Commercial	60 MHz[3]	PDIL40	Stick
TS80C52X2zzz-VCB	8K ROM	5V ±10%	Commercial	60 MHz[3]	PLCC44	Stick
TS80C52X2zzz-VCC	8K ROM	5V ±10%	Commercial	60 MHz[3]	PQFP44	Tray
TS80C52X2zzz-VCE	8K ROM	5V ±10%	Commercial	60 MHz[3]	VQFP44	Tray
TS80C52X2zzz-MIA	8K ROM	5V ±10%	Industrial	40 MHz[1]	PDIL40	Stick
TS80C52X2zzz-MIB	8K ROM	5V ±10%	Industrial	40 MHz[1]	PLCC44	Stick
TS80C52X2zzz-MIC	8K ROM	5V ±10%	Industrial	40 MHz[1]	PQFP44	Tray
TS80C52X2zzz-MIE	8K ROM	5V ±10%	Industrial	40 MHz[1]	VQFP44	Tray
TS80C52X2zzz-LIA	8K ROM	2.7 to 5.5V	Industrial	30 MHz[1]	PDIL40	Stick
TS80C52X2zzz-LIB	8K ROM	2.7 to 5.5V	Industrial	30 MHz[1]	PLCC44	Stick
TS80C52X2zzz-LIC	8K ROM	2.7 to 5.5V	Industrial	30 MHz[1]	PQFP44	Tray
TS80C52X2zzz-LIE	8K ROM	2.7 to 5.5V	Industrial	30 MHz[1]	VQFP44	Tray
TS80C52X2zzz-VIA	8K ROM	5V ±10%	Industrial	60 MHz[3]	PDIL40	Stick
TS80C52X2zzz-VIB	8K ROM	5V ±10%	Industrial	60 MHz[3]	PLCC44	Stick
TS80C52X2zzz-VIC	8K ROM	5V ±10%	Industrial	60 MHz[3]	PQFP44	Tray
TS80C52X2zzz-VIE	8K ROM	5V ±10%	Industrial	60 MHz[3]	VQFP44	Tray
AT80C52X2zzz-3CSUM	8K ROM	5V ±10%	Industrial & Green	40 MHz[1]	PDIL40	Stick
AT80C52X2zzz-SLSUM	8K ROM	5V ±10%	Industrial & Green	40 MHz[1]	PLCC44	Stick
AT80C52X2zzz-RLTUM	8K ROM	5V ±10%	Industrial & Green	40 MHz[1]	VQFP44	Tray

Table 37. Possible Ordering Entries (Continued)

Part Number[3]	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT80C52X2zzz-3CSUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz[1]	PDIL40	Stick
AT80C52X2zzz-SLSUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz[1]	PLCC44	Stick
AT80C52X2zzz-RLTUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz[1]	VQFP44	Tray
AT80C52X2zzz-3CSUV	8K ROM	5V ±10%	Industrial & Green	60 MHz[3]	PDIL40	Stick
AT80C52X2zzz-SLSUV	8K ROM	5V ±10%	Industrial & Green	60 MHz[3]	PLCC44	Stick
AT80C52X2zzz-RLTUV	8K ROM	5V ±10%	Industrial & Green	60 MHz[3]	VQFP44	Tray
TS87C52X2-MCA	8K OTP	5V ±10%	Commercial	40 MHz[1]	PDIL40	Stick
TS87C52X2-MCB	8K OTP	5V ±10%	Commercial	40 MHz[1]	PLCC44	Stick
TS87C52X2-MCC	8K OTP	5V ±10%	Commercial	40 MHz[1]	PQFP44	Tray
TS87C52X2-MCE	8K OTP	5V ±10%	Commercial	40 MHz[1]	VQFP44	Tray
TS87C52X2-LCA	8K OTP	2.7 to 5.5V	Commercial	30 MHz[1]	PDIL40	Stick
TS87C52X2-LCB	8K OTP	2.7 to 5.5V	Commercial	30 MHz[1]	PLC44	Stick
TS87C52X2-LCC	8K OTP	2.7 to 5.5V	Commercial	30 MHz[1]	PQFP44	Tray
TS87C52X2-LCE	8K OTP	2.7 to 5.5V	Commercial	30 MHz[1]	VQFP44	Tray
TS87C52X2-VCA	8K OTP	5V ±10%	Commercial	60 MHz[3]	PDIL40	Stick
TS87C52X2-VCB	8K OTP	5V ±10%	Commercial	60 MHz[3]	PLCC44	Stick
TS87C52X2-VCC	8K OTP	5V ±10%	Commercial	60 MHz[3]	PQFP44	Tray
TS87C52X2-VCE	8K OTP	5V ±10%	Commercial	60 MHz[3]	VQFP44	Tray
TS87C52X2-MIA	8K OTP	5V ±10%	Industrial	40 MHz[1]	PDIL40	Stick
TS87C52X2-MIB	8K OTP	5V ±10%	Industrial	40 MHz[1]	PLCC44	Stick
TS87C52X2-MIC	8K OTP	5V ±10%	Industrial	40 MHz[1]	PQFP44	Tray
TS87C52X2-MIE	8K OTP	5V ±10%	Industrial	40 MHz[1]	VQFP44	Tray
TS87C52X2-LIA	8K OTP	2.7 to 5.5V	Industrial	30 MHz[1]	PDIL40	Stick
TS87C52X2-LIB	8K OTP	2.7 to 5.5V	Industrial	30 MHz[1]	PLCC44	Stick
TS87C52X2-LIC	8K OTP	2.7 to 5.5V	Industrial	30 MHz[1]	PQFP44	Tray
TS87C52X2-LIE	8K OTP	2.7 to 5.5V	Industrial	30 MHz[1]	VQFP44	Tray
TS87C52X2-VIA	8K OTP	5V ±10%	Industrial	60 MHz[3]	PDIL40	Stick
TS87C52X2-VIB	8K OTP	5V ±10%	Industrial	60 MHz[3]	PLCC44	Stick
TS87C52X2-VIC	8K OTP	5V ±10%	Industrial	60 MHz[3]	PQFP44	Tray
TS87C52X2-VIE	8K OTP	5V ±10%	Industrial	60 MHz[3]	VQFP44	Tray