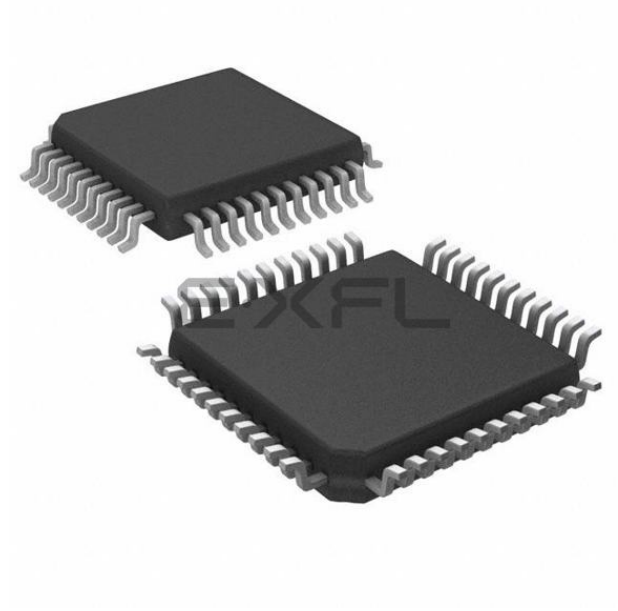

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/20MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-PQFP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts80c32x2-mcc

TS80C52X2 Enhanced Features

In comparison to the original 80C52, the TS80C52X2 implements some new features, which are:

- The X2 option
- The Dual Data Pointer
- The 4 level interrupt priority system
- The power-off flag
- The ONCE mode
- The ALE disabling
- Some enhanced features are also located in the UART and the Timer 2

X2 Feature

The TS80C52X2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

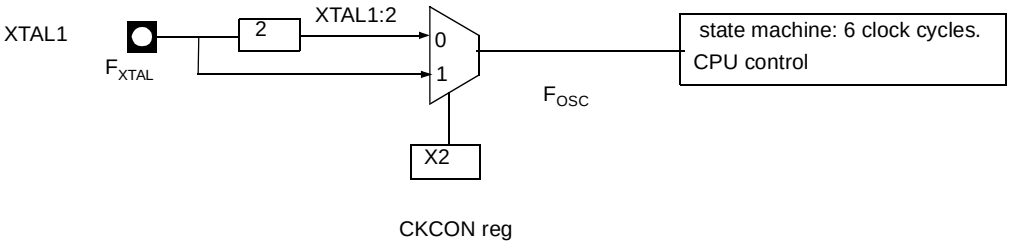
- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power
- Save power consumption while keeping same CPU power (oscillator power saving)
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes
- Increase CPU power by 2 while keeping same crystal frequency

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 1. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 2 shows the mode switching waveforms.

Figure 1. Clock Generation Diagram



Timer 2

The timer 2 in the TS80C52X2 is compatible with the timer 2 in the 80C52.
It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 5) and T2MOD register (See Table 6). Timer 2 operation is similar to Timer 0 and Timer 1. C/$\overline{T2}$ selects $F_{OSC}/12$ (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/$\overline{RL2}$ (T2CON), as described in the Atmel 8-bit Microcontroller Hardware description.

Refer to the Atmel 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C52X2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

Auto-reload Mode

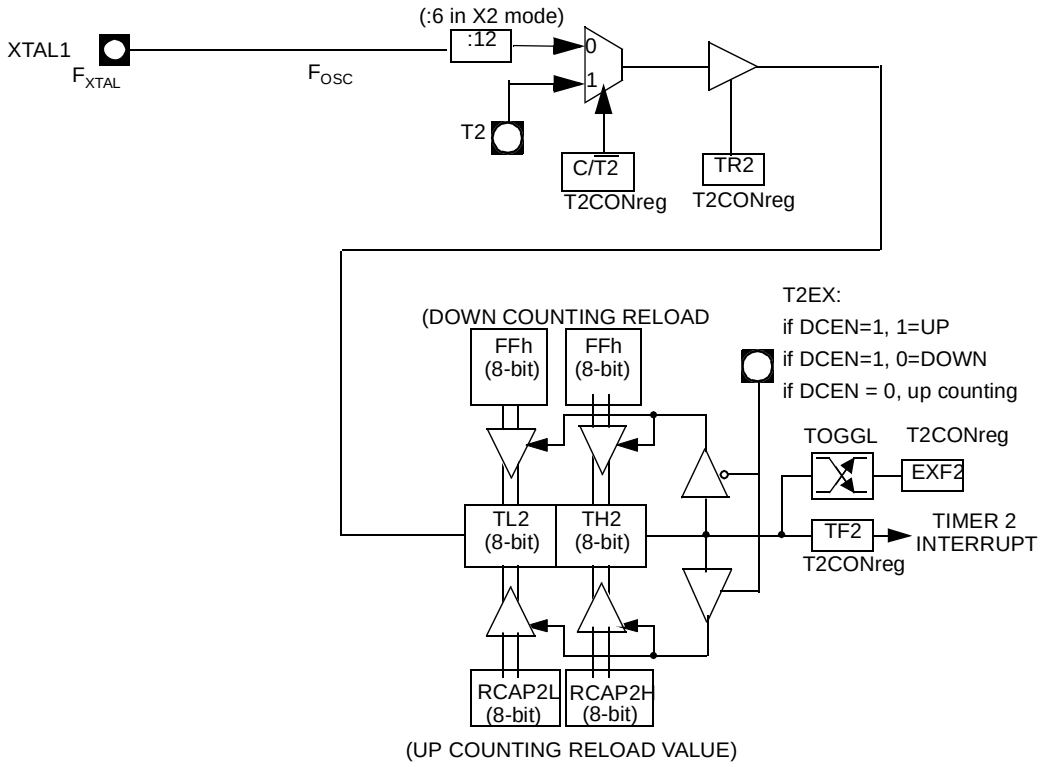
The Auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 4. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.

Figure 4. Auto-reload Mode Up/Down Counter (DCEN = 1)



Programmable Clock-output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 5) . The input clock increments TL2 at frequency $F_{OSC}/2$. The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers :

$$Clock-OutFrequency = \frac{F_{osc}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz ($F_{OSC}/2^{16)}$ to 4 MHz ($F_{OSC}/4$). The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear C/$\overline{T2}$ bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.
- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.

It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.

Table 6. T2MOD Register

T2MOD - Timer 2 Mode Control Register (C9h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	T2OE	**Timer 2 Output Enable bit** Clear to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.
0	DCEN	**Down Counter Enable bit** Clear to disable timer 2 as up/down counter. Set to enable timer 2 as up/down counter.

Reset Value = XXXX XX00b

Not bit addressable

TS80C52X2 Serial I/O Port

The serial I/O port in the TS80C52X2 is compatible with the serial I/O port in the 80C52. It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

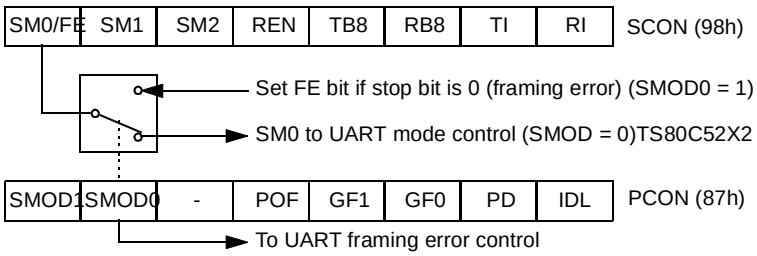
Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 6).

Figure 6. Framing Error Block Diagram



When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 9.) bit is set.
Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 7. and Figure 8.).

Figure 7. UART Timings in Mode 1

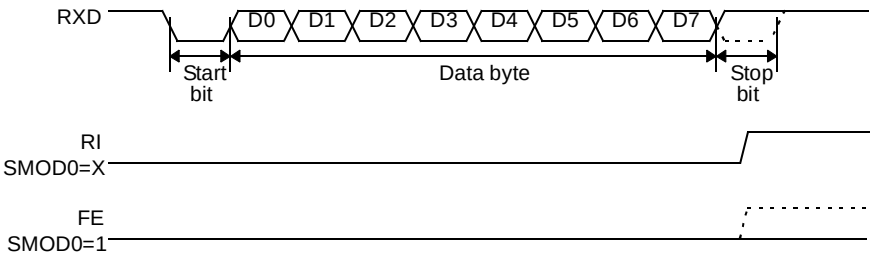
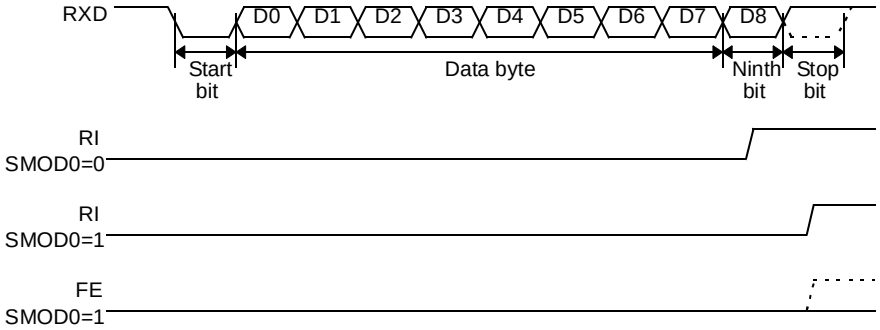


Figure 8. UART Timings in Modes 2 and 3



Automatic Address Recognition

The automatic address recognition feature is enabled when the multiprocessor communication feature is enabled (SM2 bit in SCON register is set).

Implemented in hardware, automatic address recognition enhances the multiprocessor communication feature by allowing the serial port to examine the address of each incoming command frame. Only when the serial port recognizes its own address, the receiver sets RI bit in SCON register to generate an interrupt. This ensures that the CPU is not interrupted by command frames addressed to other devices.

If desired, you may enable the automatic address recognition feature in mode 1. In this configuration, the stop bit takes the place of the ninth data bit. Bit RI is set only when the received command frame address matches the device's address and is terminated by a valid stop bit.

To support automatic address recognition, a device is identified by a given address and a broadcast address.

Note: The multiprocessor communication and automatic address recognition features cannot be enabled in mode 0 (i.e. setting SM2 bit in SCON register in mode 0 has no effect).

Given Address

Each device has an individual address that is specified in SADDR register; the SADEN register is a mask byte that contains don't-care bits (defined by zeros) to form the device's given address. The don't-care bits provide the flexibility to address one or more slaves at a time. The following example illustrates how a given address is formed.

To address a device by its individual address, the SADEN mask byte must be `1111 1111b`.

For example:

```
SADDR0101 0110b
SADEN1111 1100b
Given0101 01XXb
```

The following is an example of how to use given addresses to address different slaves:

```
Slave A:SADDR1111 0001b
    SADEN1111 1010b
    Given1111 0X0Xb


Slave B:SADDR1111 0011b
    SADEN1111 1001b
    Given1111 0XX1b


Slave C:SADDR1111 0010b
    SADEN1111 1101b
    Given1111 00X1b
```

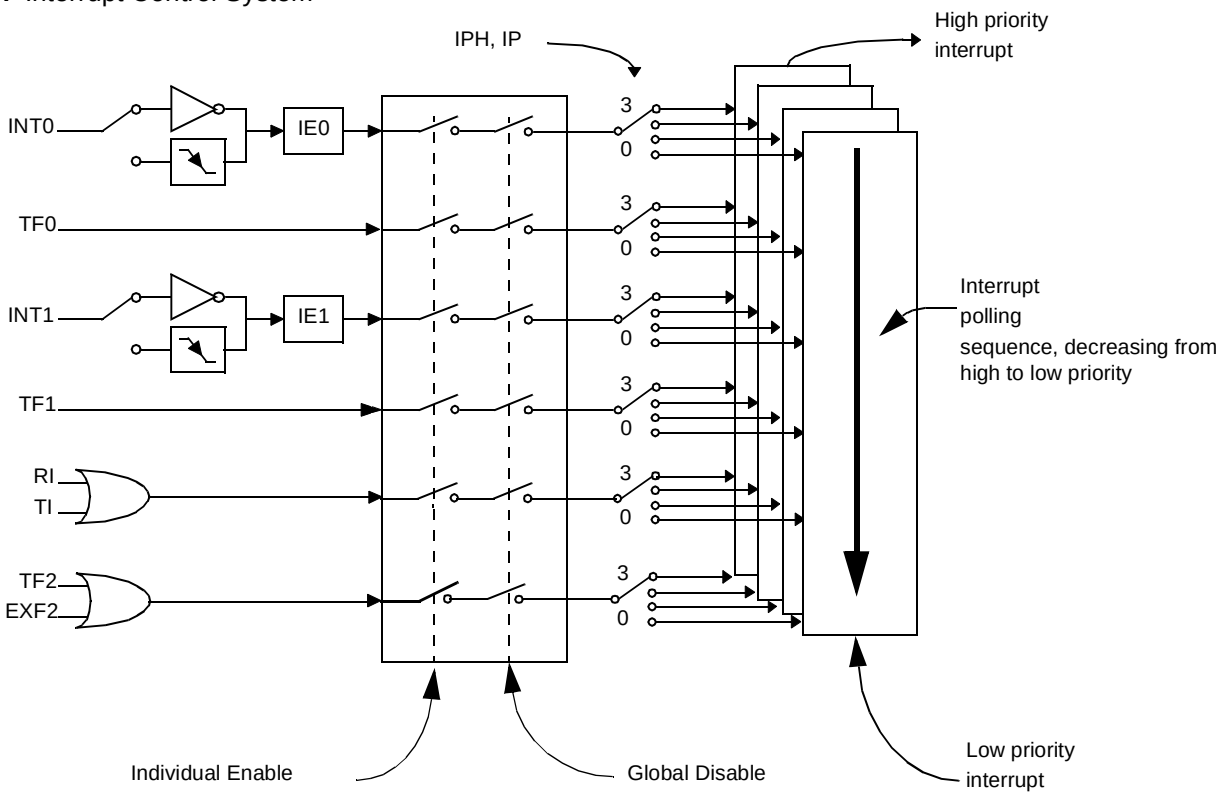
The SADEN byte is selected so that each slave may be addressed separately.

For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g.

Interrupt System

The TS80C52X2 has a total of 6 interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), three timer interrupts (timers 0, 1 and 2) and the serial port interrupt. These interrupts are shown in Figure 9.

Figure 9. Interrupt Control System



Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 12.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 13.) and in the Interrupt Priority High register (See Table 14.). shows the bit values and priority levels associated with each combination.

Table 11. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level

are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Table 12. IE Register

IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	**-**	**ET2**	**ES**	**ET1**	**EX1**	**ET0**	**EX0**

Bit Number	Bit Mnemonic	Description
7	EA	**Enable All interrupt bit** Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	ET2	**Timer 2 overflow interrupt Enable bit** Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	**Serial port Enable bit** Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	**Timer 1 overflow interrupt Enable bit** Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	**External interrupt 1 Enable bit** Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	**Timer 0 overflow interrupt Enable bit** Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	**External interrupt 0 Enable bit** Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0X00 0000b

Bit addressable

Table 14. IPH Register

IPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	PT2H	**Timer 2 overflow interrupt Priority High bit** PT2H PT2 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
4	PSH	**Serial port Priority High bit** PSH PS Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
3	PT1H	**Timer 1 overflow interrupt Priority High bit** PT1H PT1 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
2	PX1H	**External interrupt 1 Priority High bit** PX1H PX1 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
1	PT0H	**Timer 0 overflow interrupt Priority High bit** PT0H PT0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
0	PX0H	**External interrupt 0 Priority High bit** PX0H PX0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest

Reset Value = XX00 0000b

Not bit addressable

Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirely : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occured during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

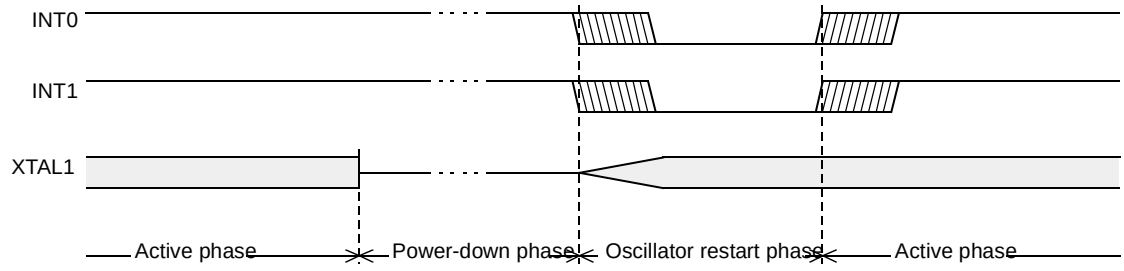
Power-down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 10., PCON register).

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{INT0}$ and $\overline{INT1}$ are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.
Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 10. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.
Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C52X2 into power-down mode.

Figure 10. Power-down Exit Waveform



Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

Note: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

Table 15. The State of Ports During Idle and Power-down Modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data(1)	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data(1)	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

Note: 1. Port 0 can force a "zero" level. A "one" will leave port floating.

Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 18. AUXR Register

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	AO

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	AO	**ALE Output bit** Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = XXXX XXX0b

Not bit addressable

Electrical Characteristics

Absolute Maximum Ratings[1]

Ambiant Temperature Under Bias:
C = commercial.....0°C to 70°C
I = industrial .....-40°C to 85°C
Storage Temperature ..... -65°C to + 150°C
Voltage on V_{CC} to V_{SS}.....-0.5V to + 7 V
Voltage on V_{PP} to V_{SS} .....-0.5V to + 13 V
Voltage on Any Pin to V_{SS}.....-0.5V to V_{CC} + 0.5V
Power Dissipation ..... 1 W[2]

Notes:
1. Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

Power Consumption Measurement

Since the introduction of the first C51 devices, every manufacturer made operating Icc measurements under reset, which made sense for the designs were the CPU was running under reset. In Atmel new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That's why, while keeping measurements under Reset, Atmel presents a new way to measure the operating Icc:

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = Vcc, RST = Vss, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating Icc.

DC Parameters for Standard Voltage

T_A = 0°C to +70°C; V_{SS} = 0 V; V_{CC} = 5V ± 10%; F = 0 to 40 MHz.
T_A = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 5V ± 10%; F = 0 to 40 MHz.

Table 22. DC Parameters in Standard Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage except XTAL1, RST	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, XTAL1, RST	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage, ports 1, 2, 3 [6]			0.3 0.45 1.0	V V V	I_{OL} = 100 µA[4] I_{OL} = 1.6 mA[4] I_{OL} = 3.5 mA[4]
V_{OL1}	Output Low Voltage, port 0 [6]			0.3 0.45 1.0	V V V	I_{OL} = 200 µA[4] I_{OL} = 3.2 mA[4] I_{OL} = 7.0 mA[4]
V_{OL2}	Output Low Voltage, ALE, $\overline{PSEN}$			0.3 0.45 1.0	V V V	I_{OL} = 100 µA[4] I_{OL} = 1.6 mA[4] I_{OL} = 3.5 mA[4]

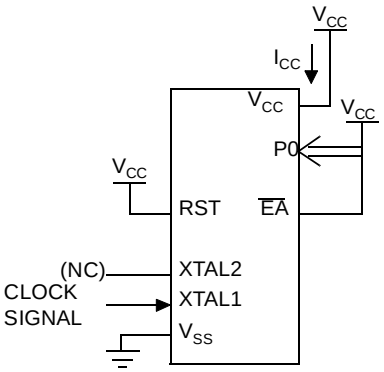
Table 22. DC Parameters in Standard Voltage (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	Output High Voltage, ports 1, 2, 3	V_{CC} - 0.3 V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -10 µA I_{OH} = -30 µA I_{OH} = -60 µA V_{CC} = 5V ± 10%
V_{OH1}	Output High Voltage, port 0	V_{CC} - 0.3 V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA V_{CC} = 5V ± 10%
V_{OH2}	Output High Voltage,ALE, $\overline{PSEN}$	V_{CC} - 0.3 V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -100 µA I_{OH} = -1.6 mA I_{OH} = -3.5 mA V_{CC} = 5V ± 10%
R_{RST}	RST Pulldown Resistor	50	90 (5)	200	kΩ	
I_{IL}	Logical 0 Input Current ports 1, 2 and 3			-50	µA	Vin = 0.45V
I_{LI}	Input Leakage Current			±10	µA	0.45V < Vin < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	µA	Vin = 2.0 V
C_{IO}	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz T_A = 25°C
I_{PD}	Power Down Current		20 (5)	50	µA	2.0 V < V_{CC} < 5.5V(3)
I_{CC} under RESET	Power Supply Current Maximum values, X1 mode: (7)			1 + 0.4 Freq (MHz) at12MHz 5.8 at16MHz 7.4	mA	V_{CC} = 5.5V(1)
I_{CC} operating	Power Supply Current Maximum values, X1 mode: (7)			3 + 0.6 Freq (MHz) at12MHz 10.2 at16MHz 12.6	mA	V_{CC} = 5.5V(8)
I_{CC} idle	Power Supply Current Maximum values, X1 mode: (7)			0.25+0.3 Freq (MHz) at12MHz 3.9 at16MHz 5.1	mA	V_{CC} = 5.5V(2)

Port 0: 26 mA
Ports 1, 2 and 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

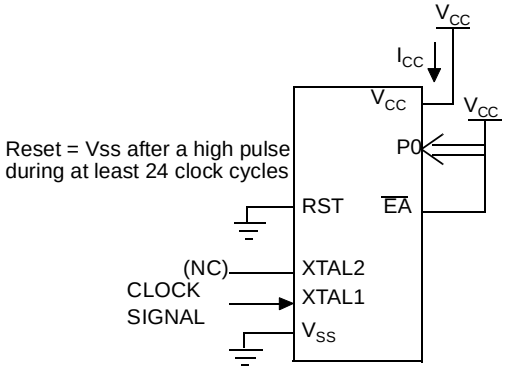
7. For other values, please contact your sales office.
8. Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 17.), V_{IL} = V_{SS} + 0.5V,
V_{IH} = V_{CC} - 0.5V; XTAL2 N.C.; $\overline{EA}$ = Port 0 = V_{CC}; RST = V_{SS}. The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.

Figure 13. I_{CC} Test Condition, under reset



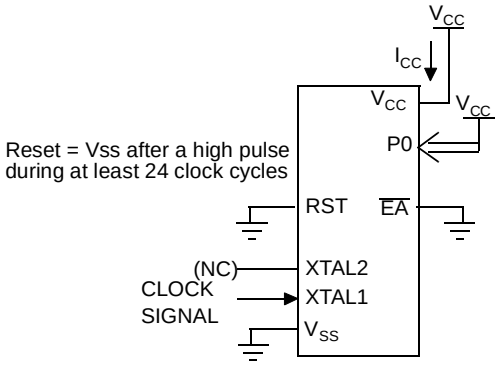
All other pins are disconnected.

Figure 14. Operating I_{CC} Test Condition



All other pins are disconnected.

Figure 15. I_{CC} Test Condition, Idle Mode



All other pins are disconnected.

Table 27. AC Parameters for Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
T	25		33		25		50		33		ns
T_{LHLL}	40		25		42		35		52		ns
T_{AVLL}	10		4		12		5		13		ns
T_{LLAX}	10		4		12		5		13		ns
T_{LLIV}		70		45		78		65		98	ns
T_{LLPL}	15		9		17		10		18		ns
T_{PLPH}	55		35		60		50		75		ns
T_{PLIV}		35		25		50		30		55	ns
T_{PXIX}	0		0		0		0		0		ns
T_{PXIZ}		18		12		20		10		18	ns
T_{AVIV}		85		53		95		80		122	ns
T_{PLAZ}		10		10		10		10		10	ns

Table 28. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{LHLL}	Min	2 T - x	T - x	10	8	15	ns
T_{AVLL}	Min	T - x	0.5 T - x	15	13	20	ns
T_{LLAX}	Min	T - x	0.5 T - x	15	13	20	ns
T_{LLIV}	Max	4 T - x	2 T - x	30	22	35	ns
T_{LLPL}	Min	T - x	0.5 T - x	10	8	15	ns
T_{PLPH}	Min	3 T - x	1.5 T - x	20	15	25	ns
T_{PLIV}	Max	3 T - x	1.5 T - x	40	25	45	ns
T_{PXIX}	Min	x	x	0	0	0	ns
T_{PXIZ}	Max	T - x	0.5 T - x	7	5	15	ns
T_{AVIV}	Max	5 T - x	2.5 T - x	40	30	45	ns
T_{PLAZ}	Max	x	x	10	10	10	ns

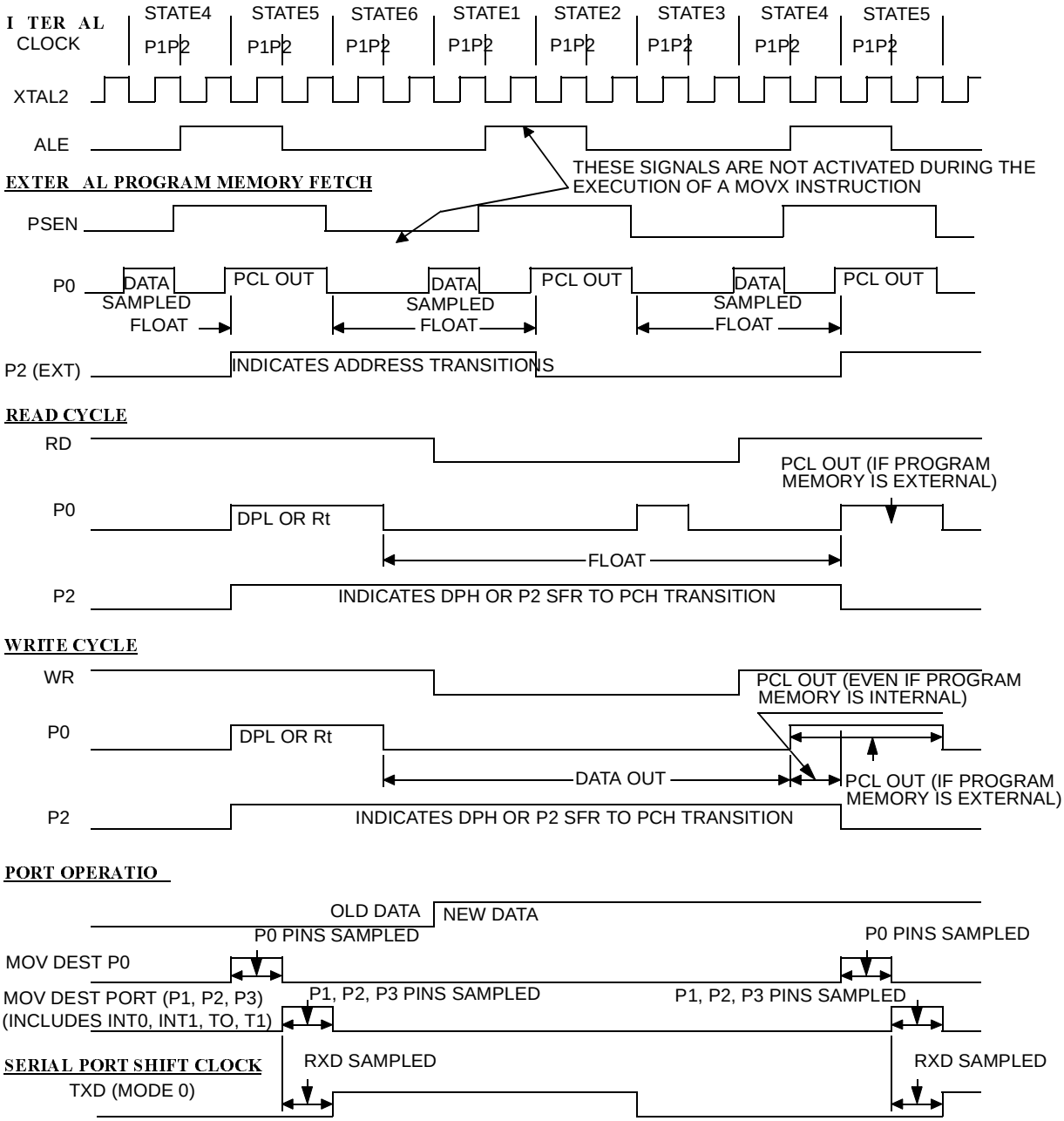
Table 30. AC Parameters for a Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
T_{RLRH}	130		85		135		125		175		ns
T_{WLWH}	130		85		135		125		175		ns
T_{RLDV}		100		60		102		95		137	ns
T_{RHDX}	0		0		0		0		0		ns
T_{RHDZ}		30		18		35		25		42	ns
T_{LLDV}		160		98		165		155		222	ns
T_{AVDV}		165		100		175		160		235	ns
T_{LLWL}	50	100	30	70	55	95	45	105	70	130	ns
T_{AVWL}	75		47		80		70		103		ns
T_{QVWX}	10		7		15		5		13		ns
T_{QVWH}	160		107		165		155		213		ns
T_{WHQX}	15		9		17		10		18		ns
T_{RLAZ}		0		0		0		0		0	ns
T_{WHLH}	10	40	7	27	15	35	5	45	13	53	ns

Clock Waveforms

Valid in normal clock mode. In X2 mode XTAL2 signal must be changed to XTAL2 divided by two.

Figure 26. Clock Waveforms



This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though (T_A = 25°C fully loaded) $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

Table 37. Possible Ordering Entries (Continued)

Part Number[3]	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT80C52X2zzz-3CSUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz[1]	PDIL40	Stick
AT80C52X2zzz-SLSUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz[1]	PLCC44	Stick
AT80C52X2zzz-RLTUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz[1]	VQFP44	Tray
AT80C52X2zzz-3CSUV	8K ROM	5V ±10%	Industrial & Green	60 MHz[3]	PDIL40	Stick
AT80C52X2zzz-SLSUV	8K ROM	5V ±10%	Industrial & Green	60 MHz[3]	PLCC44	Stick
AT80C52X2zzz-RLTUV	8K ROM	5V ±10%	Industrial & Green	60 MHz[3]	VQFP44	Tray
TS87C52X2-MCA	8K OTP	5V ±10%	Commercial	40 MHz[1]	PDIL40	Stick
TS87C52X2-MCB	8K OTP	5V ±10%	Commercial	40 MHz[1]	PLCC44	Stick
TS87C52X2-MCC	8K OTP	5V ±10%	Commercial	40 MHz[1]	PQFP44	Tray
TS87C52X2-MCE	8K OTP	5V ±10%	Commercial	40 MHz[1]	VQFP44	Tray
TS87C52X2-LCA	8K OTP	2.7 to 5.5V	Commercial	30 MHz[1]	PDIL40	Stick
TS87C52X2-LCB	8K OTP	2.7 to 5.5V	Commercial	30 MHz[1]	PLC44	Stick
TS87C52X2-LCC	8K OTP	2.7 to 5.5V	Commercial	30 MHz[1]	PQFP44	Tray
TS87C52X2-LCE	8K OTP	2.7 to 5.5V	Commercial	30 MHz[1]	VQFP44	Tray
TS87C52X2-VCA	8K OTP	5V ±10%	Commercial	60 MHz[3]	PDIL40	Stick
TS87C52X2-VCB	8K OTP	5V ±10%	Commercial	60 MHz[3]	PLCC44	Stick
TS87C52X2-VCC	8K OTP	5V ±10%	Commercial	60 MHz[3]	PQFP44	Tray
TS87C52X2-VCE	8K OTP	5V ±10%	Commercial	60 MHz[3]	VQFP44	Tray
TS87C52X2-MIA	8K OTP	5V ±10%	Industrial	40 MHz[1]	PDIL40	Stick
TS87C52X2-MIB	8K OTP	5V ±10%	Industrial	40 MHz[1]	PLCC44	Stick
TS87C52X2-MIC	8K OTP	5V ±10%	Industrial	40 MHz[1]	PQFP44	Tray
TS87C52X2-MIE	8K OTP	5V ±10%	Industrial	40 MHz[1]	VQFP44	Tray
TS87C52X2-LIA	8K OTP	2.7 to 5.5V	Industrial	30 MHz[1]	PDIL40	Stick
TS87C52X2-LIB	8K OTP	2.7 to 5.5V	Industrial	30 MHz[1]	PLCC44	Stick
TS87C52X2-LIC	8K OTP	2.7 to 5.5V	Industrial	30 MHz[1]	PQFP44	Tray
TS87C52X2-LIE	8K OTP	2.7 to 5.5V	Industrial	30 MHz[1]	VQFP44	Tray
TS87C52X2-VIA	8K OTP	5V ±10%	Industrial	60 MHz[3]	PDIL40	Stick
TS87C52X2-VIB	8K OTP	5V ±10%	Industrial	60 MHz[3]	PLCC44	Stick
TS87C52X2-VIC	8K OTP	5V ±10%	Industrial	60 MHz[3]	PQFP44	Tray
TS87C52X2-VIE	8K OTP	5V ±10%	Industrial	60 MHz[3]	VQFP44	Tray

Table 37. Possible Ordering Entries (Continued)

Part Number[3]	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT87C52X2-3CSUM	8K OTP	5V ±10%	Industrial & Green	40 MHz[1]	PDIL40	Stick
AT87C52X2-SLSUM	8K OTP	5V ±10%	Industrial & Green	40 MHz[1]	PLCC44	Stick
AT87C52X2-RLTUM	8K OTP	5V ±10%	Industrial & Green	40 MHz[1]	VQFP44	Tray
AT87C52X2-3CSUL	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz[1]	PDIL40	Stick
AT87C52X2-SLSUL	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz[1]	PLCC44	Stick
AT87C52X2-RLTUL	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz[1]	VQFP44	Tray
AT87C52X2-3CSUV	8K OTP	5V ±10%	Industrial & Green	60 MHz[3]	PDIL40	Stick
AT87C52X2-SLSUV	8K OTP	5V ±10%	Industrial & Green	60 MHz[3]	PLCC44	Stick
AT87C52X2-RLTUV	8K OTP	5V ±10%	Industrial & Green	60 MHz[3]	VQFP44	Tray

Notes: 1. 20 MHz in X2 Mode.
2. Tape and Reel available for SL, PQFP and RL packages
3. 30 MHz in X2 Mode.