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Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/20MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	-
Program Memory Type	ROMIess
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-PQFP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts80c32x2-mic

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Table 1. Memory Size

	ROM (bytes)	EPROM (bytes)	TOTAL RAM (bytes)
TS80C32X2	0	0	256
TS80C52X2	8k	0	256
TS87C52X2	0	8k	256

Block Diagram



2. Alternate function of Port 3

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TS80C52X2 Enhanced Features

In comparison to the original 80C52, the TS80C52X2 implements some new features, which are:

- The X2 option
- The Dual Data Pointer
- The 4 level interrupt priority system
- The power-off flag
- The ONCE mode
- The ALE disabling
- Some enhanced features are also located in the UART and the Timer 2

X2 Feature The TS80C52X2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power
- Save power consumption while keeping same CPU power (oscillator power saving)
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes
- Increase CPU power by 2 while keeping same crystal frequency

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

DescriptionThe clock for the whole circuit and peripheral is first divided by two before being used by
the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1
input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic
ratio between 40 to 60%. Figure 1. shows the clock generation block diagram. X2 bit is
validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD
mode. Figure 2 shows the mode switching waveforms.

Figure 1. Clock Generation Diagram



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Figure 2. Mode Switching Waveforms

The X2 bit in the CKCON register (See Table 3.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

Note: In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.

Table 3. CKCON Register

CKCON - Clock Control Register (8Fh)

7	6	5	4	3	2	1	0			
-	-	-	-	-	-	-	X2			
Bit Number	Bit Mnemonic	Description	Description							
7	-	Reserved The value rea	Reserved Che value read from this bit is indeterminate. Do not set this bit.							
6	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.							
5	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.							
4	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.							
3	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.							
2	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.							
1	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.							
0	X2	CPU and pe Clear to sele Set to select	CPU and peripheral clock bit Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$). Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$).							

Reset Value = XXXX XXX0b

Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (http://www.atmel.com)





Dual Data Pointer Register (Ddptr)

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called

DPS = AUXR1/bit0 (See Table 5.) that allows the program code to switch between them (Refer to Figure 3).

Figure 3. Use of Dual Pointer



Table 4. AUXR1: Auxiliary Register 1

7	6	5	4	3	2	1	0			
-	-	-	-	GF3	0	-	DPS			
Bit Number	Bit Mnemonic	Descriptior	Description							
7	-	Reserved The value re	Reserved The value read from this bit is indeterminate. Do not set this bit.							
6	-	Reserved The value re	Reserved The value read from this bit is indeterminate. Do not set this bit.							
5	-	Reserved The value re	Reserved The value read from this bit is indeterminate. Do not set this bit.							
4	-	Reserved The value re	Reserved The value read from this bit is indeterminate. Do not set this bit.							
3	GF3	This bit is a	general purpo	ose user flag						
2	0	Reserved Always stud	Reserved Always stuck at 0							
1	-	Reserved The value re	Reserved The value read from this bit is indeterminate. Do not set this bit.							
0	DPS	Data Pointe Clear to sele Set to selec	Data Pointer Selection Clear to select DPTR0. Set to select DPTR1.							

Reset Value = XXXX XXX0 Not bit addressable





Programmable Clock-output

In the clock-out mode, timer 2 operates as a 50%-duty-cycle, programmable clock generator (See Figure 5). The input clock increments TL2 at frequency F_{OSC}/2. The timer repeatedly counts to overflow from a loaded value. At overflow, the contents of RCAP2H and RCAP2L registers are loaded into TH2 and TL2. In this mode, timer 2 overflows do not generate interrupts. The formula gives the clock-out frequency as a function of the system oscillator frequency and the value in the RCAP2H and RCAP2L registers :

$$Clock - OutFrequency = \frac{F_{osc}}{4 \times (65536 - RCAP2H/RCAP2L)}$$

For a 16 MHz system clock, timer 2 has a programmable frequency range of 61 Hz $(F_{OSC}/2^{16})$ to 4 MHz $(F_{OSC}/4)$. The generated clock signal is brought out to T2 pin (P1.0).

Timer 2 is programmed for the clock-out mode as follows:

- Set T2OE bit in T2MOD register.
- Clear C/T2 bit in T2CON register.
- Determine the 16-bit reload value from the formula and enter it in RCAP2H/RCAP2L registers.
- Enter a 16-bit initial value in timer registers TH2/TL2. It can be the same as the reload value or a different one depending on the application.
- To start the timer, set TR2 run control bit in T2CON register.

It is possible to use timer 2 as a baud rate generator and a clock generator simultaneously. For this configuration, the baud rates and clock frequencies are not independent since both functions use the values in the RCAP2H and RCAP2L registers.







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Table 9.SCON RegisterSCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0	
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI	
Bit Number	Bit Mnemonic	Description						
7	FE	Framing Error Clear to reset Set by hardwa SMOD0 must	Framing Error bit (SMOD0=1) Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit					
	SM0	Serial port Mo Refer to SM1 f SMOD0 must	ode bit 0 for serial port be cleared to	mode selecti enable acce	on. ss to the SM0 b	it		
6	SM1						n X2 mode)	
5	SM2	Serial port Mode 2 bit / Multiprocessor Communication Enable bit Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.						
4	REN	Reception En Clear to disabl Set to enable s	able bit e serial recep serial receptic	otion. on.				
3	TB8	Transmitter Bit Clear to transr Set to transmit	: 8 / Ninth bit t nit a logic 0 in : a logic 1 in tł	to transmit in 1 the 9th bit. 1 he 9th bit.	modes 2 and 3			
2	RB8	Receiver Bit 8 / Ninth bit received in modes 2 and 3 Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.						
1	TI	Transmit Interrupt flag Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.						
0	RI	Receive Intern Clear to ackno Set by hardwa 8. in the other	Receive Interrupt flag Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0, see Figure 7. and Figure 8. in the other modes.					

Reset Value = 0000 0000b Bit addressable



Interrupt System

The TS80C52X2 has a total of 6 interrupt vectors: two external interrupts (INT0 and INT1), three timer interrupts (timers 0, 1 and 2) and the serial port interrupt. These interrupts are shown in Figure 9.

Figure 9. Interrupt Control System



Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 12.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 13.) and in the Interrupt Priority High register (See Table 14.). shows the bit values and priority levels associated with each combination.

Table 11. Priority Level Bit Values	

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level

	®
Idle mode	An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirely : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.
	There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.
	The flag bits GF0 and GF1 can be used to give an indication if an interrupt occured dur- ing normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.
	The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.
Power-down Mode	To save maximum power, a power-down mode can be invoked by software (Refer to Table 10., PCON register).
	In power-down mode, the oscillator is stopped and the instruction that invoked power- down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power- down. To properly terminate power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.
	Only external interrupts INTO and INT1 are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input. Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 10. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.
	Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C52X2 into power-down mode.
Figure 10. Power-down Exit Wa	aveform

MEI



Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

Note: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data ⁽¹⁾	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data Address		Port Data
Power Down	Internal	0	0	Port Data ⁽¹⁾	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data Port Dat		Port Data

Table 15. The State of Ports During Idle and Power-down Modes

Note: 1. Port 0 can force a "zero" level. A "one" will leave port floating.





Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 18. AUXR Register

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0			
-	-	-	-	-	-	-	AO			
Bit Number	Bit Mnemonic	Description	Description							
7	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.							
6	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.							
5	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.							
4	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.							
3	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.							
2	-	Reserved The value read from this bit is indeterminate. Do not set this bit.								
1	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.							
0	AO	ALE Output Clear to resto Set to disable	ALE Output bit Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.							

Reset Value = XXXX XXX0b Not bit addressable 12,000 μ W/cm² rating for 30 minutes, at a distance of about 25 mm, should be sufficient. An exposure of 1 hour is recommended with most of standard erasers.

Erasure of the EPROM begins to occur when the chip is exposed to light with wavelength shorter than approximately 4,000 Å. Since sunlight and fluorescent lighting have wavelengths in this range, exposure to these light sources over an extended time (about 1 week in sunlight, or 3 years in room-level fluorescent lighting) could cause inadvertent erasure. If an application subjects the device to this type of exposure, it is suggested that an opaque label be placed over the window.

Signature Bytes The TS80/87C52X2 has four signature bytes in location 30h, 31h, 60h and 61h. To read these bytes follow the procedure for EPROM verify but activate the control lines provided in Table 31. for Read Signature Bytes. Table 35. shows the content of the signature byte for the TS80/87C52X2.

Location	Contents	Comment
30h	58h	Manufacturer Code: Atmel
31h	57h	Family Code: C51 X2
60h	2Dh	Product name: TS80C52X2
60h	ADh	Product name:TS87C52X2
60h	20h	Product name: TS80C32X2
61h	FFh	Product revision number

Table 21. Signature Bytes Content





Table 23. DC Parameters for Low Voltage

Symbol	Parameter	Min	Тур	Мах	Unit	Test Conditions
V _{IL}	Input Low Voltage	-0.5		0.2 V _{CC} - 0.1	V	
V _{IH}	Input High Voltage except XTAL1, RST	0.2 V _{CC} + 0.9		V _{CC} + 0.5	V	
V _{IH1}	Input High Voltage, XTAL1, RST	0.7 V _{CC}		V _{CC} + 0.5	V	
V _{OL}	Output Low Voltage, ports 1, 2, 3 ⁽⁶⁾			0.45	V	I _{OL} = 0.8 mA ⁽⁴⁾
V _{OL1}	Output Low Voltage, port 0, ALE, PSEN (6)			0.45	V	I _{OL} = 1.6 mA ⁽⁴⁾
V _{OH}	Output High Voltage, ports 1, 2, 3	0.9 V _{CC}			V	I _{OH} = -10 μA
V _{OH1}	Output High Voltage, port 0, ALE, PSEN	0.9 V _{CC}			V	I _{OH} = -40 μA
I _{IL}	Logical 0 Input Current ports 1, 2 and 3			-50	μΑ	Vin = 0.45V
I _{LI}	Input Leakage Current			±10	μΑ	$0.45V < Vin < V_{CC}$
I _{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	μΑ	Vin = 2.0 V
R _{RST}	RST Pulldown Resistor	50	90 (5)	200	kΩ	
CIO	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz TA = 25°C
I _{PD}	Power Down Current		20 ⁽⁵⁾ 10 ⁽⁵⁾	50 30	μA	$V_{CC} = 2.0 \text{ V to } 5.5 \text{V}^{(3)}$ $V_{CC} = 2.0 \text{ V to } 3.3 \text{ V}^{(3)}$
I _{CC} under RESET	Power Supply Current Maximum values, X1 mode: (7)			1 + 0.2 Freq (MHz) at12MHz 3.4 at16MHz 4.2	mA	$V_{CC} = 3.3 V^{(1)}$
I _{CC} operating	Power Supply Current Maximum values, X1 mode: ⁽⁷⁾			1 + 0.3 Freq (MHz) at12MHz 4.6 at16MHz 5.8	mA	$V_{CC} = 3.3 V^{(8)}$
I _{CC} idle	Power Supply Current Maximum values, X1 mode: (7)			0.15 Freq (MHz) + 0.2 at12MHz 2 at16MHz 2.6	mA	V _{CC} = 3.3 V ⁽²⁾

Notes: 1. I_{CC} under reset is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 17.), V_{IL} = V_{SS} + 0.5V,

 $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; $\overline{EA} = RST = Port 0 = V_{CC}$. I_{CC} would be slightly higher if a crystal oscillator used...

2. Idle I_{CC} is measured with all out<u>put</u> pins disconnected; XTAL1 driven with T_{CLCH} , $T_{CHCL} = 5$ ns, $V_{IL} = V_{SS} + 0.5V$, $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C; Port 0 = V_{CC} ; EA = RST = V_{SS} (see Figure 15.).

Power Down I_{CC} is measured with all output pins disconnected; EA = V_{SS}, PORT 0 = V_{CC}; XTAL2 NC.; RST = V_{SS} (see Figure 16.).

4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi V_{OL} peak 0.6V. A Schmitt Trigger use is not necessary.

5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.

 Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows: Maximum I_{OL} per port pin: 10 mA Maximum I_{OL} per 8-bit port:

TS8xCx2X2

Port 0: 26 mA Ports 1, 2 and 3: 15 mA Maximum total I_{OL} for all output pins: 71 mA If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

- 7. For other values, please contact your sales office.
- Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 17.), V_{IL} = V_{SS} + 0.5V,

 $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; $\overline{EA} = Port 0 = V_{CC}$; RST = V_{SS} . The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.

Figure 13. I_{CC} Test Condition, under reset



All other pins are disconnected.





All other pins are disconnected.

Figure 15. I_{CC} Test Condition, Idle Mode



All other pins are disconnected.





Figure 16. I_{CC} Test Condition, Power-down Mode



All other pins are disconnected.

Figure 17. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes



AC Parameters

Explanation of the AC Symbols	Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.							
	Example:T _{AVLL} = Time for Addr <u>ess Va</u> lid to ALE Low. T _{LLPL} = Time for ALE Low to PSEN Low.							
	TA = 0 to +70°C (commercial temperature range); $V_{SS} = 0 \text{ V}$; $V_{CC} = 5\text{V} \pm 10\%$; -M and -V ranges. TA = -40°C to +85°C (industrial temperature range); $V_{SS} = 0 \text{ V}$; $V_{CC} = 5\text{V} \pm 10\%$; -M and -V ranges. TA = 0 to +70°C (commercial temperature range); $V_{SS} = 0 \text{ V}$; 2.7 V < $V_{CC} < 5.5\text{V}$; -L range. TA = -40°C to +85°C (industrial temperature range); $V_{SS} = 0 \text{ V}$; 2.7 V < $V_{CC} < 5.5\text{V}$; -L range.							
	Table 24. giv and ALE and respected. Hi Table 24. Los	e <u>s the m</u> aximum applica I PSEN signals. Timing gher capacitance values ad Capacitance versus s	ble load capacitance for s will be guaranteed if can be used, but timings peed range, in pF	r Port 0, Port 1, 2 and 3, these capacitances are will then be degraded.				
		-M	-V	-L				
	Port 0	100	50	100				
	Port 1, 2, 3	80	50	80				
	ALE / PSEN	ALE / PSEN 100 30 100						

Table 5., Table 29. and Table 32. give the description of each AC symbols.

Table 27., Table 30. and Table 33. give for each range the AC parameter.

Table 28., Table 31. and Table 34. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

Table 25. Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20	40	30	30	20
T (ns)	25	50	25	33.3	33.3	50

Example:

 T_{LLIV} in X2 mode for a -V part at 20 MHz (T = 1/20^{E6} = 50 ns):

```
x= 22 (Table 28.)
```

T= 50ns

T_{LLIV}= 2T - x = 2 x 50 - 22 = 78ns

External Program Memory Characteristics

Table 26. Symbol Description

Symbol	Parameter
Т	Oscillator clock period
T _{LHLL}	ALE pulse width
T _{AVLL}	Address Valid to ALE
T _{LLAX}	Address Hold After ALE
T _{LLIV}	ALE to Valid Instruction In
T _{LLPL}	ALE to PSEN
T _{PLPH}	PSEN Pulse Width
T _{PLIV}	PSEN to Valid Instruction In
T _{PXIX}	Input Instruction Hold After PSEN
T _{PXIZ}	Input Instruction FloatAfter PSEN
T _{PXAV}	PSEN to Address Valid
T _{AVIV}	Address to Valid Instruction In
T _{PLAZ}	PSEN Low to Address Float





Table 30.	AC Parameters	for a	Fix	Clock
-----------	---------------	-------	-----	-------

Speed	-1 40 M	M MHz	 X2 n 30 M 60 M equ	V node MHz MHz uiv.	'- stan mod Mi	V dard le 40 Hz	- X2 n 20 f 40 f equ	L node MHz MHz uiv.	- stan mo 30 N	L dard ode MHz	Units
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T _{RLRH}	130		85		135		125		175		ns
T _{WLWH}	130		85		135		125		175		ns
T _{RLDV}		100		60		102		95		137	ns
T _{RHDX}	0		0		0		0		0		ns
T _{RHDZ}		30		18		35		25		42	ns
T _{LLDV}		160		98		165		155		222	ns
T _{AVDV}		165		100		175		160		235	ns
T _{LLWL}	50	100	30	70	55	95	45	105	70	130	ns
T _{AVWL}	75		47		80		70		103		ns
T _{QVWX}	10		7		15		5		13		ns
T _{QVWH}	160		107		165		155		213		ns
T _{WHQX}	15		9		17		10		18		ns
T _{RLAZ}		0		0		0		0		0	ns
T _{WHLH}	10	40	7	27	15	35	5	45	13	53	ns

Symbol	Туре	Standard Clock	X2 Clock	-М	-V	-L	Units
T _{XLXL}	Min	12 T	6 T				ns
T _{QVHX}	Min	10 T - x	5 T - x	50	50	50	ns
T _{XHQX}	Min	2 T - x	T - x	20	20	20	ns
T _{XHDX}	Min	х	х	0	0	0	ns
T _{XHDV}	Max	10 T - x	5 T- x	133	133	133	ns

Table 34. AC Parameters for a Variable Clock: Derating Formula

Shift Register Timing Waveforms







Table 37. Possible Ordering Entries (Continued)

	. 0	. \ /				
Part Number ⁽³⁾	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT80C52X2zzz-3CSUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PDIL40	Stick
AT80C52X2zzz-SLSUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PLCC44	Stick
AT80C52X2zzz-RLTUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	VQFP44	Tray
AT80C52X2zzz-3CSUV	8K ROM	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	PDIL40	Stick
AT80C52X2zzz-SLSUV	8K ROM	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	PLCC44	Stick
AT80C52X2zzz-RLTUV	8K ROM	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	VQFP44	Tray
TS87C52X2-MCA	8K OTP	5V ±10%	Commercial	40 MHz ⁽¹⁾	PDIL40	Stick
TS87C52X2-MCB	8K OTP	5V ±10%	Commercial	40 MHz ⁽¹⁾	PLCC44	Stick
TS87C52X2-MCC	8K OTP	5V ±10%	Commercial	40 MHz ⁽¹⁾	PQFP44	Tray
TS87C52X2-MCE	8K OTP	5V ±10%	Commercial	40 MHz ⁽¹⁾	VQFP44	Tray
TS87C52X2-LCA	8K OTP	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PDIL40	Stick
TS87C52X2-LCB	8K OTP	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PLC44	Stick
TS87C52X2-LCC	8K OTP	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PQFP44	Tray
TS87C52X2-LCE	8K OTP	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	VQFP44	Tray
TS87C52X2-VCA	8K OTP	5V ±10%	Commercial	60 MHz ⁽³⁾	PDIL40	Stick
TS87C52X2-VCB	8K OTP	5V ±10%	Commercial	60 MHz ⁽³⁾	PLCC44	Stick
TS87C52X2-VCC	8K OTP	5V ±10%	Commercial	60 MHz ⁽³⁾	PQFP44	Tray
TS87C52X2-VCE	8K OTP	5V ±10%	Commercial	60 MHz ⁽³⁾	VQFP44	Tray
TS87C52X2-MIA	8K OTP	5V ±10%	Industrial	40 MHz ⁽¹⁾	PDIL40	Stick
TS87C52X2-MIB	8K OTP	5V ±10%	Industrial	40 MHz ⁽¹⁾	PLCC44	Stick
TS87C52X2-MIC	8K OTP	5V ±10%	Industrial	40 MHz ⁽¹⁾	PQFP44	Tray
TS87C52X2-MIE	8K OTP	5V ±10%	Industrial	40 MHz ⁽¹⁾	VQFP44	Tray
TS87C52X2-LIA	8K OTP	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PDIL40	Stick
TS87C52X2-LIB	8K OTP	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PLCC44	Stick
TS87C52X2-LIC	8K OTP	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PQFP44	Tray
TS87C52X2-LIE	8K OTP	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	VQFP44	Tray
TS87C52X2-VIA	8K OTP	5V ±10%	Industrial	60 MHz ⁽³⁾	PDIL40	Stick
TS87C52X2-VIB	8K OTP	5V ±10%	Industrial	60 MHz ⁽³⁾	PLCC44	Stick
TS87C52X2-VIC	8K OTP	5V ±10%	Industrial	60 MHz ⁽³⁾	PQFP44	Тгау
TS87C52X2-VIE	8K OTP	5V ±10%	Industrial	60 MHz ⁽³⁾	VQFP44	Тгау





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