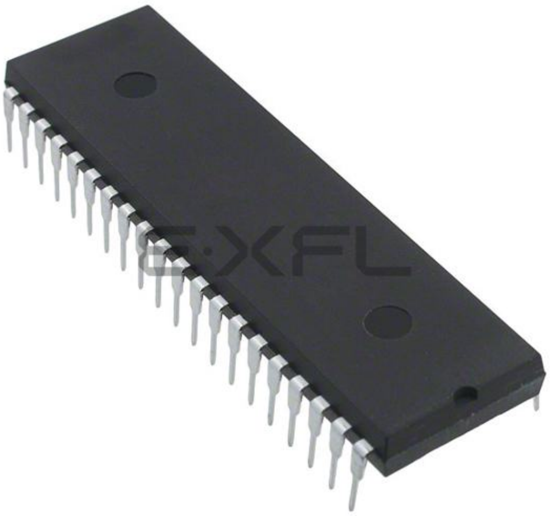


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

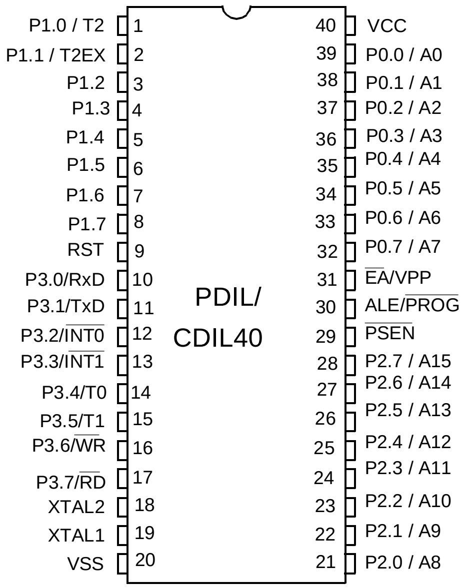
Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c52x2-lca

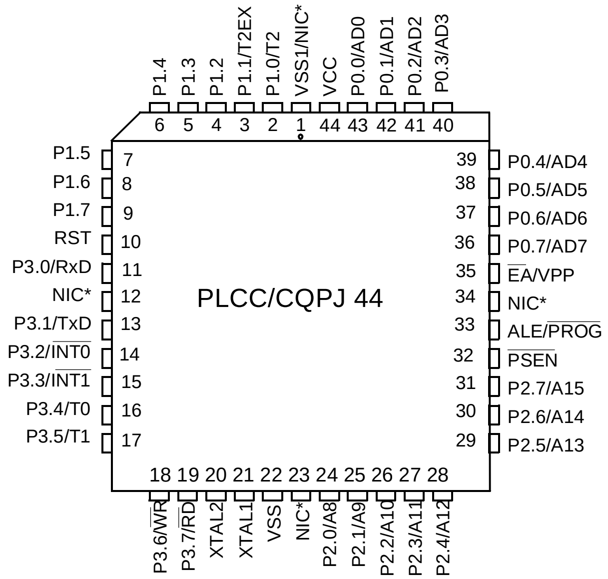
SFR Mapping

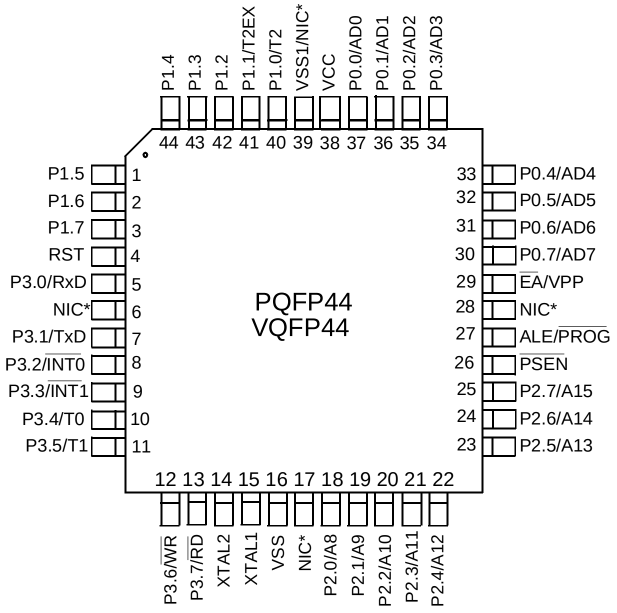
The Special Function Registers (SFRs) of the TS80C52X2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- Interrupt system registers: IE, IP, IPH
- Others: AUXR, CKCON

Pin Configuration







*NIC: No Internal Connection

Mnemonic	Pin Number			Type	Name and Function
	DIL	LCC	VQFP 1.4		
	13	15	9	I	**$\overline{\text{INT1}}$ (P3.3):** External interrupt 1
	14	16	10	I	**T0 (P3.4):** Timer 0 external input
	15	17	11	I	**T1 (P3.5):** Timer 1 external input
	16	18	12	O	**$\overline{\text{WR}}$ (P3.6):** External data memory write strobe
	17	19	13	O	**$\overline{\text{RD}}$ (P3.7):** External data memory read strobe
Reset	9	10	4	I	**Reset:** A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to $V_{CC.}$
ALE/$\overline{\text{PROG}}$	30	33	27	O (I)	**Address Latch Enable/Program Pulse:** Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during EPROM programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
PSEN	29	32	26	O	**Program Store ENable:** The read strobe to external program memory. When executing code from the external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory. $\overline{\text{PSEN}}$ is not activated during fetches from internal program memory.
$\overline{\text{EA}}$/V_{PP}	31	35	29	I	**External Access Enable/Programming Supply Voltage:** $\overline{\text{EA}}$ must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH (RB) or 7FFFH (RC), or FFFFH (RD). If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (RB) or 7FFFH (RC) $\overline{\text{EA}}$ must be held low for ROMless devices. This pin also receives the 12.75V programming supply voltage (V_{PP}) during EPROM programming. If security level 1 is programmed, $\overline{\text{EA}}$ will be internally latched on Reset.
XTAL1	19	21	15	I	**Crystal 1:** Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	O	**Crystal 2:** Output from the inverting oscillator amplifier

TS80C52X2 Enhanced Features

In comparison to the original 80C52, the TS80C52X2 implements some new features, which are**:**

- The X2 option
- The Dual Data Pointer
- The 4 level interrupt priority system
- The power-off flag
- The ONCE mode
- The ALE disabling
- Some enhanced features are also located in the UART and the Timer 2

X2 Feature

The TS80C52X2 core needs only 6 clock periods per machine cycle. This feature called ”X2” provides the following advantages:

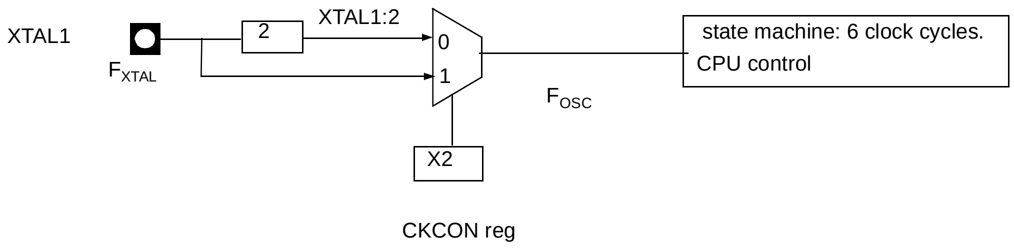
- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power
- Save power consumption while keeping same CPU power (oscillator power saving)
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes
- Increase CPU power by 2 while keeping same crystal frequency

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 1. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 2 shows the mode switching waveforms.

Figure 1. Clock Generation Diagram



Dual Data Pointer Register (Ddptr)

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called
DPS = AUXR1/bit0 (See Table 5.) that allows the program code to switch between them (Refer to Figure 3).

Figure 3. Use of Dual Pointer

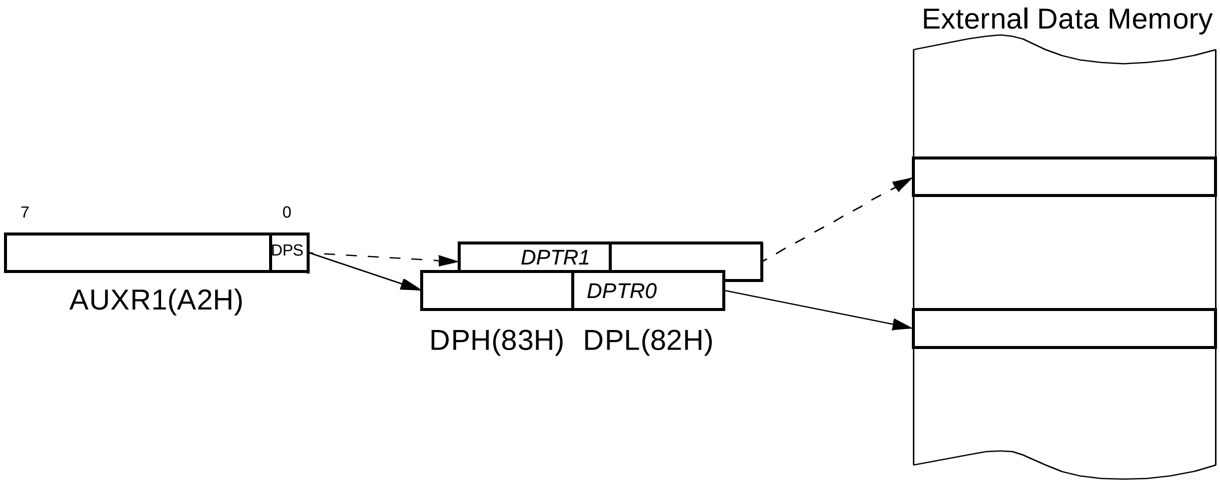


Table 4. AUXR1: Auxiliary Register 1

7	6	5	4	3	2	1	0
-	**-**	**-**	**-**	**GF3**	**0**	**-**	**DPS**

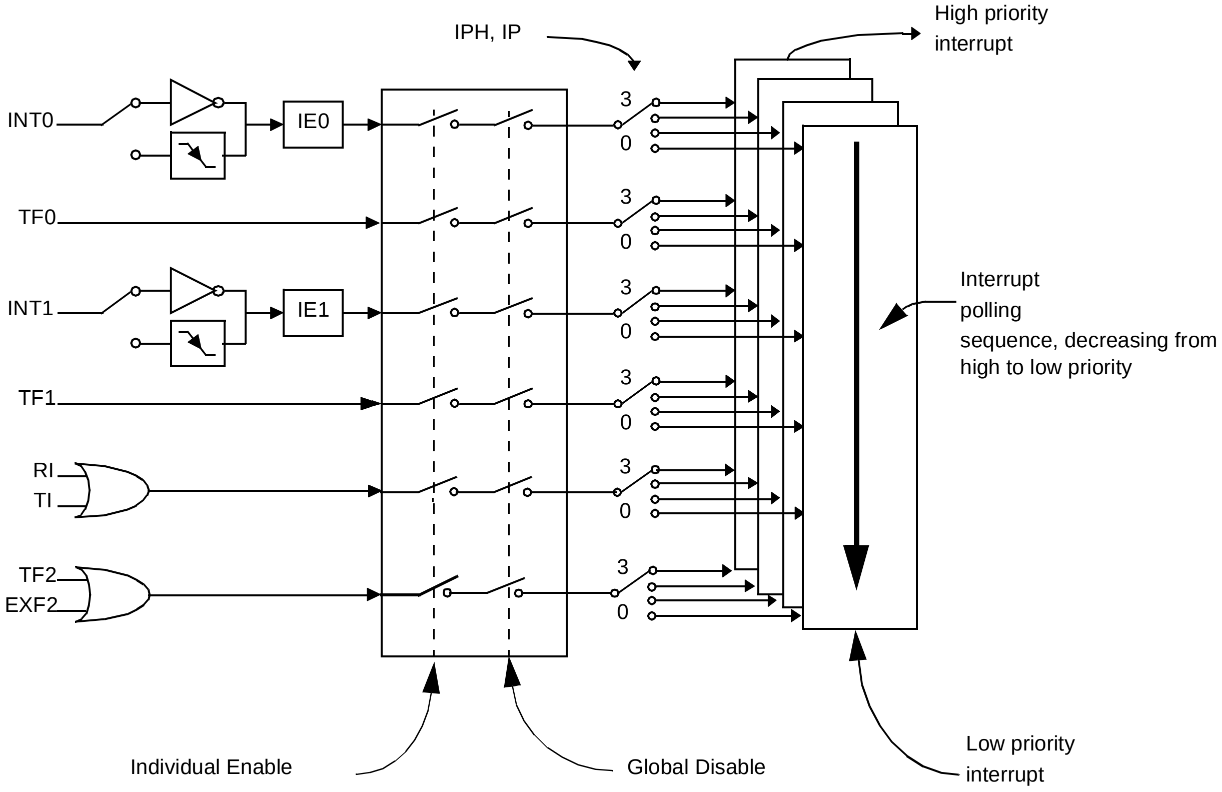
Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	GF3	This bit is a general purpose user flag
2	0	**Reserved** Always stuck at 0
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	DPS	**Data Pointer Selection** Clear to select DPTR0. Set to select DPTR1.

Reset Value = XXXX XXX0
Not bit addressable

Interrupt System

The TS80C52X2 has a total of 6 interrupt vectors: two external interrupts ($\overline{\text{INT0}}$ and $\overline{\text{INT1}}$), three timer interrupts (timers 0, 1 and 2) and the serial port interrupt. These interrupts are shown in Figure 9.

Figure 9. Interrupt Control System



Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 12.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 13.) and in the Interrupt Priority High register (See Table 14.). shows the bit values and priority levels associated with each combination.

Table 11. Priority Level Bit Values

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Table 12. IE Register
IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	-	ET2	ES	ET1	EX1	ET0	EX0

Bit Number	Bit Mnemonic	Description
7	EA	**Enable All interrupt bit** Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	ET2	**Timer 2 overflow interrupt Enable bit** Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	**Serial port Enable bit** Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	**Timer 1 overflow interrupt Enable bit** Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	**External interrupt 1 Enable bit** Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	**Timer 0 overflow interrupt Enable bit** Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	**External interrupt 0 Enable bit** Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0X00 0000b
Bit addressable

Table 14. IPH Register
IPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	PT2H	**Timer 2 overflow interrupt Priority High bit** PT2H PT2 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
4	PSH	**Serial port Priority High bit** PSH PS Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
3	PT1H	**Timer 1 overflow interrupt Priority High bit** PT1H PT1 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
2	PX1H	**External interrupt 1 Priority High bit** PX1H PX1 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
1	PT0H	**Timer 0 overflow interrupt Priority High bit** PT0H PT0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest
0	PX0H	**External interrupt 0 Priority High bit** PX0H PX0 Priority Level 0 0 Lowest 0 1 1 0 1 1 Highest

Reset Value = XX00 0000b
Not bit addressable

Power-off Flag

The power-off flag allows the user to distinguish between a “cold start” reset and a “warm start” reset.

A cold start reset is the one induced by V_{CC} switch-on. A warm start reset occurs while V_{CC} is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 17.). POF is set by hardware when V_{CC} rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a Vcc range from 4.5V to 5.5V. For lower Vcc value, reading POF bit will return indeterminate value.

Table 17. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0** Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-off Flag** Clear to recognize next reset type. Set by hardware when V_{CC} rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b
Not bit addressable

TS80C52X2

ROM Structure

The TS80C52X2 ROM memory is divided in three different arrays:

- the code array:8 Kbytes.
- the encryption array:64 bytes.
- the signature array:4 bytes.

ROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

Encryption Array

Within the ROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

Program Lock Bits

The lock bits when programmed according to Table 19. will provide different level of protection for the on-chip code and data.

Table 19. Program Lock bits

Program Lock Bits				
Security level	LB1	LB2	LB3	Protection Description
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	P	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset.

U: unprogrammed
P: programmed

Signature bytes

The TS80C52X2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 9.

Verify Algorithm

Refer to Section "Verify Algorithm".

Electrical Characteristics

Absolute Maximum Ratings(1)

Ambiant Temperature Under Bias:
C = commercial..0°C to 70°C
I = industrial ....-40°C to 85°C
Storage Temperature .... -65°C to + 150°C
Voltage on V_{CC} to V_{SS} ....-0.5V to + 7 V
Voltage on V_{PP} to V_{SS} ....-0.5V to + 13 V
Voltage on Any Pin to V_{SS}..........................-0.5V to V_{CC} + 0.5V
Power Dissipation .... 1 W(2)

Notes:
1. Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

Power Consumption Measurement

Since the introduction of the first C51 devices, every manufacturer made operating Icc measurements under reset, which made sense for the designs were the CPU was running under reset. In Atmel new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That's why, while keeping measurements under Reset, Atmel presents a new way to measure the operating Icc:

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = Vcc, RST = Vss, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating Icc.

DC Parameters for Standard Voltage

TA = 0°C to +70°C; V_{SS} = 0 V; V_{CC} = 5V ± 10%; F = 0 to 40 MHz.
TA = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 5V ± 10%; F = 0 to 40 MHz.

Table 22. DC Parameters in Standard Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage except XTAL1, RST	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, XTAL1, RST	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage, ports 1, 2, 3 (6)			0.3 0.45 1.0	V V V	I_{OL} = 100 μA(4) I_{OL} = 1.6 mA(4) I_{OL} = 3.5 mA(4)
V_{OL1}	Output Low Voltage, port 0 (6)			0.3 0.45 1.0	V V V	I_{OL} = 200 μA(4) I_{OL} = 3.2 mA(4) I_{OL} = 7.0 mA(4)
V_{OL2}	Output Low Voltage, ALE, $\overline{PSEN}$			0.3 0.45 1.0	V V V	I_{OL} = 100 μA(4) I_{OL} = 1.6 mA(4) I_{OL} = 3.5 mA(4)

Table 22. DC Parameters in Standard Voltage (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	Output High Voltage, ports 1, 2, 3	V_{CC} - 0.3 V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -10 µA I_{OH} = -30 µA I_{OH} = -60 µA V_{CC} = 5V ± 10%
V_{OH1}	Output High Voltage, port 0	V_{CC} - 0.3 V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -200 µA I_{OH} = -3.2 mA I_{OH} = -7.0 mA V_{CC} = 5V ± 10%
V_{OH2}	Output High Voltage,ALE, $\overline{\text{PSEN}}$	V_{CC} - 0.3 V_{CC} - 0.7 V_{CC} - 1.5			V V V	I_{OH} = -100 µA I_{OH} = -1.6 mA I_{OH} = -3.5 mA V_{CC} = 5V ± 10%
R_{RST}	RST Pulldown Resistor	50	90 (5)	200	kΩ	
I_{IL}	Logical 0 Input Current ports 1, 2 and 3			-50	µA	Vin = 0.45V
I_{LI}	Input Leakage Current			±10	µA	0.45V < Vin < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	µA	Vin = 2.0 V
C_{IO}	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz T_A = 25°C
I_{PD}	Power Down Current		20 (5)	50	µA	2.0 V < $V_{CC <}$ 5.5V(3)
I_{CC} under RESET	Power Supply Current Maximum values, X1 mode: (7)			1 + 0.4 Freq (MHz) at12MHz 5.8 at16MHz 7.4	mA	V_{CC} = 5.5V(1)
I_{CC} operating	Power Supply Current Maximum values, X1 mode: (7)			3 + 0.6 Freq (MHz) at12MHz 10.2 at16MHz 12.6	mA	V_{CC} = 5.5V(8)
I_{CC} idle	Power Supply Current Maximum values, X1 mode: (7)			0.25+0.3 Freq (MHz) at12MHz 3.9 at16MHz 5.1	mA	V_{CC} = 5.5V(2)

DC Parameters for Low Voltage

T_A = 0°C to +70°C; V_{SS} = 0 V; V_{CC} = 2.7 V to 5.5V ; F = 0 to 30 MHz.
T_A = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 2.7 V to 5.5V ; F = 0 to 30 MHz.

Table 23. DC Parameters for Low Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage except XTAL1, RST	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, XTAL1, RST	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage, ports 1, 2, 3 (6)			0.45	V	I_{OL} = 0.8 mA(4)
V_{OL1}	Output Low Voltage, port 0, ALE, $\overline{\text{PSEN}}$ (6)			0.45	V	I_{OL} = 1.6 mA(4)
V_{OH}	Output High Voltage, ports 1, 2, 3	0.9 V_{CC}			V	I_{OH} = -10 µA
V_{OH1}	Output High Voltage, port 0, ALE, $\overline{\text{PSEN}}$	0.9 V_{CC}			V	I_{OH} = -40 µA
I_{IL}	Logical 0 Input Current ports 1, 2 and 3			-50	µA	Vin = 0.45V
I_{LI}	Input Leakage Current			±10	µA	0.45V < Vin < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	µA	Vin = 2.0 V
R_{RST}	RST Pulldown Resistor	50	90 (5)	200	kΩ	
CIO	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz T_A = 25°C
I_{PD}	Power Down Current		20 (5) 10 (5)	50 30	µA	V_{CC} = 2.0 V to 5.5V(3) V_{CC} = 2.0 V to 3.3 V(3)
I_{CC} under RESET	Power Supply Current Maximum values, X1 mode: (7)			1 + 0.2 Freq (MHz) at12MHz 3.4 at16MHz 4.2	mA	V_{CC} = 3.3 V(1)
I_{CC} operating	Power Supply Current Maximum values, X1 mode: (7)			1 + 0.3 Freq (MHz) at12MHz 4.6 at16MHz 5.8	mA	V_{CC} = 3.3 V(8)
I_{CC} idle	Power Supply Current Maximum values, X1 mode: (7)			0.15 Freq (MHz) + 0.2 at12MHz 2 at16MHz 2.6	mA	V_{CC} = 3.3 V(2)

Notes:

1. I_{CC} under reset is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 17.), V_{IL} = V_{SS} + 0.5V,
   V_{IH} = V_{CC} - 0.5V; XTAL2 N.C.; $\overline{\text{EA}}$ = RST = Port 0 = V_{CC}. I_{CC} would be slightly higher if a crystal oscillator used..
2. Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5V, V_{IH} = V_{CC} - 0.5V; XTAL2 N.C; Port 0 = V_{CC}; $\overline{\text{EA}}$ = RST = V_{SS} (see Figure 15.).
3. Power Down I_{CC} is measured with all output pins disconnected; $\overline{\text{EA}}$ = V_{SS}, PORT 0 = V_{CC}; XTAL2 NC.; RST = V_{SS} (see Figure 16.).
4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi V_{OL} peak 0.6V. A Schmitt Trigger use is not necessary.
5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
6. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:

Figure 16. I_{CC} Test Condition, Power-down Mode

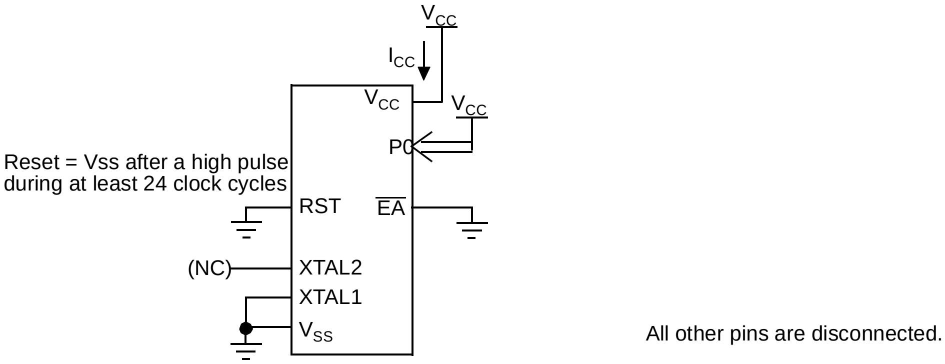
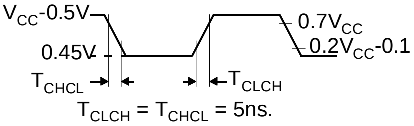


Figure 17. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes



AC Parameters

Explanation of the AC Symbols

Each timing symbol has 5 characters. The first character is always a “T” (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.

Example:T_{AVLL} = Time for Address Valid to ALE Low.
T_{LLPL} = Time for ALE Low to $\overline{\text{PSEN}}$ Low.

TA = 0 to +70°C (commercial temperature range); V_{SS} = 0 V; V_{CC} = 5V ± 10%; -M and -V ranges.
TA = -40°C to +85°C (industrial temperature range); V_{SS} = 0 V; V_{CC} = 5V ± 10%; -M and -V ranges.
TA = 0 to +70°C (commercial temperature range); V_{SS} = 0 V; 2.7 V < V_{CC} < 5.5V; -L range.
TA = -40°C to +85°C (industrial temperature range); V_{SS} = 0 V; 2.7 V < V_{CC} < 5.5V; -L range.

Table 24. gives the maximum applicable load capacitance for Port 0, Port 1, 2 and 3, and ALE and $\overline{\text{PSEN}}$ signals. Timings will be guaranteed if these capacitances are respected. Higher capacitance values can be used, but timings will then be degraded.

Table 24. Load Capacitance versus speed range, in pF

	-M	-V	-L
Port 0	100	50	100
Port 1, 2, 3	80	50	80
ALE / $\overline{\text{PSEN}}$	100	30	100

Table 5., Table 29. and Table 32. give the description of each AC symbols.

Table 27., Table 30. and Table 33. give for each range the AC parameter.

Table 28., Table 31. and Table 34. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

Table 25. Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20	40	30	30	20
T (ns)	25	50	25	33.3	33.3	50

Example:

T_{LLIV} in X2 mode for a -V part at 20 MHz ($T = 1/20^{E6} = 50$ ns):

x= 22 (Table 28.)

T= 50ns

$T_{LLIV}= 2T - x = 2 \times 50 - 22 = 78$ns

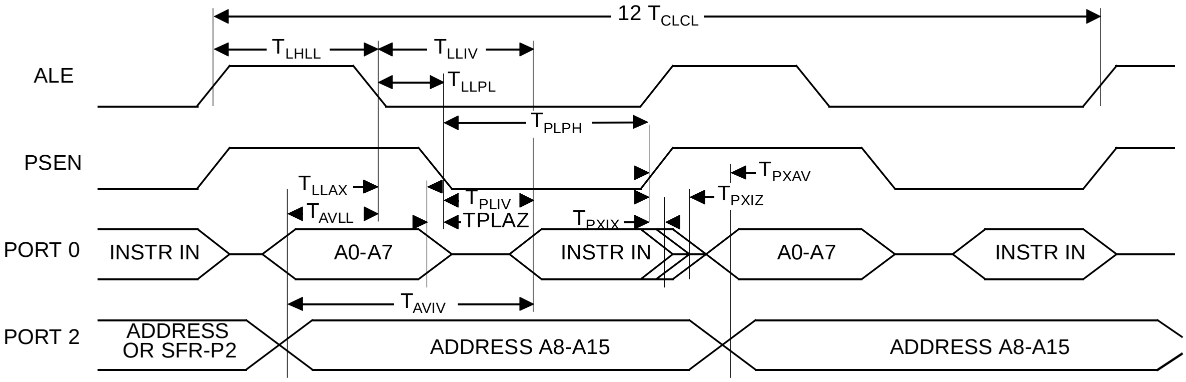
External Program Memory Characteristics

Table 26. Symbol Description

Symbol	Parameter
T	Oscillator clock period
T_{LHLL}	ALE pulse width
T_{AVLL}	Address Valid to ALE
T_{LLAX}	Address Hold After ALE
T_{LLIV}	ALE to Valid Instruction In
T_{LLPL}	ALE to $\overline{\text{PSEN}}$
T_{PLPH}	$\overline{\text{PSEN}}$ Pulse Width
T_{PLIV}	$\overline{\text{PSEN}}$ to Valid Instruction In
T_{PXIX}	Input Instruction Hold After $\overline{\text{PSEN}}$
T_{PXIZ}	Input Instruction FloatAfter $\overline{\text{PSEN}}$
T_{PXAV}	$\overline{\text{PSEN}}$ to Address Valid
T_{AVIV}	Address to Valid Instruction In
T_{PLAZ}	$\overline{\text{PSEN}}$ Low to Address Float

External Program Memory Read Cycle

Figure 18. External Program Memory Read Cycle



External Data Memory Characteristics

Table 29. Symbol Description

Symbol	Parameter
T_{RLRH}	$\overline{\text{RD}}$ Pulse Width
T_{WLWH}	$\overline{\text{WR}}$ Pulse Width
T_{RLDV}	$\overline{\text{RD}}$ to Valid Data In
T_{RHDX}	Data Hold After $\overline{\text{RD}}$
T_{RHDZ}	Data Float After $\overline{\text{RD}}$
T_{LLDV}	ALE to Valid Data In
T_{AVDV}	Address to Valid Data In
T_{LLWL}	ALE to $\overline{\text{WR}}$ or $\overline{\text{RD}}$
T_{AVWL}	Address to $\overline{\text{WR}}$ or $\overline{\text{RD}}$
T_{QVWX}	Data Valid to $\overline{\text{WR}}$ Transition
T_{QVWH}	Data set-up to $\overline{\text{WR}}$ High
T_{WHQX}	Data Hold After $\overline{\text{WR}}$
T_{RLAZ}	$\overline{\text{RD}}$ Low to Address Float
T_{WHLH}	$\overline{\text{RD}}$ or $\overline{\text{WR}}$ High to ALE high

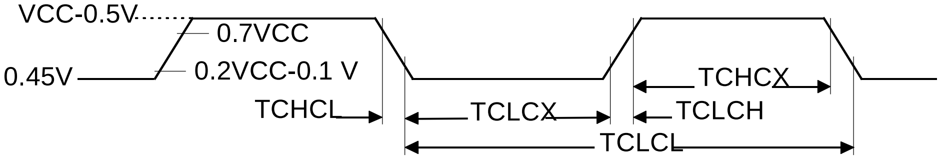
External Clock Drive Characteristics (XTAL1)

Table 36. AC Parameters

Symbol	Parameter	Min	Max	Units
T_{CLCL}	Oscillator Period	25		ns
T_{CHCX}	High Time	5		ns
T_{CLCX}	Low Time	5		ns
T_{CLCH}	Rise Time		5	ns
T_{CHCL}	Fall Time		5	ns
T_{CHCX}/T_{CLCX}	Cyclic ratio in X2 mode	40	60	%

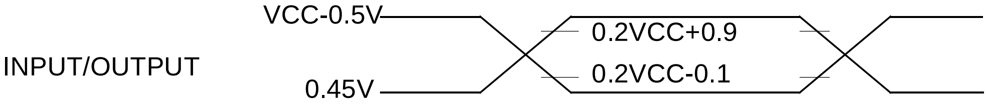
External Clock Drive Waveforms

Figure 23. External Clock Drive Waveforms



AC Testing Input/Output Waveforms

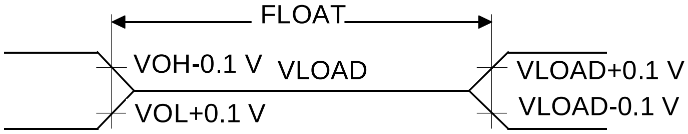
Figure 24. AC Testing Input/Output Waveforms



AC inputs during testing are driven at V_{CC} - 0.5 for a logic “1” and 0.45V for a logic “0”. Timing measurement are made at V_{IH} min for a logic “1” and V_{IL} max for a logic “0”.

Float Waveforms

Figure 25. Float Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20mA$.

Ordering Information

Table 37. Possible Ordering Entries

Part Number(3)	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS80C32X2-MCA	ROMLess	5V ±10%	Commercial	40 MHz(1)	PDIL40	Stick
TS80C32X2-MCB	ROMLess	5V ±10%	Commercial	40 MHz(1)	PLCC44	Stick
TS80C32X2-MCC	ROMLess	5V ±10%	Commercial	40 MHz(1)	PQFP44	Tray
TS80C32X2-MCE	ROMLess	5V ±10%	Commercial	40 MHz(1)	VQFP44	Tray
TS80C32X2-LCA	ROMLess	2.7 to 5.5V	Commercial	30 MHz(1)	PDIL40	Stick
TS80C32X2-LCB	ROMLess	2.7 to 5.5V	Commercial	30 MHz(1)	PLCC44	Stick
TS80C32X2-LCC	ROMLess	2.7 to 5.5V	Commercial	30 MHz(1)	PQFP44	Tray
TS80C32X2-LCE	ROMLess	2.7 to 5.5V	Commercial	30 MHz(1)	VQFP44	Tray
TS80C32X2-VCA	ROMLess	5V ±10%	Commercial	60 MHz(3)	PDIL40	Stick
TS80C32X2-VCB	ROMLess	5V ±10%	Commercial	60 MHz(3)	PLCC44	Stick
TS80C32X2-VCC	ROMLess	5V ±10%	Commercial	60 MHz(3)	PQFP44	Tray
TS80C32X2-VCE	ROMLess	5V ±10%	Commercial	60 MHz(3)	VQFP44	Tray
TS80C32X2-MIA	ROMLess	5V ±10%	Industrial	40 MHz(1)	PDIL40	Stick
TS80C32X2-MIB	ROMLess	5V ±10%	Industrial	40 MHz(1)	PLCC44	Stick
TS80C32X2-MIC	ROMLess	5V ±10%	Industrial	40 MHz(1)	PQFP44	Tray
TS80C32X2-MIE	ROMLess	5V ±10%	Industrial	40 MHz(1)	VQFP44	Tray
TS80C32X2-LIA	ROMLess	2.7 to 5.5V	Industrial	30 MHz(1)	PDIL40	Stick
TS80C32X2-LIB	ROMLess	2.7 to 5.5V	Industrial	30 MHz(1)	PLCC44	Stick
TS80C32X2-LIC	ROMLess	2.7 to 5.5V	Industrial	30 MHz(1)	PQFP44	Tray
TS80C32X2-LIE	ROMLess	2.7 to 5.5V	Industrial	30 MHz(1)	VQFP44	Tray
TS80C32X2-VIA	ROMLess	5V ±10%	Industrial	60 MHz(3)	PDIL40	Stick
TS80C32X2-VIB	ROMLess	5V ±10%	Industrial	60 MHz(3)	PLCC44	Stick
TS80C32X2-VIC	ROMLess	5V ±10%	Industrial	60 MHz(3)	PQFP44	Tray
TS80C32X2-VIE	ROMLess	5V ±10%	Industrial	60 MHz(3)	VQFP44	Tray
AT80C32X2-3CSUM	ROMLess	5V ±10%	Industrial & Green	40 MHz(1)	PDIL40	Stick
AT80C32X2-SLSUM	ROMLess	5V ±10%	Industrial & Green	40 MHz(1)	PLCC44	Stick
AT80C32X2-RLTUM	ROMLess	5V ±10%	Industrial & Green	40 MHz(1)	VQFP44	Tray
AT80C32X2-RLTUM	ROMLess	5V ±10%	Industrial & Green	40 MHz(1)	VQFP44	Tape & Reel
AT80C32X2-3CSUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz(1)	PDIL40	Stick
AT80C32X2-SLSUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz(1)	PLCC44	Stick

Table 37. Possible Ordering Entries (Continued)

Part Number(3)	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT80C52X2zzz-3CSUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz(1)	PDIL40	Stick
AT80C52X2zzz-SLSUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz(1)	PLCC44	Stick
AT80C52X2zzz-RLTUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz(1)	VQFP44	Tray
AT80C52X2zzz-3CSUV	8K ROM	5V ±10%	Industrial & Green	60 MHz(3)	PDIL40	Stick
AT80C52X2zzz-SLSUV	8K ROM	5V ±10%	Industrial & Green	60 MHz(3)	PLCC44	Stick
AT80C52X2zzz-RLTUV	8K ROM	5V ±10%	Industrial & Green	60 MHz(3)	VQFP44	Tray
TS87C52X2-MCA	8K OTP	5V ±10%	Commercial	40 MHz(1)	PDIL40	Stick
TS87C52X2-MCB	8K OTP	5V ±10%	Commercial	40 MHz(1)	PLCC44	Stick
TS87C52X2-MCC	8K OTP	5V ±10%	Commercial	40 MHz(1)	PQFP44	Tray
TS87C52X2-MCE	8K OTP	5V ±10%	Commercial	40 MHz(1)	VQFP44	Tray
TS87C52X2-LCA	8K OTP	2.7 to 5.5V	Commercial	30 MHz(1)	PDIL40	Stick
TS87C52X2-LCB	8K OTP	2.7 to 5.5V	Commercial	30 MHz(1)	PLC44	Stick
TS87C52X2-LCC	8K OTP	2.7 to 5.5V	Commercial	30 MHz(1)	PQFP44	Tray
TS87C52X2-LCE	8K OTP	2.7 to 5.5V	Commercial	30 MHz(1)	VQFP44	Tray
TS87C52X2-VCA	8K OTP	5V ±10%	Commercial	60 MHz(3)	PDIL40	Stick
TS87C52X2-VCB	8K OTP	5V ±10%	Commercial	60 MHz(3)	PLCC44	Stick
TS87C52X2-VCC	8K OTP	5V ±10%	Commercial	60 MHz(3)	PQFP44	Tray
TS87C52X2-VCE	8K OTP	5V ±10%	Commercial	60 MHz(3)	VQFP44	Tray
TS87C52X2-MIA	8K OTP	5V ±10%	Industrial	40 MHz(1)	PDIL40	Stick
TS87C52X2-MIB	8K OTP	5V ±10%	Industrial	40 MHz(1)	PLCC44	Stick
TS87C52X2-MIC	8K OTP	5V ±10%	Industrial	40 MHz(1)	PQFP44	Tray
TS87C52X2-MIE	8K OTP	5V ±10%	Industrial	40 MHz(1)	VQFP44	Tray
TS87C52X2-LIA	8K OTP	2.7 to 5.5V	Industrial	30 MHz(1)	PDIL40	Stick
TS87C52X2-LIB	8K OTP	2.7 to 5.5V	Industrial	30 MHz(1)	PLCC44	Stick
TS87C52X2-LIC	8K OTP	2.7 to 5.5V	Industrial	30 MHz(1)	PQFP44	Tray
TS87C52X2-LIE	8K OTP	2.7 to 5.5V	Industrial	30 MHz(1)	VQFP44	Tray
TS87C52X2-VIA	8K OTP	5V ±10%	Industrial	60 MHz(3)	PDIL40	Stick
TS87C52X2-VIB	8K OTP	5V ±10%	Industrial	60 MHz(3)	PLCC44	Stick
TS87C52X2-VIC	8K OTP	5V ±10%	Industrial	60 MHz(3)	PQFP44	Tray
TS87C52X2-VIE	8K OTP	5V ±10%	Industrial	60 MHz(3)	VQFP44	Tray

Table 37. Possible Ordering Entries (Continued)

Part Number[3]	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT87C52X2-3CSUM	8K OTP	5V ±10%	Industrial & Green	40 MHz(1)	PDIL40	Stick
AT87C52X2-SLSUM	8K OTP	5V ±10%	Industrial & Green	40 MHz(1)	PLCC44	Stick
AT87C52X2-RLTUM	8K OTP	5V ±10%	Industrial & Green	40 MHz(1)	VQFP44	Tray
AT87C52X2-3CSUL	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz(1)	PDIL40	Stick
AT87C52X2-SLSUL	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz(1)	PLCC44	Stick
AT87C52X2-RLTUL	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz(1)	VQFP44	Tray
AT87C52X2-3CSUV	8K OTP	5V ±10%	Industrial & Green	60 MHz(3)	PDIL40	Stick
AT87C52X2-SLSUV	8K OTP	5V ±10%	Industrial & Green	60 MHz(3)	PLCC44	Stick
AT87C52X2-RLTUV	8K OTP	5V ±10%	Industrial & Green	60 MHz(3)	VQFP44	Tray

Notes:
1. 20 MHz in X2 Mode.
2. Tape and Reel available for SL, PQFP and RL packages
3. 30 MHz in X2 Mode.