



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-VQFP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c52x2-lce

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

SFR Mapping

The Special Function Registers (SFRs) of the TS80C52X2 fall into the following categories:

- C51 core registers: ACC, B, DPH, DPL, PSW, SP, AUXR1
- I/O port registers: P0, P1, P2, P3
- Timer registers: T2CON, T2MOD, TCON, TH0, TH1, TH2, TMOD, TL0, TL1, TL2, RCAP2L, RCAP2H
- Serial I/O port registers: SADDR, SADEN, SBUF, SCON
- Power and clock control registers: PCON
- Interrupt system registers: IE, IP, IPH
- Others: AUXR, CKCON





Table 2. All SFRs with their address and their reset value

	Bit Addressable		Non Bit Addressable									
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F				
F8h									FFh			
F0h	B 0000 0000								F7h			
E8h									EFh			
E0h	ACC 0000 0000								E7h			
D8 h									DFh			
D0 h	PSW 0000 0000								D7h			
C8 h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh			
C0 h									C7h			
B8h	IP XX00 0000	SADEN 0000 0000							BFh			
B0h	P3 1111 1111							IPH XX00 0000	B7h			
A8h	IE 0X00 0000	SADDR 0000 0000							AFh			
A0h	P2 1111 1111		AUXR1 XXXX XXX0						A7h			
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh			
90h	P1 1111 1111								97h			
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXXXXX0	CKCON XXXX XXX0	8Fh			
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h			
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F				

Reserved

Pin Configuration



*NIC: No Internal Connection





Mnemonic	Pin Number			Туре	Name and Function			
	DIL	LCC	VQFP 1.4					
V _{SS}	20	22	16	I	Ground: 0V reference			
Vss1		1	39	I	Optional Ground: Contact the Sales Office for ground connection.			
V _{cc}	40	44	38	I	Power Supply: This is the power supply voltage for normal, idle and power-down operation			
P0.0-P0.7	39- 32	43- 36	37-30	I/O	Port 0 : Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as bidh impedance inputs Port 0 pins must be polarized to Vcc.			
					or Vss in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes.			
P1.0-P1.7	1-8	2-9	40-44 1-3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled bids by the internal pull-ups and can be used as inputs. As			
					high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receiv the low-order address byte during memory programming a verification. Alternate functions for Port 1 include:			
	1	2	40	I/O	T2 (P1.0): Timer/Counter 2 external count input/Clockout			
	2	3	41	1	T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction Control			
P2.0-P2.7	21- 28	24- 31	18-25	I/O	Port 2 : Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled with a structure of a structure of the structure			
					high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high- order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX atDPTR). In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX atRi), port 2 emits the contents of the P2 SFR. Some Port 2 pins receive the high order address bits during EPROM programming and verification: P2.0 to P2.4			
P3.0-P3.7	10- 17	11, 13- 19	5, 7-13	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source			
					current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below.			
	10	11	5	I	RXD (P3.0): Serial input port			
	11	13	7	0	TXD (P3.1): Serial output port			
	12	14	8	Ι	INT0 (P3.2): External interrupt 0			

TS8xCx2X2

6

Timer 2	The timer 2 in the TS80C52X2 is compatible with the timer 2 in the 80C52. It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 5) and T2MOD register (See Table 6). Timer 2 operation is similar to Timer 0 and Timer 1. C/T2 selects $F_{OSC}/12$ (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.
	Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/RL2 (T2CON), as described in the Atmel 8-bit Microcontroller Hardware description.
	Refer to the Atmel 8-bit Microcontroller Hardware description for the description of Cap- ture and Baud Rate Generator Modes.
	In TS80C52X2 Timer 2 includes the following enhancements:
	Auto-reload mode with up or down counter
	Programmable clock-output
Auto-reload Mode	The Auto-reload mode configures timer 2 as a 16-bit timer or event counter with auto- matic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 4. In this mode the T2EX pin controls the direction of count.
	When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.
	When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.
	The EXF2 bit toggles when timer 2 overflows or underflows according to the the direc- tion of the count. EXF2 does not generate any interrupt. This bit can be used to provide

17-bit resolution.

12 **TS8xCx2X2**





For slave A, bit 0 (the LSB) is a don't-care bit; for slaves B and C, bit 0 is a 1. To communicate with slave A only, the master must send an address where bit 0 is clear (e.g.

18 **TS8xCx2X2**



Table 9.SCON RegisterSCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0		
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI		
Bit Number	Bit Mnemonic	Description							
7	FE	Framing Error Clear to reset Set by hardwa SMOD0 must	r bit (SMOD0 the error state re when an in be set to enal	=1) e, not cleared avalid stop bit ole access to	l by a valid stop is detected. the FE bit	bit.			
	SM0	Serial port Mo Refer to SM1 f SMOD0 must	ode bit 0 for serial port be cleared to	mode selecti enable acce	on. ss to the SM0 b	it			
6	SM1	Serial port Mo SM0 SM1 0 0 1 0 1 1 1 1	Serial port Mode bit 1 SM0 SM1 Mode Description Baud Rate 0 0 0 Shift Register F _{XTAL} /12 (/6 in X2 mode) 0 1 1 8-bit UART Variable 1 0 2 9-bit UART F _{XTAL} /64 or F _{XTAL} /32 (/32, /16 in X2 mode) 1 1 3 9-bit UART Variable						
5	SM2	Serial port Mo Clear to disabl Set to enable r eventually mod	Serial port Mode 2 bit / Multiprocessor Communication Enable bit Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.						
4	REN	Reception En Clear to disabl Set to enable s	able bit e serial recep serial receptic	otion. on.					
3	TB8	Transmitter Bit Clear to transr Set to transmit	: 8 / Ninth bit t nit a logic 0 in : a logic 1 in tł	to transmit in 1 the 9th bit. 1 he 9th bit.	modes 2 and 3				
2	RB8	Receiver Bit 8 Cleared by hau Set by hardwa In mode 1, if S	B / Ninth bit r rdware if 9th b re if 9th bit re M2 = 0, RB8	eceived in n bit received is ceived is a lo is the receive	nodes 2 and 3 s a logic 0. ogic 1. ed stop bit. In m	ode 0 RB8 is	not used.		
1	TI	Transmit Inter Clear to ackno Set by hardwa stop bit in the o	rrupt flag wledge interr re at the end other modes.	upt. of the 8th bit	time in mode 0	or at the begi	nning of the		
0	RI	Receive Intern Clear to ackno Set by hardwa 8. in the other	rupt flag wledge interr re at the end modes.	upt. of the 8th bit	time in mode 0,	see Figure 7	'. and Figure		

Reset Value = 0000 0000b Bit addressable

Table 10. PCON RegisterPCON - Power Control Register (87h)

7	6	5	4	3	2	1	0			
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL			
Bit Number	Bit Mnemonic	Descriptio	Description							
7	SMOD1	Serial port Set to sele	Serial port Mode bit 1 Set to select double baud rate in mode 1, 2 or 3.							
6	SMOD0	Serial port Clear to sel Set to to se	erial port Mode bit 0 Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.							
5	-	Reserved The value r	Reserved The value read from this bit is indeterminate. Do not set this bit.							
4	POF	Power-off Clear to rec Set by hard by software	Power-off Flag Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.							
3	GF1	General pu Cleared by Set by user	Irpose Flag user for gene for general p	ral purpose us urpose usage	sage.					
2	GF0	General pu Cleared by Set by user	Irpose Flag user for gene for general p	ral purpose us urpose usage	sage.					
1	PD	Power-dow Cleared by Set to enter	vn mode bit hardware wh r power-down	en reset occur mode.	S.					
0	IDL	Idle mode Clear by ha Set to enter	bit Irdware when r idle mode.	interrupt or re	set occurs.					

Reset Value = 00X1 0000b Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.



Table 14.IPH RegisterIPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	-	PT2H	PSH	PT1H	PX1H	РТОН	PX0H
Bit Number	Bit Mnemonic	Description					
7	-	Reserved The value rea	d from this bit	is indetermina	ate. Do not se	t this bit.	
6	-	Reserved The value rea	d from this bit	is indetermina	ate. Do not se	t this bit.	
5	PT2H	Timer 2 over PT2H PT2 0 0 1 0 1 1	flow interrup Priority Leve Lowest Highest	t Priority Higl _임	ı bit		
4	PSH	Serial port P PSH PS 0 0 1 0 1 1	riority High b <u>Priority Leve</u> Lowest Highest	it el			
3	PT1H	Timer 1 over PT1H PT1 0 0 1 0 1 1	flow interrupt Priority Leve Lowest Highest	t Priority Higl ગ	ו bit		
2	PX1H	External inte PX1H PX1 0 0 0 1 1 0 1 1	rrupt 1 Priori <u>Priority Leve</u> Lowest Highest	ty High bit 한			
1	РТОН	Timer 0 over PTOH PTO 0 0 1 0 1 1	flow interrup Priority Leve Lowest Highest	t Priority Higl <u>위</u>	ı bit		
0	РХОН	External inte PX0H PX0 0 0 1 1 1 1	rrupt 0 Priori Priority Leve Lowest Highest	ty High bit 1			

Reset Value = XX00 0000b Not bit addressable



Power-off Flag

The power-off flag allows the user to distinguish between a "cold start" reset and a "warm start" reset.

A cold start reset is the one induced by V_{CC} switch-on. A warm start reset occurs while V_{CC} is still applied to the device and could be generated for example by an exit from power-down.

The power-off flag (POF) is located in PCON register (See Table 17.). POF is set by hardware when V_{CC} rises from 0 to its nominal voltage. The POF can be set or cleared by software allowing the user to determine the type of reset.

The POF value is only relevant with a Vcc range from 4.5V to 5.5V. For lower Vcc value, reading POF bit will return indeterminate value.

7	6	5	4	3	2	1	0			
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL			
Bit Number	Bit Mnemonic	Descript	ion							
7	SMOD1	Serial po Set to se	rt Mode bit 1 lect double b	l aud rate in mo	de 1, 2 or 3.					
6	SMOD0	Serial po Clear to s Set to to s	erial port Mode bit 0 lear to select SM0 bit in SCON register. et to to select FE bit in SCON register.							
5	-	Reserved The value	Reserved The value read from this bit is indeterminate. Do not set this bit.							
4	POF	Power-of Clear to r Set by ha set by so	i f Flag ecognize nex rdware when ftware.	t reset type. V _{CC} rises fron	n 0 to its nomi	nal voltage. Ca	an also be			
3	GF1	General Cleared b Set by us	purpose Flag by user for ge er for genera	g neral purpose l purpose usaç	usage. je.					
2	GF0	General Cleared b Set by us	purpose Flag by user for ge er for genera	3 neral purpose I purpose usaç	usage. je.					
1	PD	Power-de Cleared b Set to en	Power-down mode bit Cleared by hardware when reset occurs. Set to enter power-down mode.							
0	IDL	Idle mod Clear by Set to en	e bit hardware whe ter idle mode.	en interrupt or	reset occurs.					

Table 17. PCON Register

PCON - Power Control Register (87h)

Reset Value = 00X1 0000b Not bit addressable





Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 18. AUXR Register

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0				
-	-	-	-	-	-	-	AO				
Bit Number	Bit Mnemonic	Description	Description								
7	-	Reserved The value rea	eserved he value read from this bit is indeterminate. Do not set this bit.								
6	-	Reserved The value rea	eserved le value read from this bit is indeterminate. Do not set this bit.								
5	-	Reserved The value rea	eserved ne value read from this bit is indeterminate. Do not set this bit.								
4	-	Reserved The value rea	ad from this b	it is indetermi	nate. Do not s	et this bit.					
3	-	Reserved The value rea	ad from this b	it is indetermi	nate. Do not s	et this bit.					
2	-	Reserved The value rea	ad from this b	it is indetermi	nate. Do not s	et this bit.					
1	-	Reserved The value rea	ad from this b	it is indetermi	nate. Do not s	et this bit.					
0	AO	ALE Output Clear to resto Set to disable	bit pre ALE opera e ALE operati	ation during in on during inte	ternal fetches rnal fetches.						

Reset Value = XXXX XXX0b Not bit addressable

TS80C52X2

ROM Structure The T

The TS80C52X2 ROM memory is divided in three different arrays:

- the code array:8 Kbytes.
- the encryption array:64 bytes.
- the signature array:4 bytes.

ROM Lock System The program Lock system, when programmed, protects the on-chip program against software piracy.

Encryption Array Within the ROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

Program Lock BitsThe lock bits when programmed according to Table 19. will provide different level of pro-
tection for the on-chip code and data.

Table 19.	Program	Lock bits	
Pr	ogram Lock	Bits	

Pi	rogram L	ock Bits		
Security level	LB1	LB2	LB3	Protection Description
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	Ρ	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset.

U: unprogrammed P: programmed

Signature bytes

The TS80C52X2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 9.

Verify Algorithm

Refer to Section "Verify Algorithm".



TS8xCx2X2

Control and program signals must be held at the levels indicated in Table 35.

Definition of terms

Address Lines: P1.0-P1.7, P2.0-P2.4 respectively for A0-A12 Data Lines: P0.0-P0.7 for D0-D7 Control Signals: RST, PSEN, P2.6, P2.7, P3.3, P3.6, P3.7. Program Signals: ALE/PROG, EA/VPP.

Table 20. EPROM Set-up Modes

Mode	RST	PSEN	ALE/ PROG	EA/ VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code data	1	0	Ţ	12.75V	0	1	1	1	1
Verify Code data	1	0	1	1	0		0	1	1
Program Encryption Array Address 0-3Fh	1	0	U	12.75V	0	1	1	0	1
Read Signature Bytes	1	0	1	1	0	٦_٢	0	0	0
Program Lock bit 1	1	0	ប	12.75V	1	1	1	1	1
Program Lock bit 2	1	0	Ъ	12.75V	1	1	1	0	0
Program Lock bit 3	1	0	Ъ	12.75V	1	0	1	1	0

Figure 11. Set-Up Modes Configuration



* See Table 31. for proper value on these inputs



TS8xCx2X2

Port 0: 26 mA Ports 1, 2 and 3: 15 mA Maximum total I_{OL} for all output pins: 71 mA If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

- 7. For other values, please contact your sales office.
- Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 17.), V_{IL} = V_{SS} + 0.5V,

 $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; $\overline{EA} = Port 0 = V_{CC}$; RST = V_{SS} . The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.

Figure 13. I_{CC} Test Condition, under reset



All other pins are disconnected.





All other pins are disconnected.

Figure 15. I_{CC} Test Condition, Idle Mode



All other pins are disconnected.





Figure 16. I_{CC} Test Condition, Power-down Mode



All other pins are disconnected.

Figure 17. Clock Signal Waveform for I_{CC} Tests in Active and Idle Modes



AC Parameters

Explanation of the AC Symbols	Each timing symbol has 5 characters. The first character is always a "T" (stands for time). The other characters, depending on their positions, stand for the name of a signal or the logical status of that signal. The following is a list of all the characters and what they stand for.						
	Example:T _{AVLL} = Time for Addr <u>ess Va</u> lid to ALE Low. T _{LLPL} = Time for ALE Low to PSEN Low.						
	TA = 0 to +70°C (commercial temperature range); $V_{SS} = 0$ V; $V_{CC} = 5V \pm 10\%$; -M and -V ranges. TA = -40°C to +85°C (industrial temperature range); $V_{SS} = 0$ V; $V_{CC} = 5V \pm 10\%$; -M and -V ranges. TA = 0 to +70°C (commercial temperature range); $V_{SS} = 0$ V; 2.7 V < $V_{CC} < 5.5$ V; -L range. TA = -40°C to +85°C (industrial temperature range); $V_{SS} = 0$ V; 2.7 V < $V_{CC} < 5.5$ V; -L range.						
	Table 24. giv and ALE and respected. Hi Table 24. Los	e <u>s the m</u> aximum applica I PSEN signals. Timing gher capacitance values ad Capacitance versus s	ble load capacitance for s will be guaranteed if can be used, but timings peed range, in pF	r Port 0, Port 1, 2 and 3, these capacitances are will then be degraded.			
		-M	-V	-L			
	Port 0	100	50	100			
	Port 1, 2, 3	80	50	80			
	ALE / PSEN	100	30	100			

Table 5., Table 29. and Table 32. give the description of each AC symbols.

Table 27., Table 30. and Table 33. give for each range the AC parameter.

Table 28., Table 31. and Table 34. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

Table 25. Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20	40	30	30	20
T (ns)	25	50	25	33.3	33.3	50

Example:

 T_{LLIV} in X2 mode for a -V part at 20 MHz (T = 1/20^{E6} = 50 ns):

```
x= 22 (Table 28.)
```

T= 50ns

T_{LLIV}= 2T - x = 2 x 50 - 22 = 78ns

External Program Memory Characteristics

Table 26. Symbol Description

Symbol	Parameter
Т	Oscillator clock period
T _{LHLL}	ALE pulse width
T _{AVLL}	Address Valid to ALE
T _{LLAX}	Address Hold After ALE
T _{LLIV}	ALE to Valid Instruction In
T _{LLPL}	ALE to PSEN
T _{PLPH}	PSEN Pulse Width
T _{PLIV}	PSEN to Valid Instruction In
T _{PXIX}	Input Instruction Hold After PSEN
T _{PXIZ}	Input Instruction FloatAfter PSEN
T _{PXAV}	PSEN to Address Valid
T _{AVIV}	Address to Valid Instruction In
T _{PLAZ}	PSEN Low to Address Float





EPROM Programming and Verification Characteristics

 T_A = 21°C to 27°C; V_{SS} = 0V; $~V_{CC}$ = 5V \pm 10% while programming. V_{CC} = operating range while verifying.

 Table 35.
 EPROM Programming Parameters

Symbol	Parameter	Min	Max	Units
V _{PP}	Programming Supply Voltage	12.5	13	V
I _{PP}	Programming Supply Current		75	mA
1/T _{CLCL}	Oscillator Frquency	4	6	MHz
T _{AVGL}	Address Setup to PROG Low	48 T _{CLCL}		
T _{GHAX}	Adress Hold after PROG	48 T _{CLCL}		
T _{DVGL}	Data Setup to PROG Low	48 T _{CLCL}		
T _{GHDX}	Data Hold after PROG	48 T _{CLCL}		
T _{EHSH}	(Enable) High to V _{PP}	48 T _{CLCL}		
T _{SHGL}	V _{PP} Setup to PROG Low	10		μs
T _{GHSL}	V _{PP} Hold after PROG	10		μs
T _{GLGH}	PROG Width	90	110	μs
T _{AVQV}	Address to Valid Data		48 T _{CLCL}	
T _{ELQV}	ENABLE Low to Data Valid		48 T _{CLCL}	
T _{EHQZ}	Data Float after ENABLE	0	48 T _{CLCL}	

EPROM Programming and Verification Waveforms

Figure 22. EPROM Programming and Verification Waveforms



* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

Ordering Information

Table 37. Possible Ordering Entries

Part Number ⁽³⁾	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS80C32X2-MCA	ROMLess	5V <u>±</u> 10%	Commercial	40 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-MCB	ROMLess	5V <u>±</u> 10%	Commercial	40 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-MCC	ROMLess	5V <u>±</u> 10%	Commercial	40 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-MCE	ROMLess	5V <u>±</u> 10%	Commercial	40 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-LCA	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-LCB	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-LCC	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-LCE	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-VCA	ROMLess	5V <u>±</u> 10%	Commercial	60 MHz ⁽³⁾	PDIL40	Stick
TS80C32X2-VCB	ROMLess	5V <u>±</u> 10%	Commercial	60 MHz ⁽³⁾	PLCC44	Stick
TS80C32X2-VCC	ROMLess	5V <u>±</u> 10%	Commercial	60 MHz ⁽³⁾	PQFP44	Tray
TS80C32X2-VCE	ROMLess	5V <u>±</u> 10%	Commercial	60 MHz ⁽³⁾	VQFP44	Tray
TS80C32X2-MIA	ROMLess	5V <u>±</u> 10%	Industrial	40 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-MIB	ROMLess	5V <u>±</u> 10%	Industrial	40 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-MIC	ROMLess	5V <u>±</u> 10%	Industrial	40 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-MIE	ROMLess	5V <u>±</u> 10%	Industrial	40 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-LIA	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-LIB	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-LIC	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-LIE	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-VIA	ROMLess	5V <u>±</u> 10%	Industrial	60 MHz ⁽³⁾	PDIL40	Stick
TS80C32X2-VIB	ROMLess	5V <u>±</u> 10%	Industrial	60 MHz ⁽³⁾	PLCC44	Stick
TS80C32X2-VIC	ROMLess	5V <u>±</u> 10%	Industrial	60 MHz ⁽³⁾	PQFP44	Tray
TS80C32X2-VIE	ROMLess	5V <u>±</u> 10%	Industrial	60 MHz ⁽³⁾	VQFP44	Tray
AT80C32X2-3CSUM	ROMLess	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	PDIL40	Stick
AT80C32X2-SLSUM	ROMLess	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	PLCC44	Stick
AT80C32X2-RLTUM	ROMLess	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	VQFP44	Tray
AT80C32X2-RLTUM	ROMLess	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	VQFP44	Tape & Reel
AT80C32X2-3CSUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PDIL40	Stick
AT80C32X2-SLSUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PLCC44	Stick





Table 37. Possible Ordering Entries (Continued)

			Tomporatura			
Part Number ⁽³⁾	Memory Size	Supply Voltage	Range	Max Frequency	Package	Packing
AT80C32X2-RLTUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	VQFP44	Tray
AT80C32X2-3CSUV	ROMLess	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	PDIL40	Stick
AT80C32X2-SLSUV	ROMLess	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	PLCC44	Stick
AT80C32X2-RLTUV	ROMLess	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	VQFP44	Tray
TS80C52X2zzz-MCA	8K ROM	2.7 to 5.5V	Commercial	40 MHz ⁽¹⁾	PDIL40	Stick
TS80C52X2zzz-MCB	8K ROM	2.7 to 5.5V	Commercial	40 MHz ⁽¹⁾	PLCC44	Stick
TS80C52X2zzz-MCC	8K ROM	2.7 to 5.5V	Commercial	40 MHz ⁽¹⁾	PQFP44	Tray
TS80C52X2zzz-MCE	8K ROM	2.7 to 5.5V	Commercial	40 MHz ⁽¹⁾	VQFP44	Tray
TS80C52X2zzz-LCA	8K ROM	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PDIL40	Stick
TS80C52X2zzz-LCB	8K ROM	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PLCC44	Stick
TS80C52X2zzz-LCC	8K ROM	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PQFP44	Tray
TS80C52X2zzz-LCE	8K ROM	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	VQFP44	Tray
TS80C52X2zzz-VCA	8K ROM	5V <u>±</u> 10%	Commercial	60 MHz ⁽³⁾	PDIL40	Stick
TS80C52X2zzz-VCB	8K ROM	5V ±10%	Commercial	60 MHz ⁽³⁾	PLCC44	Stick
TS80C52X2zzz-VCC	8K ROM	5V ±10%	Commercial	60 MHz ⁽³⁾	PQFP44	Tray
TS80C52X2zzz-VCE	8K ROM	5V ±10%	Commercial	60 MHz ⁽³⁾	VQFP44	Tray
TS80C52X2zzz-MIA	8K ROM	5V ±10%	Industrial	40 MHz ⁽¹⁾	PDIL40	Stick
TS80C52X2zzz-MIB	8K ROM	5V ±10%	Industrial	40 MHz ⁽¹⁾	PLCC44	Stick
TS80C52X2zzz-MIC	8K ROM	5V ±10%	Industrial	40 MHz ⁽¹⁾	PQFP44	Tray
TS80C52X2zzz-MIE	8K ROM	5V ±10%	Industrial	40 MHz ⁽¹⁾	VQFP44	Tray
TS80C52X2zzz-LIA	8K ROM	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PDIL40	Stick
TS80C52X2zzz-LIB	8K ROM	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PLCC44	Stick
TS80C52X2zzz-LIC	8K ROM	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PQFP44	Tray
TS80C52X2zzz-LIE	8K ROM	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	VQFP44	Tray
TS80C52X2zzz-VIA	8K ROM	5V ±10%	Industrial	60 MHz ⁽³⁾	PDIL40	Stick
TS80C52X2zzz-VIB	8K ROM	5V ±10%	Industrial	60 MHz ⁽³⁾	PLCC44	Stick
TS80C52X2zzz-VIC	8K ROM	5V ±10%	Industrial	60 MHz ⁽³⁾	PQFP44	Tray
TS80C52X2zzz-VIE	8K ROM	5V ±10%	Industrial	60 MHz ⁽³⁾	VQFP44	Tray
AT80C52X2zzz-3CSUM	8K ROM	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	PDIL40	Stick
AT80C52X2zzz-SLSUM	8K ROM	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	PLCC44	Stick
AT80C52X2zzz-RLTUM	8K ROM	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	VQFP44	Tray



Table 37. Possible Ordering Entries (Continued)

Part Number ⁽³⁾	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT87C52X2-3CSUM	8K OTP	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	PDIL40	Stick
AT87C52X2-SLSUM	8K OTP	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	PLCC44	Stick
AT87C52X2-RLTUM	8K OTP	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	VQFP44	Тгау
AT87C52X2-3CSUL	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PDIL40	Stick
AT87C52X2-SLSUL	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PLCC44	Stick
AT87C52X2-RLTUL	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	VQFP44	Tray
AT87C52X2-3CSUV	8K OTP	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	PDIL40	Stick
AT87C52X2-SLSUV	8K OTP	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	PLCC44	Stick
AT87C52X2-RLTUV	8K OTP	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	VQFP44	Tray

Notes: 1. 20 MHz in X2 Mode.

2. Tape and Reel available for SL, PQFP and RL packages

3. 30 MHz in X2 Mode.