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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	30/20MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	44-PLCC (16.6x16.6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c52x2-lib

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Pin Configuration



*NIC: No Internal Connection



Mnemonic		Pin Nu	mber	Туре	Name and Function
	DIL	LCC	VQFP 1.4		
	13	15	9	I	INT1 (P3.3): External interrupt 1
	14	16	10	I	T0 (P3.4): Timer 0 external input
	15	17	11	I	T1 (P3.5): Timer 1 external input
	16	18	12	0	WR (P3.6): External data memory write strobe
	17	19	13	0	RD (P3.7): External data memory read strobe
Reset	9	10	4	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal diffused resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC} .
ALE/PROG	30	33	27	O (I)	Address Latch Enable/Program Pulse: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted at a constant rate of 1/6 (1/3 in X2 mode) the oscillator frequency, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. This pin is also the program pulse input (PROG) during EPROM programming. ALE can be disabled by setting SFR's AUXR.0 bit. With this bit set, ALE will be inactive during internal fetches.
PSEN	29	32	26	0	Program Store ENable: The read strobe to external program memory. When executing code from the external program memory, <u>PSEN</u> is activated twice each machine cycle, except that two <u>PSEN</u> activations are skipped during each access to external data memory. <u>PSEN</u> is not activated during fetches from internal program memory.
EA/V _{PP}	31	35	29	1	External Access Enable/Programming Supply Voltage: EA must be externally held low to enable the device to fetch code from external program memory locations 0000H and 3FFFH (RB) or 7FFFH (RC), or FFFFH (RD). If EA is held high, the device executes from internal program memory unless the program counter contains an address greater than 3FFFH (RB) or 7FFFH (RC) EA must be held low for ROMless devices. This pin also receives the 12.75V programming supply voltage (V _{PP}) during EPROM programming. If security level 1 is programmed, EA will be internally latched on Reset.
XTAL1	19	21	15	I	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.
XTAL2	18	20	14	0	Crystal 2: Output from the inverting oscillator amplifier



Table 5	. T2CON	l Register
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T2CON - Timer 2 Control Register (C8h)

7	6	5	4	3	2	1	0		
TF2	EXF2	RCLK	RCLK TCLK EXEN2 TR2 C/T2#				CP/RL2#		
Bit Number	Bit Mnemonic	Description							
7	TF2	Timer 2 overf Must be cleare Set by hardwa	Fimer 2 overflow Flag Must be cleared by software. Set by hardware on timer 2 overflow, if RCLK = 0 and TCLK = 0.						
6	EXF2	Timer 2 Exter Set when a ca EXEN2=1. When set, cau interrupt is ena Must be cleare mode (DCEN	Fimer 2 External Flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. When set, causes the CPU to vector to timer 2 interrupt routine when timer 2 nterrupt is enabled. Must be cleared by software. EXF2 doesn't cause an interrupt in Up/down counter mode (DCEN = 1)						
5	RCLK	Receive Clock Clear to use time Set to use time	Receive Clock bit Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3. Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3.						
4	TCLK	Transmit Cloc Clear to use tin Set to use time	Transmit Clock bit Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3. Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3.						
3	EXEN2	Timer 2 Exter Clear to ignore Set to cause a detected, if tim	Timer 2 External Enable bit Clear to ignore events on T2EX pin for timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port.						
2	TR2	Timer 2 Run of Clear to turn of Set to turn on t	Timer 2 Run control bit Clear to turn off timer 2. Set to turn on timer 2.						
1	C/T2#	Timer/Counte Clear for timer Set for counter for clock out m	Timer/Counter 2 select bit Clear for timer operation (input from internal clock system: F _{OSC}). Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode.						
0	CP/RL2#	Timer 2 Captu If RCLK=1 or 7 timer 2 overflo Clear to Auto-r EXEN2=1. Set to capture	for clock out mode. Timer 2 Capture/Reload bit If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to Auto-reload on timer 2 overflow. Clear to Auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1. Set to capture on negative transitions on T2EX pin if EXEN2=1.						

Reset Value = 0000 0000b Bit addressable





Table 9.SCON RegisterSCON - Serial Control Register (98h)

7	6	5	4	3	2	1	0		
FE/SM0	SM1	SM2	REN	TB8	RB8	TI	RI		
Bit Number	Bit Mnemonic	Description							
7	FE	Framing Error Clear to reset Set by hardwa SMOD0 must	Framing Error bit (SMOD0=1) Clear to reset the error state, not cleared by a valid stop bit. Set by hardware when an invalid stop bit is detected. SMOD0 must be set to enable access to the FE bit						
	SM0	Serial port Mo Refer to SM1 f SMOD0 must	ode bit 0 for serial port be cleared to	mode selecti enable acce	on. ss to the SM0 b	it			
6	SM1	Serial port Mo SM0 SM1 0 0 1 0 1 1 1 1	$\begin{array}{c c c c c c c c c c c c c c c c c c c $						
5	SM2	Serial port Mo Clear to disabl Set to enable r eventually mod	Serial port Mode 2 bit / Multiprocessor Communication Enable bit Clear to disable multiprocessor communication feature. Set to enable multiprocessor communication feature in mode 2 and 3, and eventually mode 1. This bit should be cleared in mode 0.						
4	REN	Reception En Clear to disabl Set to enable s	able bit e serial recep serial receptic	otion. on.					
3	TB8	Transmitter Bit Clear to transr Set to transmit	: 8 / Ninth bit t nit a logic 0 in : a logic 1 in tł	to transmit in 1 the 9th bit. 1 he 9th bit.	modes 2 and 3				
2	RB8	Receiver Bit 8 Cleared by hau Set by hardwa In mode 1, if S	Receiver Bit 8 / Ninth bit received in modes 2 and 3 Cleared by hardware if 9th bit received is a logic 0. Set by hardware if 9th bit received is a logic 1. In mode 1, if SM2 = 0, RB8 is the received stop bit. In mode 0 RB8 is not used.						
1	TI	Transmit Inter Clear to ackno Set by hardwa stop bit in the o	Transmit Interrupt flag Clear to acknowledge interrupt. Set by hardware at the end of the 8th bit time in mode 0 or at the beginning of the stop bit in the other modes.						
0	RI	Receive Intern Clear to ackno Set by hardwa 8. in the other	rupt flag wledge interr re at the end modes.	upt. of the 8th bit	time in mode 0,	see Figure 7	'. and Figure		

Reset Value = 0000 0000b Bit addressable



Interrupt System

The TS80C52X2 has a total of 6 interrupt vectors: two external interrupts (INT0 and INT1), three timer interrupts (timers 0, 1 and 2) and the serial port interrupt. These interrupts are shown in Figure 9.

Figure 9. Interrupt Control System



Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 12.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 13.) and in the Interrupt Priority High register (See Table 14.). shows the bit values and priority levels associated with each combination.

Table 11. Priority Level Bit Values	

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level

are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Table 12. IE Register

IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0		
EA	-	ET2	ES	ET1	EX1	ET0	EX0		
Bit Number	Bit Mnemonic	Description							
7	EA	Enable All int Clear to disab Set to enable If EA=1, each clearing its ow	Enable All interrupt bit Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.						
6	-	Reserved The value read	d from this bit	is indetermina	ate. Do not se	t this bit.			
5	ET2	Timer 2 overf Clear to disab Set to enable	Fimer 2 overflow interrupt Enable bit Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.						
4	ES	Serial port Er Clear to disab Set to enable	n able bit le serial port i serial port inte	nterrupt. errupt.					
3	ET1	Timer 1 overf Clear to disab Set to enable	Timer 1 overflow interrupt Enable bit Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.						
2	EX1	External inter Clear to disab Set to enable	External interrupt 1 Enable bit Clear to disable external interrupt 1. Set to enable external interrupt 1.						
1	ET0	Timer 0 overf Clear to disab Set to enable	Timer 0 overflow interrupt Enable bit Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.						
0	EX0	External inter Clear to disab Set to enable	rupt 0 Enable le external int external inter	e bit errupt 0. rupt 0.					

Reset Value = 0X00 0000b Bit addressable





Table 13. IP RegisterIP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0			
-	-	PT2	PS	PT1	PX1	PT0	PX0			
Bit Number	Bit Mnemonic	Descriptio	Description							
7	-	Reserved The value	Reserved The value read from this bit is indeterminate. Do not set this bit.							
6	-	Reserved The value	Reserved The value read from this bit is indeterminate. Do not set this bit.							
5	PT2	Timer 2 ov Refer to PT	Timer 2 overflow interrupt Priority bit Refer to PT2H for priority level.							
4	PS	Serial port	Serial port Priority bit Refer to PSH for priority level.							
3	PT1	Timer 1 ov Refer to PT	Timer 1 overflow interrupt Priority bit Refer to PT1H for priority level.							
2	PX1	External in Refer to P	External interrupt 1 Priority bit Refer to PX1H for priority level.							
1	PT0	Timer 0 ov Refer to PT	Timer 0 overflow interrupt Priority bit Refer to PT0H for priority level.							
0	PX0	External in Refer to P	nterrupt 0 Pri (0H for priorit	i ority bit y level.						

Reset Value = XX00 0000b Bit addressable

Table 14.IPH RegisterIPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	-	PT2H	PSH	PT1H	PX1H	РТОН	PX0H
Bit Number	Bit Mnemonic	Description					
7	-	Reserved The value rea	d from this bit	is indetermina	ate. Do not se	t this bit.	
6	-	Reserved The value rea	d from this bit	is indetermina	ate. Do not se	t this bit.	
5	PT2H	Timer 2 over PT2H PT2 0 0 1 0 1 1	flow interrup Priority Leve Lowest Highest	t Priority Higl _임	ı bit		
4	PSH	Serial port P PSH PS 0 0 1 0 1 1	riority High b <u>Priority Leve</u> Lowest Highest	it el			
3	PT1H	Timer 1 over PT1H PT1 0 0 1 0 1 1	flow interrupt Priority Leve Lowest Highest	t Priority Higl ગ	ו bit		
2	PX1H	External inte PX1H PX1 0 0 0 1 1 0 1 1	rrupt 1 Priori <u>Priority Leve</u> Lowest Highest	ty High bit 한			
1	РТОН	Timer 0 over PTOH PTO 0 0 1 0 1 1	flow interrup Priority Leve Lowest Highest	t Priority Higl <u>위</u>	ı bit		
0	РХОН	External inte PXOH PXO 0 0 0 1 1 0 1 1	rrupt 0 Priori Priority Leve Lowest Highest	ty High bit 1			

Reset Value = XX00 0000b Not bit addressable



	®
Idle mode	An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is pre- served in its entirely : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.
	There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.
	The flag bits GF0 and GF1 can be used to give an indication if an interrupt occured dur- ing normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.
	The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.
Power-down Mode	To save maximum power, a power-down mode can be invoked by software (Refer to Table 10., PCON register).
	In power-down mode, the oscillator is stopped and the instruction that invoked power- down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power- down. To properly terminate power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.
	Only external interrupts INTO and INT1 are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input. Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 10. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.
	Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C52X2 into power-down mode.
Figure 10. Power-down Exit Wa	aveform

MEI



Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

Note: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data ⁽¹⁾	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data ⁽¹⁾	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

Table 15. The State of Ports During Idle and Power-down Modes

Note: 1. Port 0 can force a "zero" level. A "one" will leave port floating.





EPROM Structure The TS87C52X2 is divided in two different arrays:

- the code array: 8 Kbytes
- the encryption array: 64 bytes

In addition a third non programmable array is implemented:

the signature array: 4 bytes

EPROM Lock System The program Lock system, when programmed, protects the on-chip program against software piracy.

Encryption Array Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

Program Lock Bits The three lock bits, when programmed according to Table 1., will provide different level of protection for the on-chip code and data.

Pr	ogram Lo	ock Bits		
Security level	LB1	LB2	LB3	Protection Description
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	Ρ	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, \overline{EA} is sampled and latched on reset, and further programming of the EPROM is disabled.
3	U	Р	U	Same as 2, also verify is disabled.
4	U	U	Р	Same as 3, also external execution is disabled.

U: unprogrammed P: programmed

WARNING: Security level 2 and 3 should only be programmed after EPROM and Core verification.

Signature Bytes The TS80/87C52X2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 9.

EPROM Programming

Set-up modes

In order to program and verify the EPROM or to read the signature bytes, the TS87C52X2 is placed in specific set-up modes (See Figure 11.).



Electrical Characteristics

Absolute Maximum Ratings⁽¹⁾

Ambiant Temperature Under Bias:	
C = commercial	0°C to 70°C
I = industrial	40°C to 85°C
Storage Temperature	65°C to + 150°C
Voltage on V _{CC} to V _{SS}	0.5V to + 7 V
Voltage on V _{PP} to V _{SS}	0.5V to + 13 V
Voltage on Any Pin to V _{SS}	0.5V to V _{CC} + 0.5V
Power Dissipation	1 W ⁽²⁾
·	
Storage Temperature	$\begin{array}{l} -65^{\circ}\text{C to} + 150^{\circ}\text{C} \\0.5\text{V to} + 7 \text{ V} \\0.5\text{V to} + 13 \text{ V} \\0.5\text{V to} \text{ V}_{\text{CC}} + 0.5\text{V} \\1 \text{ W}^{(2)} \end{array}$

- Notes: 1. Stresses at or above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
 - 2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

Power Consumption Measurement Since the introduction of the first C51 devices, every manufacturer made operating lcc measurements under reset, which made sense for the designs were the CPU was running under reset. In Atmel new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That's why, while keeping measurements under Reset, Atmel presents a new way to measure the operating lcc:

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = Vcc, RST = Vss, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating Icc.

DC Parameters for	TA = 0°C to +70°C; V_{SS} = 0 V; V_{CC} = 5V ± 10%; F = 0 to 40 MHz.
Standard Voltage	TA = -40°C to +85°C; $V_{SS} = 0 V$; $V_{CC} = 5V \pm 10\%$; F = 0 to 40 MHz.

Table 22.	DC Parameters	in	Standard	Voltage
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Symbol	Parameter	Min	Тур	Мах	Unit	Test Conditions
V _{IL}	Input Low Voltage	-0.5		0.2 V _{CC} - 0.1	V	
V _{IH}	Input High Voltage except XTAL1, RST	0.2 V _{CC} + 0.9		V _{CC} + 0.5	V	
V _{IH1}	Input High Voltage, XTAL1, RST	0.7 V _{CC}		V _{CC} + 0.5	V	
V _{OL}	Output Low Voltage, ports 1, 2, 3 ⁽⁶⁾			0.3 0.45 1.0	V V V	$\begin{split} I_{OL} &= 100 \; \mu A^{(4)} \\ I_{OL} &= 1.6 \; m A^{(4)} \\ I_{OL} &= 3.5 \; m A^{(4)} \end{split}$
V _{OL1}	Output Low Voltage, port 0 ⁽⁶⁾			0.3 0.45 1.0	V V V	$I_{OL} = 200 \ \mu A^{(4)}$ $I_{OL} = 3.2 \ m A^{(4)}$ $I_{OL} = 7.0 \ m A^{(4)}$
V _{OL2}	Output Low Voltage, ALE, PSEN			0.3 0.45 1.0	V V V	$I_{OL} = 100 \ \mu A^{(4)}$ $I_{OL} = 1.6 \ m A^{(4)}$ $I_{OL} = 3.5 \ m A^{(4)}$

TS8xCx2X2

Port 0: 26 mA Ports 1, 2 and 3: 15 mA Maximum total I_{OL} for all output pins: 71 mA If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

- 7. For other values, please contact your sales office.
- Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 17.), V_{IL} = V_{SS} + 0.5V,

 $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; $\overline{EA} = Port 0 = V_{CC}$; RST = V_{SS} . The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.

Figure 13. I_{CC} Test Condition, under reset



All other pins are disconnected.





All other pins are disconnected.

Figure 15. I_{CC} Test Condition, Idle Mode



All other pins are disconnected.



Table 28., Table 31. and Table 34. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

Table 25. Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20 40		30 30		20
T (ns)	25	50	25	33.3	33.3	50

Example:

 T_{LLIV} in X2 mode for a -V part at 20 MHz (T = 1/20^{E6} = 50 ns):

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x= 22 (Table 28.)
```

T= 50ns

T_{LLIV}= 2T - x = 2 x 50 - 22 = 78ns

External Program Memory Characteristics

Table 26. Symbol Description

Symbol	Parameter
Т	Oscillator clock period
T _{LHLL}	ALE pulse width
T _{AVLL}	Address Valid to ALE
T _{LLAX}	Address Hold After ALE
T _{LLIV}	ALE to Valid Instruction In
T _{LLPL}	ALE to PSEN
T _{PLPH}	PSEN Pulse Width
T _{PLIV}	PSEN to Valid Instruction In
T _{PXIX}	Input Instruction Hold After PSEN
T _{PXIZ}	Input Instruction FloatAfter PSEN
T _{PXAV}	PSEN to Address Valid
T _{AVIV}	Address to Valid Instruction In
T _{PLAZ}	PSEN Low to Address Float





Table 27. AC Parameters for Fix Clock	
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Speed	-M 40 MHz		-V -V X2 mode standard 30 MHz mode 40 -M 60 MHz MHz 40 MHz equiv.		V dard le 40 Hz	-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Т	25		33		25		50		33		ns
T _{LHLL}	40		25		42		35		52		ns
T _{AVLL}	10		4		12		5		13		ns
T _{LLAX}	10		4		12		5		13		ns
T _{LLIV}		70		45		78		65		98	ns
T _{LLPL}	15		9		17		10		18		ns
T _{PLPH}	55		35		60		50		75		ns
T _{PLIV}		35		25		50		30		55	ns
T _{PXIX}	0		0		0		0		0		ns
T _{PXIZ}		18		12		20		10		18	ns
T _{AVIV}		85		53		95		80		122	ns
T _{PLAZ}		10		10		10		10		10	ns

Table 28. AC Parameters for a Variable Clock: derating formula

Symbol	Туре	Standard Clock	X2 Clock	-М	-V	-L	Units
T _{LHLL}	Min	2 T - x	T - x	10	8	15	ns
T _{AVLL}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLAX}	Min	T - x	0.5 T - x	15	13	20	ns
T _{LLIV}	Max	4 T - x	2 T - x	30	22	35	ns
T _{LLPL}	Min	T - x	0.5 T - x	10	8	15	ns
T _{PLPH}	Min	3 T - x	1.5 T - x	20	15	25	ns
T _{PLIV}	Max	3 T - x	1.5 T - x	40	25	45	ns
T _{PXIX}	Min	х	х	0	0	0	ns
T _{PXIZ}	Max	T - x	0.5 T - x	7	5	15	ns
T _{AVIV}	Max	5 T - x	2.5 T - x	40	30	45	ns
T _{PLAZ}	Max	x	x	10	10	10	ns



Table 30.	AC Parameters	for a	Fix	Clock
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Speed	-M 40 MHz		-M 40 MHz		-V X2 mode 30 MHz -M 60 MHz 0 MHz equiv.		'- stan mod Mi	-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz	
Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
T _{RLRH}	130		85		135		125		175		ns		
T _{WLWH}	130		85		135		125		175		ns		
T _{RLDV}		100		60		102		95		137	ns		
T _{RHDX}	0		0		0		0		0		ns		
T _{RHDZ}		30		18		35		25		42	ns		
T _{LLDV}		160		98		165		155		222	ns		
T _{AVDV}		165		100		175		160		235	ns		
T _{LLWL}	50	100	30	70	55	95	45	105	70	130	ns		
T _{AVWL}	75		47		80		70		103		ns		
T _{QVWX}	10		7		15		5		13		ns		
T _{QVWH}	160		107		165		155		213		ns		
T _{WHQX}	15		9		17		10		18		ns		
T _{RLAZ}		0		0		0		0		0	ns		
T _{WHLH}	10	40	7	27	15	35	5	45	13	53	ns		

Symbol	Туре	Standard Clock	X2 Clock	-М	-V	-L	Units
T _{RLRH}	Min	6 T - x	3 T - x	20	15	25	ns
T _{WLWH}	Min	6 T - x	3 T - x	20	15	25	ns
T _{RLDV}	Max	5 T - x	2.5 T - x	25	23	30	ns
T _{RHDX}	Min	х	х	0	0	0	ns
T _{RHDZ}	Max	2 T - x	T - x	20	15	25	ns
T _{LLDV}	Max	8 T - x	4T -x	40	35	45	ns
T _{AVDV}	Max	9 T - x	4.5 T - x	60	50	65	ns
T _{LLWL}	Min	3 T - x	1.5 T - x	25	20	30	ns
T _{LLWL}	Max	3 T + x	1.5 T + x	25	20	30	ns
T _{AVWL}	Min	4 T - x	2 T - x	25	20	30	ns
T _{QVWX}	Min	T - x	0.5 T - x	15	10	20	ns
T _{QVWH}	Min	7 T - x	3.5 T - x	15	10	20	ns
T _{WHQX}	Min	T - x	0.5 T - x	10	8	15	ns
T _{RLAZ}	Max	х	х	0	0	0	ns
T _{WHLH}	Min	T - x	0.5 T - x	15	10	20	ns
T _{WHLH}	Max	T + x	0.5 T + x	15	10	20	ns

Table 31. AC Parameters for a Variable Clock: Derating Formula

External Data Memory Write Cycle







EPROM Programming and Verification Characteristics

 T_A = 21°C to 27°C; V_{SS} = 0V; $~V_{CC}$ = 5V \pm 10% while programming. V_{CC} = operating range while verifying.

 Table 35.
 EPROM Programming Parameters

Symbol	Parameter	Min	Max	Units
V _{PP}	Programming Supply Voltage	12.5	13	V
I _{PP}	Programming Supply Current		75	mA
1/T _{CLCL}	Oscillator Frquency	4	6	MHz
T _{AVGL}	Address Setup to PROG Low	48 T _{CLCL}		
T _{GHAX}	Adress Hold after PROG	48 T _{CLCL}		
T _{DVGL}	Data Setup to PROG Low	48 T _{CLCL}		
T _{GHDX}	Data Hold after PROG	48 T _{CLCL}		
T _{EHSH}	(Enable) High to V _{PP}	48 T _{CLCL}		
T _{SHGL}	V _{PP} Setup to PROG Low	10		μs
T _{GHSL}	V _{PP} Hold after PROG	10		μs
T _{GLGH}	PROG Width	90	110	μs
T _{AVQV}	Address to Valid Data		48 T _{CLCL}	
T _{ELQV}	ENABLE Low to Data Valid		48 T _{CLCL}	
T _{EHQZ}	Data Float after ENABLE	0	48 T _{CLCL}	

EPROM Programming and Verification Waveforms

Figure 22. EPROM Programming and Verification Waveforms



* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

Ordering Information

Table 37. Possible Ordering Entries

Part Number ⁽³⁾	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS80C32X2-MCA	ROMLess	5V <u>±</u> 10%	Commercial	40 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-MCB	ROMLess	5V <u>±</u> 10%	Commercial	40 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-MCC	ROMLess	5V <u>±</u> 10%	Commercial	40 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-MCE	ROMLess	5V <u>±</u> 10%	Commercial	40 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-LCA	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-LCB	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-LCC	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-LCE	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-VCA	ROMLess	5V <u>±</u> 10%	Commercial	60 MHz ⁽³⁾	PDIL40	Stick
TS80C32X2-VCB	ROMLess	5V <u>±</u> 10%	Commercial	60 MHz ⁽³⁾	PLCC44	Stick
TS80C32X2-VCC	ROMLess	5V <u>±</u> 10%	Commercial	60 MHz ⁽³⁾	PQFP44	Tray
TS80C32X2-VCE	ROMLess	5V <u>±</u> 10%	Commercial	60 MHz ⁽³⁾	VQFP44	Tray
TS80C32X2-MIA	ROMLess	5V <u>±</u> 10%	Industrial	40 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-MIB	ROMLess	5V <u>±</u> 10%	Industrial	40 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-MIC	ROMLess	5V <u>±</u> 10%	Industrial	40 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-MIE	ROMLess	5V <u>±</u> 10%	Industrial	40 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-LIA	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-LIB	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-LIC	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-LIE	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-VIA	ROMLess	5V <u>±</u> 10%	Industrial	60 MHz ⁽³⁾	PDIL40	Stick
TS80C32X2-VIB	ROMLess	5V <u>±</u> 10%	Industrial	60 MHz ⁽³⁾	PLCC44	Stick
TS80C32X2-VIC	ROMLess	5V <u>±</u> 10%	Industrial	60 MHz ⁽³⁾	PQFP44	Tray
TS80C32X2-VIE	ROMLess	5V <u>±</u> 10%	Industrial	60 MHz ⁽³⁾	VQFP44	Tray
AT80C32X2-3CSUM	ROMLess	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	PDIL40	Stick
AT80C32X2-SLSUM	ROMLess	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	PLCC44	Stick
AT80C32X2-RLTUM	ROMLess	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	VQFP44	Tray
AT80C32X2-RLTUM	ROMLess	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	VQFP44	Tape & Reel
AT80C32X2-3CSUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PDIL40	Stick
AT80C32X2-SLSUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PLCC44	Stick





Table 37. Possible Ordering Entries (Continued)

			Tomporatura			
Part Number ⁽³⁾	Memory Size	Supply Voltage	Range	Max Frequency	Package	Packing
AT80C32X2-RLTUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	VQFP44	Tray
AT80C32X2-3CSUV	ROMLess	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	PDIL40	Stick
AT80C32X2-SLSUV	ROMLess	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	PLCC44	Stick
AT80C32X2-RLTUV	ROMLess	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	VQFP44	Tray
TS80C52X2zzz-MCA	8K ROM	2.7 to 5.5V	Commercial	40 MHz ⁽¹⁾	PDIL40	Stick
TS80C52X2zzz-MCB	8K ROM	2.7 to 5.5V	Commercial	40 MHz ⁽¹⁾	PLCC44	Stick
TS80C52X2zzz-MCC	8K ROM	2.7 to 5.5V	Commercial	40 MHz ⁽¹⁾	PQFP44	Tray
TS80C52X2zzz-MCE	8K ROM	2.7 to 5.5V	Commercial	40 MHz ⁽¹⁾	VQFP44	Tray
TS80C52X2zzz-LCA	8K ROM	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PDIL40	Stick
TS80C52X2zzz-LCB	8K ROM	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PLCC44	Stick
TS80C52X2zzz-LCC	8K ROM	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PQFP44	Tray
TS80C52X2zzz-LCE	8K ROM	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	VQFP44	Tray
TS80C52X2zzz-VCA	8K ROM	5V <u>±</u> 10%	Commercial	60 MHz ⁽³⁾	PDIL40	Stick
TS80C52X2zzz-VCB	8K ROM	5V ±10%	Commercial	60 MHz ⁽³⁾	PLCC44	Stick
TS80C52X2zzz-VCC	8K ROM	5V ±10%	Commercial	60 MHz ⁽³⁾	PQFP44	Tray
TS80C52X2zzz-VCE	8K ROM	5V ±10%	Commercial	60 MHz ⁽³⁾	VQFP44	Tray
TS80C52X2zzz-MIA	8K ROM	5V ±10%	Industrial	40 MHz ⁽¹⁾	PDIL40	Stick
TS80C52X2zzz-MIB	8K ROM	5V ±10%	Industrial	40 MHz ⁽¹⁾	PLCC44	Stick
TS80C52X2zzz-MIC	8K ROM	5V ±10%	Industrial	40 MHz ⁽¹⁾	PQFP44	Tray
TS80C52X2zzz-MIE	8K ROM	5V ±10%	Industrial	40 MHz ⁽¹⁾	VQFP44	Tray
TS80C52X2zzz-LIA	8K ROM	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PDIL40	Stick
TS80C52X2zzz-LIB	8K ROM	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PLCC44	Stick
TS80C52X2zzz-LIC	8K ROM	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PQFP44	Tray
TS80C52X2zzz-LIE	8K ROM	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	VQFP44	Tray
TS80C52X2zzz-VIA	8K ROM	5V ±10%	Industrial	60 MHz ⁽³⁾	PDIL40	Stick
TS80C52X2zzz-VIB	8K ROM	5V ±10%	Industrial	60 MHz ⁽³⁾	PLCC44	Stick
TS80C52X2zzz-VIC	8K ROM	5V ±10%	Industrial	60 MHz ⁽³⁾	PQFP44	Tray
TS80C52X2zzz-VIE	8K ROM	5V ±10%	Industrial	60 MHz ⁽³⁾	VQFP44	Tray
AT80C52X2zzz-3CSUM	8K ROM	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	PDIL40	Stick
AT80C52X2zzz-SLSUM	8K ROM	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	PLCC44	Stick
AT80C52X2zzz-RLTUM	8K ROM	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	VQFP44	Tray