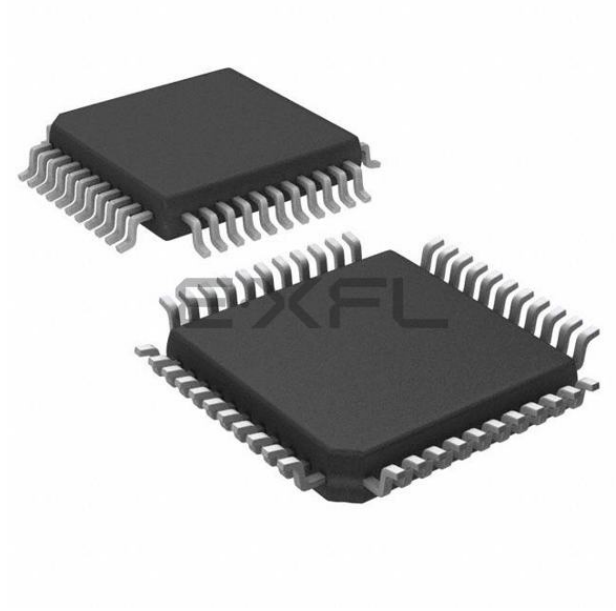


**Welcome to E-XFL.COM**

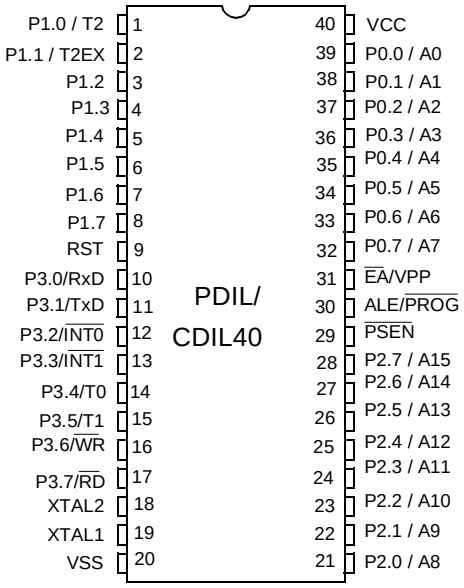
## What is "Embedded - Microcontrollers"?

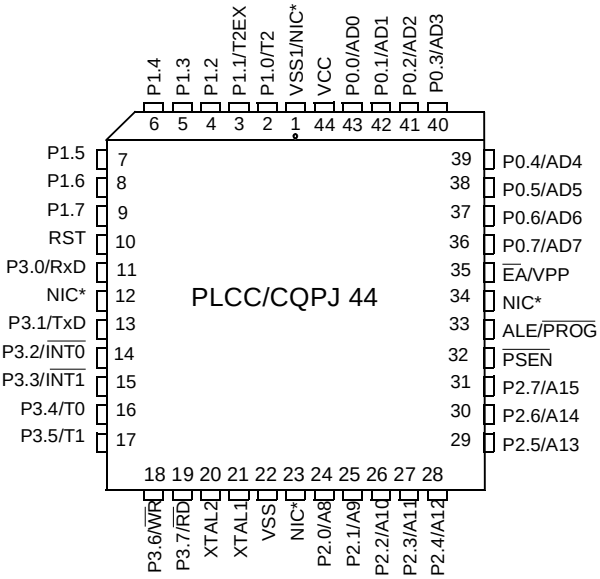
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

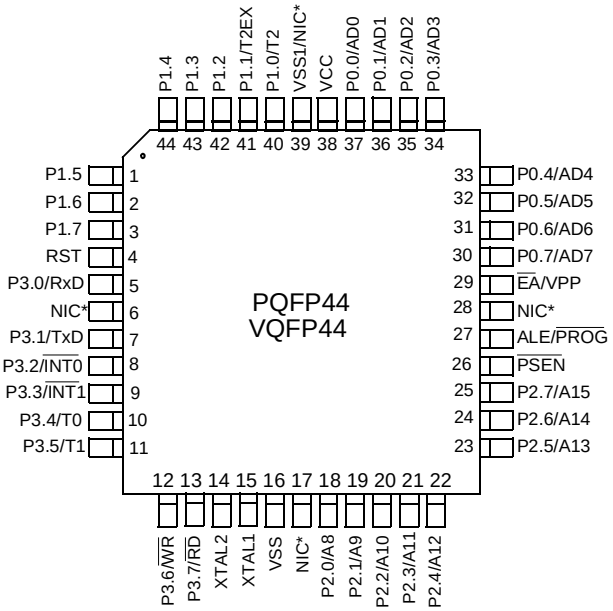
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | 80C51 |
| Core Size | 8-Bit |
| Speed | 40/20MHz |
| Connectivity | UART/USART |
| Peripherals | POR |
| Number of I/O | 32 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | OTP |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 4.5V ~ 5.5V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-QFP |
| Supplier Device Package | 44-VQFP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/ts87c52x2-mce |

## Pin Configuration



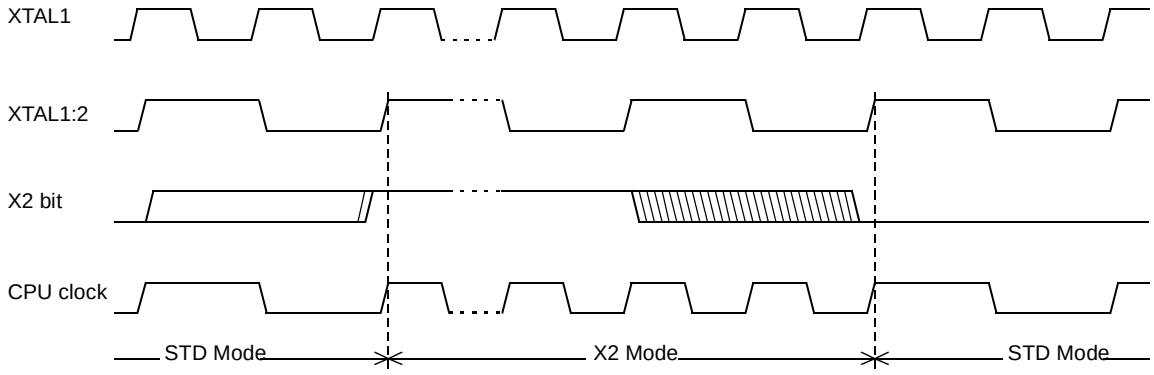




*NIC: No Internal Connection

| Mnemonic | Pin Number | | | Type | Name and Function |
|---|---|---|---|---|---|
| | DIL | LCC | VQFP 1.4 | | |
| $V_{SS}$ | 20 | 22 | 16 | I | **Ground:** 0V reference |
| Vss1 | | 1 | 39 | I | Optional Ground: **Contact the Sales Office for ground connection.** |
| $V_{CC}$ | 40 | 44 | 38 | I | **Power Supply:** This is the power supply voltage for normal, idle and power-down operation |
| P0.0-P0.7 | 39-32 | 43-36 | 37-30 | I/O | **Port 0**: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high impedance inputs.Port 0 pins must be polarized to Vcc or Vss in order to prevent any parasitic current consumption. Port 0 is also the multiplexed low-order address and data bus during access to external program and data memory. In this application, it uses strong internal pull-up when emitting 1s. Port 0 also inputs the code bytes during EPROM programming. External pull-ups are required during program verification during which P0 outputs the code bytes. |
| | | | | | |
| P1.0-P1.7 | 1-8 | 2-9 | 40-44 1-3 | I/O | Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally pulled low will source current because of the internal pull-ups. Port 1 also receives the low-order address byte during memory programming and verification.<br>Alternate functions for Port 1 include: |
| | | | | | |
| | 1 | 2 | 40 | I/O | **T2 (P1.0):** Timer/Counter 2 external count input/Clockout |
| | 2 | 3 | 41 | I | **T2EX (P1.1):** Timer/Counter 2 Reload/Capture/Direction Control |
| P2.0-P2.7 | 21-28 | 24-31 | 18-25 | I/O | **Port 2**: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally pulled low will source current because of the internal pull-ups. Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX atDPTR).In this application, it uses strong internal pull-ups emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX atRi), port 2 emits the contents of the P2 SFR. Some Port 2 pins receive the high order address bits during EPROM programming and verification: P2.0 to P2.4 |
| | | | | | |
| P3.0-P3.7 | 10-17 | 11, 13-19 | 5, 7-13 | I/O | Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally pulled low will source current because of the internal pull-ups. Port 3 also serves the special features of the 80C51 family, as listed below. |
| | | | | | |
| | 10 | 11 | 5 | I | **RXD (P3.0):** Serial input port |
| | 11 | 13 | 7 | O | **TXD (P3.1):** Serial output port |
| | 12 | 14 | 8 | I | **$\overline{\text{INT0}}$ (P3.2):** External interrupt 0 |

**Figure 2.** Mode Switching Waveforms




The X2 bit in the CKCON register (See Table 3.) allows to switch from 12 clock cycles per instruction to 6 clock cycles and vice versa. At reset, the standard speed is activated (STD mode). Setting this bit activates the X2 feature (X2 mode).

Note: In order to prevent any incorrect operation while operating in X2 mode, user must be aware that all peripherals using clock frequency as time reference (UART, timers) will have their time reference divided by two. For example a free running timer generating an interrupt every 20 ms will then generate an interrupt every 10 ms. UART with 4800 baud rate will have 9600 baud rate.

**Table 3.** CKCON Register

CKCON - Clock Control Register (8Fh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | - | - | - | - | X2 |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 4 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 3 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 2 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 1 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 0 | X2 | **CPU and peripheral clock bit**<br>Clear to select 12 clock periods per machine cycle (STD mode, $F_{OSC}=F_{XTAL}/2$).<br>Set to select 6 clock periods per machine cycle (X2 mode, $F_{OSC}=F_{XTAL}$). |

Reset Value = XXXX XXX0b

Not bit addressable

For further details on the X2 feature, please refer to ANM072 available on the web (http://www.atmel.com)

## Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.

ASSEMBLY LANGUAGE

```
; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2    AUXR1 EQU 0A2H
;
0000 909000MOV DPTR,#SOURCE ; address of SOURCE
0003 05A2 INC AUXR1 ; switch data pointers
0005 90A000 MOV DPTR,#DEST ; address of DEST
0008    LOOP:
0008 05A2 INC AUXR1 ; switch data pointers
000A E0 MOVX A,atDPTR ; get a byte from SOURCE
000B A3 INC DPTR ; increment SOURCE address
000C 05A2 INC AUXR1 ; switch data pointers
000E F0 MOVX atDPTR,A ; write the byte to DEST
000F A3 INC DPTR ; increment DEST address
0010 70F6JNZ LOOP ; check for 0 terminator
0012 05A2 INC AUXR1 ; (optional) restore DPS
```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

## Timer 2

The timer 2 in the TS80C52X2 is compatible with the timer 2 in the 80C52.
It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 5) and T2MOD register (See Table 6). Timer 2 operation is similar to Timer 0 and Timer 1. C/$\overline{T2}$ selects $F_{OSC}/12$ (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/$\overline{RL2}$ (T2CON), as described in the Atmel 8-bit Microcontroller Hardware description.

Refer to the Atmel 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C52X2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

### Auto-reload Mode

The Auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 4. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.

**Table 14.** IPH Register

IPH - Interrupt Priority High Register (B7h)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | PT2H | PSH | PT1H | PX1H | PT0H | PX0H |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | PT2H | **Timer 2 overflow interrupt Priority High bit**<br>PT2H PT2 Priority Level<br>0 0 Lowest<br>0 1<br>1 0<br>1 1 Highest |
| 4 | PSH | **Serial port Priority High bit**<br>PSH PS Priority Level<br>0 0 Lowest<br>0 1<br>1 0<br>1 1 Highest |
| 3 | PT1H | **Timer 1 overflow interrupt Priority High bit**<br>PT1H PT1 Priority Level<br>0 0 Lowest<br>0 1<br>1 0<br>1 1 Highest |
| 2 | PX1H | **External interrupt 1 Priority High bit**<br>PX1H PX1 Priority Level<br>0 0 Lowest<br>0 1<br>1 0<br>1 1 Highest |
| 1 | PT0H | **Timer 0 overflow interrupt Priority High bit**<br>PT0H PT0 Priority Level<br>0 0 Lowest<br>0 1<br>1 0<br>1 1 Highest |
| 0 | PX0H | **External interrupt 0 Priority High bit**<br>PX0H PX0 Priority Level<br>0 0 Lowest<br>0 1<br>1 0<br>1 1 Highest |

Reset Value = XX00 0000b

Not bit addressable

Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does no affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

Note: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

**Table 15.** The State of Ports During Idle and Power-down Modes

| Mode | Program Memory | ALE | PSEN | PORT0 | PORT1 | PORT2 | PORT3 |
|---|---|---|---|---|---|---|---|
| Idle | Internal | 1 | 1 | Port Data(1) | Port Data | Port Data | Port Data |
| Idle | External | 1 | 1 | Floating | Port Data | Address | Port Data |
| Power Down | Internal | 0 | 0 | Port Data(1) | Port Data | Port Data | Port Data |
| Power Down | External | 0 | 0 | Floating | Port Data | Port Data | Port Data |

Note: 1. Port 0 can force a "zero" level. A "one" will leave port floating.

## ONCE™ Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS80C52X2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C52X2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and $\overline{\text{PSEN}}$ is high.
- Hold ALE low as RST is deactivated.

While the TS80C52X2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 26. shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

**Table 16.** External Pin Status during ONCE Mode

| ALE | PSEN | Port 0 | Port 1 | Port 2 | Port 3 | XTAL1/2 |
|---|---|---|---|---|---|---|
| Weak pull-up | Weak pull-up | Float | Weak pull-up | Weak pull-up | Weak pull-up | Active |

## Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

**Table 18.** AUXR Register

AUXR - Auxiliary Register (8Eh)

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| - | - | - | - | - | - | - | AO |

| Bit Number | Bit Mnemonic | Description |
|---|---|---|
| 7 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 6 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 5 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 4 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 3 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 2 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 1 | - | **Reserved**<br>The value read from this bit is indeterminate. Do not set this bit. |
| 0 | AO | **ALE Output bit**<br>Clear to restore ALE operation during internal fetches.<br>Set to disable ALE operation during internal fetches. |

Reset Value = XXXX XXX0b

Not bit addressable

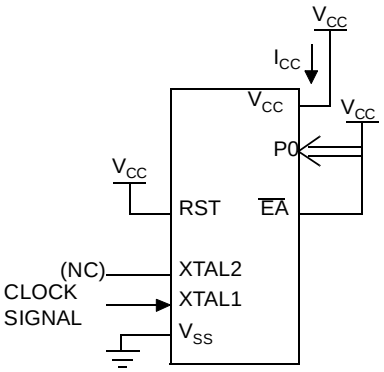
**Table 22.** DC Parameters in Standard Voltage (Continued)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage, ports 1, 2, 3 | $V_{CC}$ - 0.3<br>$V_{CC}$ - 0.7<br>$V_{CC}$ - 1.5 | | | V<br>V<br>V | $I_{OH}$ = -10 µA<br>$I_{OH}$ = -30 µA<br>$I_{OH}$ = -60 µA<br>$V_{CC}$ = 5V ± 10% |
| $V_{OH1}$ | Output High Voltage, port 0 | $V_{CC}$ - 0.3<br>$V_{CC}$ - 0.7<br>$V_{CC}$ - 1.5 | | | V<br>V<br>V | $I_{OH}$ = -200 µA<br>$I_{OH}$ = -3.2 mA<br>$I_{OH}$ = -7.0 mA<br>$V_{CC}$ = 5V ± 10% |
| $V_{OH2}$ | Output High Voltage,ALE, $\overline{PSEN}$ | $V_{CC}$ - 0.3<br>$V_{CC}$ - 0.7<br>$V_{CC}$ - 1.5 | | | V<br>V<br>V | $I_{OH}$ = -100 µA<br>$I_{OH}$ = -1.6 mA<br>$I_{OH}$ = -3.5 mA<br>$V_{CC}$ = 5V ± 10% |
| $R_{RST}$ | RST Pulldown Resistor | 50 | 90 (5) | 200 | kΩ | |
| $I_{IL}$ | Logical 0 Input Current ports 1, 2 and 3 | | | -50 | µA | Vin = 0.45V |
| $I_{LI}$ | Input Leakage Current | | | ±10 | µA | 0.45V < Vin < $V_{CC}$ |
| $I_{TL}$ | Logical 1 to 0 Transition Current, ports 1, 2, 3 | | | -650 | µA | Vin = 2.0 V |
| $C_{IO}$ | Capacitance of I/O Buffer | | | 10 | pF | Fc = 1 MHz<br>$T_A$ = 25°C |
| $I_{PD}$ | Power Down Current | | 20 (5) | 50 | µA | 2.0 V < $V_{CC}$ < 5.5V(3) |
| $I_{CC}$ under RESET | Power Supply Current Maximum values, X1 mode: (7) | | | 1 + 0.4 Freq (MHz)<br>at12MHz 5.8<br>at16MHz 7.4 | mA | $V_{CC}$ = 5.5V(1) |
| $I_{CC}$ operating | Power Supply Current Maximum values, X1 mode: (7) | | | 3 + 0.6 Freq (MHz)<br>at12MHz 10.2<br>at16MHz 12.6 | mA | $V_{CC}$ = 5.5V(8) |
| $I_{CC}$ idle | Power Supply Current Maximum values, X1 mode: (7) | | | 0.25+0.3 Freq (MHz)<br>at12MHz 3.9<br>at16MHz 5.1 | mA | $V_{CC}$ = 5.5V(2) |

Port 0: 26 mA
Ports 1, 2 and 3: 15 mA
Maximum total $I_{OL}$ for all output pins: 71 mA
If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

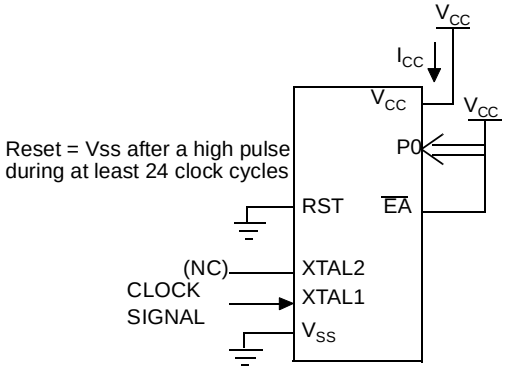
7. For other values, please contact your sales office.
8. Operating $I_{CC}$ is measured with all output pins disconnected; XTAL1 driven with $T_{CLCH}$, $T_{CHCL}$ = 5 ns (see Figure 17.), $V_{IL}$ = $V_{SS}$ + 0.5V,
$V_{IH}$ = $V_{CC}$ - 0.5V; XTAL2 N.C.; $\overline{EA}$ = Port 0 = $V_{CC}$; RST = $V_{SS}$. The internal ROM runs the code 80 FE (label: SJMP label). $I_{CC}$ would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.

**Figure 13.** $I_{CC}$ Test Condition, under reset



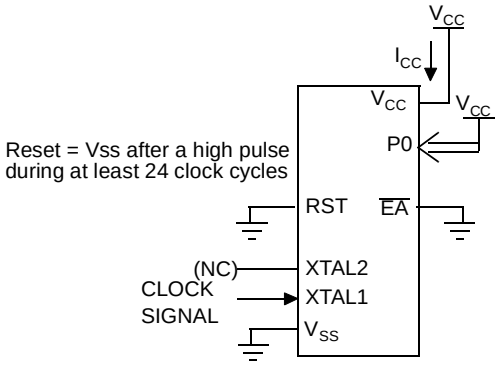

All other pins are disconnected.

**Figure 14.** Operating $I_{CC}$ Test Condition




All other pins are disconnected.

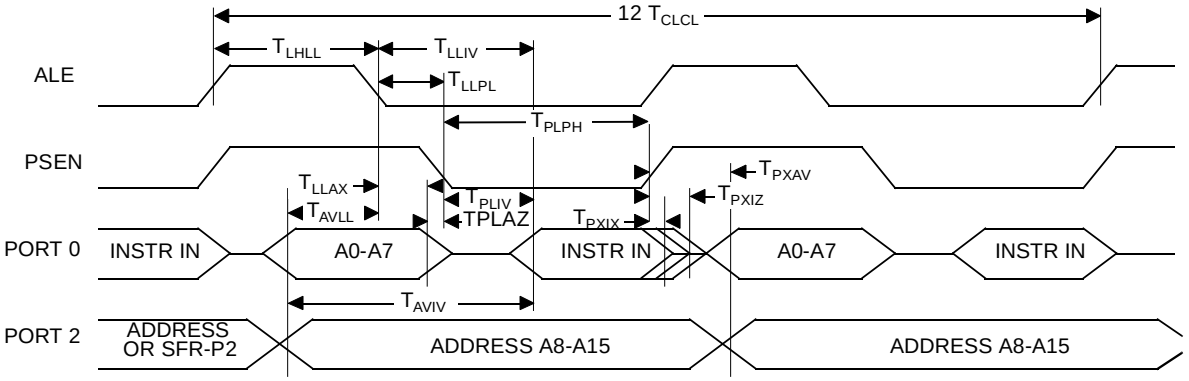
**Figure 15.** $I_{CC}$ Test Condition, Idle Mode




All other pins are disconnected.

### External Program Memory Read Cycle

**Figure 18.** External Program Memory Read Cycle




### External Data Memory Characteristics

**Table 29.** Symbol Description

| Symbol | Parameter |
|---|---|
| $T_{RLRH}$ | $\overline{RD}$ Pulse Width |
| $T_{WLWH}$ | $\overline{WR}$ Pulse Width |
| $T_{RLDV}$ | $\overline{RD}$ to Valid Data In |
| $T_{RHDX}$ | Data Hold After $\overline{RD}$ |
| $T_{RHDZ}$ | Data Float After $\overline{RD}$ |
| $T_{LLDV}$ | ALE to Valid Data In |
| $T_{AVDV}$ | Address to Valid Data In |
| $T_{LLWL}$ | ALE to $\overline{WR}$ or $\overline{RD}$ |
| $T_{AVWL}$ | Address to $\overline{WR}$ or $\overline{RD}$ |
| $T_{QVWX}$ | Data Valid to $\overline{WR}$ Transition |
| $T_{QVWH}$ | Data set-up to $\overline{WR}$ High |
| $T_{WHQX}$ | Data Hold After $\overline{WR}$ |
| $T_{RLAZ}$ | $\overline{RD}$ Low to Address Float |
| $T_{WHLH}$ | $\overline{RD}$ or $\overline{WR}$ High to ALE high |

**Table 30.** AC Parameters for a Fix Clock

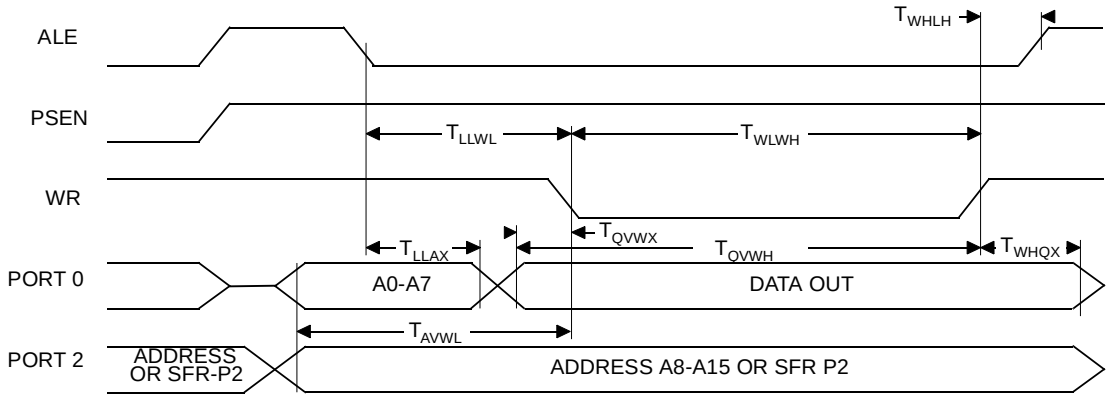
| Speed | -M 40 MHz | | -V X2 mode 30 MHz 60 MHz equiv. | | -V standard mode 40 MHz | | -L X2 mode 20 MHz 40 MHz equiv. | | -L standard mode 30 MHz | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | |
| $T_{RLRH}$ | 130 | | 85 | | 135 | | 125 | | 175 | | ns |
| $T_{WLWH}$ | 130 | | 85 | | 135 | | 125 | | 175 | | ns |
| $T_{RLDV}$ | | 100 | | 60 | | 102 | | 95 | | 137 | ns |
| $T_{RHDX}$ | 0 | | 0 | | 0 | | 0 | | 0 | | ns |
| $T_{RHDZ}$ | | 30 | | 18 | | 35 | | 25 | | 42 | ns |
| $T_{LLDV}$ | | 160 | | 98 | | 165 | | 155 | | 222 | ns |
| $T_{AVDV}$ | | 165 | | 100 | | 175 | | 160 | | 235 | ns |
| $T_{LLWL}$ | 50 | 100 | 30 | 70 | 55 | 95 | 45 | 105 | 70 | 130 | ns |
| $T_{AVWL}$ | 75 | | 47 | | 80 | | 70 | | 103 | | ns |
| $T_{QVWX}$ | 10 | | 7 | | 15 | | 5 | | 13 | | ns |
| $T_{QVWH}$ | 160 | | 107 | | 165 | | 155 | | 213 | | ns |
| $T_{WHQX}$ | 15 | | 9 | | 17 | | 10 | | 18 | | ns |
| $T_{RLAZ}$ | | 0 | | 0 | | 0 | | 0 | | 0 | ns |
| $T_{WHLH}$ | 10 | 40 | 7 | 27 | 15 | 35 | 5 | 45 | 13 | 53 | ns |

**Table 31.** AC Parameters for a Variable Clock: Derating Formula

| Symbol | Type | Standard Clock | X2 Clock | -M | -V | -L | Units |
|---|---|---|---|---|---|---|---|
| $T_{RLRH}$ | Min | 6 T - x | 3 T - x | 20 | 15 | 25 | ns |
| $T_{WLWH}$ | Min | 6 T - x | 3 T - x | 20 | 15 | 25 | ns |
| $T_{RLDV}$ | Max | 5 T - x | 2.5 T - x | 25 | 23 | 30 | ns |
| $T_{RHDX}$ | Min | x | x | 0 | 0 | 0 | ns |
| $T_{RHDZ}$ | Max | 2 T - x | T - x | 20 | 15 | 25 | ns |
| $T_{LLDV}$ | Max | 8 T - x | 4T -x | 40 | 35 | 45 | ns |
| $T_{AVDV}$ | Max | 9 T - x | 4.5 T - x | 60 | 50 | 65 | ns |
| $T_{LLWL}$ | Min | 3 T - x | 1.5 T - x | 25 | 20 | 30 | ns |
| $T_{LLWL}$ | Max | 3 T + x | 1.5 T + x | 25 | 20 | 30 | ns |
| $T_{AVWL}$ | Min | 4 T - x | 2 T - x | 25 | 20 | 30 | ns |
| $T_{QVWX}$ | Min | T - x | 0.5 T - x | 15 | 10 | 20 | ns |
| $T_{QVWH}$ | Min | 7 T - x | 3.5 T - x | 15 | 10 | 20 | ns |
| $T_{WHQX}$ | Min | T - x | 0.5 T - x | 10 | 8 | 15 | ns |
| $T_{RLAZ}$ | Max | x | x | 0 | 0 | 0 | ns |
| $T_{WHLH}$ | Min | T - x | 0.5 T - x | 15 | 10 | 20 | ns |
| $T_{WHLH}$ | Max | T + x | 0.5 T + x | 15 | 10 | 20 | ns |

### External Data Memory Write Cycle

**Figure 19.** External Data Memory Write Cycle



## EPROM Programming and Verification Characteristics

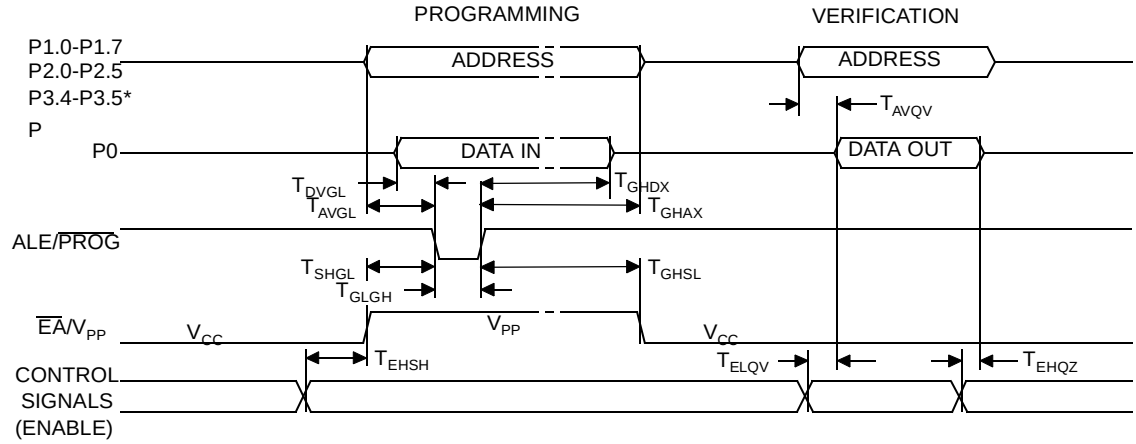
$T_A$ = 21°C to 27°C; $V_{SS}$ = 0V; $V_{CC}$ = 5V ± 10% while programming. $V_{CC}$ = operating range while verifying.

**Table 35.** EPROM Programming Parameters

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $V_{PP}$ | Programming Supply Voltage | 12.5 | 13 | V |
| $I_{PP}$ | Programming Supply Current | | 75 | mA |
| $1/T_{CLCL}$ | Oscillator Frquency | 4 | 6 | MHz |
| $T_{AVGL}$ | Address Setup to $\overline{PROG}$ Low | 48 $T_{CLCL}$ | | |
| $T_{GHAX}$ | Adress Hold after $\overline{PROG}$ | 48 $T_{CLCL}$ | | |
| $T_{DVGL}$ | Data Setup to $\overline{PROG}$ Low | 48 $T_{CLCL}$ | | |
| $T_{GHDX}$ | Data Hold after $\overline{PROG}$ | 48 $T_{CLCL}$ | | |
| $T_{EHSH}$ | (Enable) High to $V_{PP}$ | 48 $T_{CLCL}$ | | |
| $T_{SHGL}$ | $V_{PP}$ Setup to $\overline{PROG}$ Low | 10 | | µs |
| $T_{GHSL}$ | $V_{PP}$ Hold after $\overline{PROG}$ | 10 | | µs |
| $T_{GLGH}$ | $\overline{PROG}$ Width | 90 | 110 | µs |
| $T_{AVQV}$ | Address to Valid Data | | 48 $T_{CLCL}$ | |
| $T_{ELQV}$ | ENABLE Low to Data Valid | | 48 $T_{CLCL}$ | |
| $T_{EHQZ}$ | Data Float after ENABLE | 0 | 48 $T_{CLCL}$ | |

## EPROM Programming and Verification Waveforms

**Figure 22.** EPROM Programming and Verification Waveforms

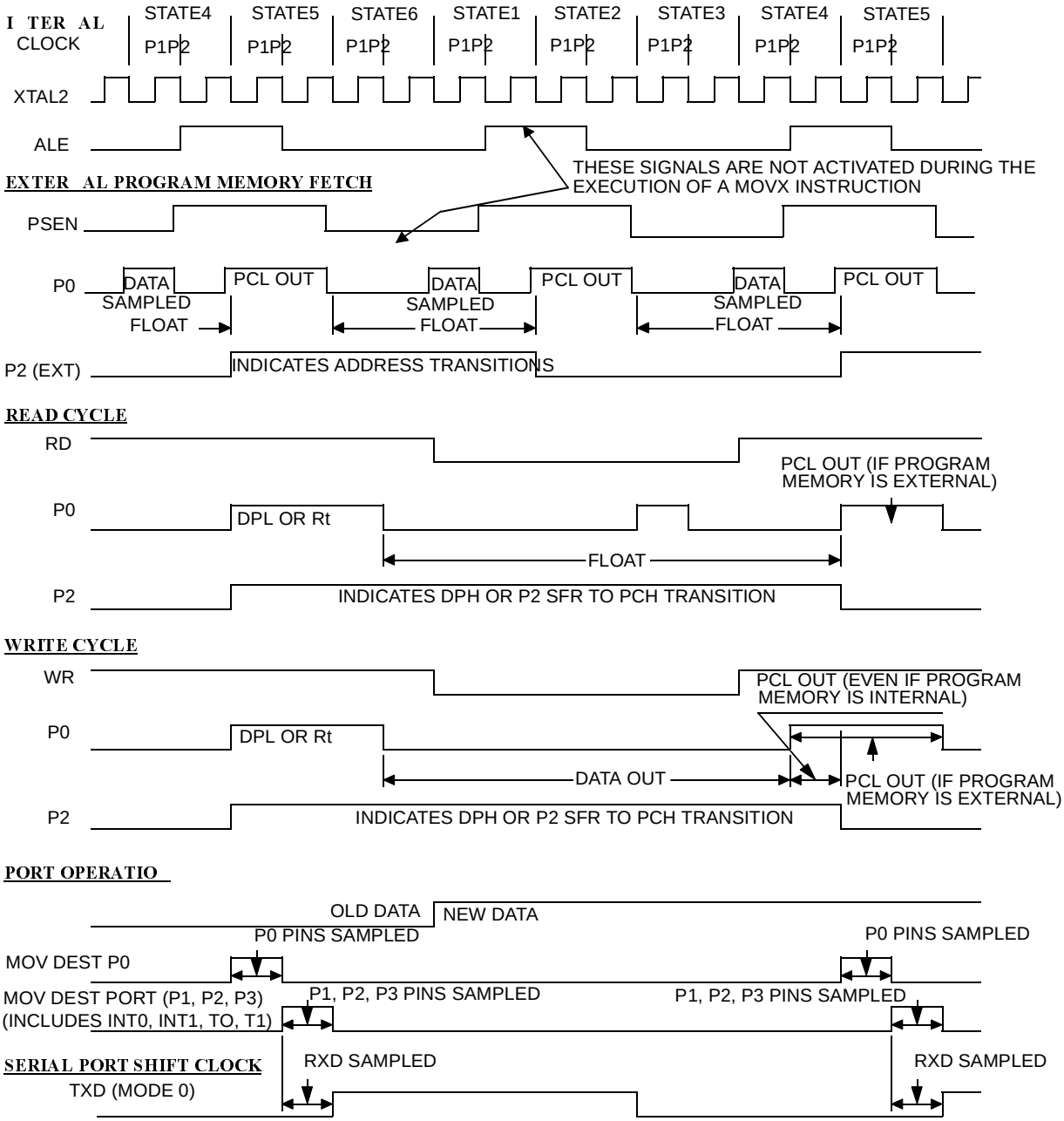



* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

**Clock Waveforms**

Valid in normal clock mode. In X2 mode XTAL2 signal must be changed to XTAL2 divided by two.

**Figure 26.** Clock Waveforms




This diagram indicates when signals are clocked internally. The time it takes the signals to propagate to the pins, however, ranges from 25 to 125 ns. This propagation delay is dependent on variables such as temperature and pin loading. Propagation also varies from output to output and component. Typically though ($T_A$ = 25°C fully loaded) $\overline{RD}$ and $\overline{WR}$ propagation delays are approximately 50ns. The other signals are typically 85 ns. Propagation delays are incorporated in the AC specifications.

## Ordering Information

**Table 37.** Possible Ordering Entries

| Part Number[3] | Memory Size | Supply Voltage | Temperature Range | Max Frequency | Package | Packing |
|---|---|---|---|---|---|---|
| **TS80C32X2**-MCA | ROMLess | 5V ±10% | Commercial | 40 MHz[1] | PDIL40 | Stick |
| **TS80C32X2**-MCB | ROMLess | 5V ±10% | Commercial | 40 MHz[1] | PLCC44 | Stick |
| **TS80C32X2**-MCC | ROMLess | 5V ±10% | Commercial | 40 MHz[1] | PQFP44 | Tray |
| **TS80C32X2**-MCE | ROMLess | 5V ±10% | Commercial | 40 MHz[1] | VQFP44 | Tray |
| **TS80C32X2**-LCA | ROMLess | 2.7 to 5.5V | Commercial | 30 MHz[1] | PDIL40 | Stick |
| **TS80C32X2**-LCB | ROMLess | 2.7 to 5.5V | Commercial | 30 MHz[1] | PLCC44 | Stick |
| **TS80C32X2**-LCC | ROMLess | 2.7 to 5.5V | Commercial | 30 MHz[1] | PQFP44 | Tray |
| **TS80C32X2**-LCE | ROMLess | 2.7 to 5.5V | Commercial | 30 MHz[1] | VQFP44 | Tray |
| **TS80C32X2**-VCA | ROMLess | 5V ±10% | Commercial | 60 MHz[3] | PDIL40 | Stick |
| **TS80C32X2**-VCB | ROMLess | 5V ±10% | Commercial | 60 MHz[3] | PLCC44 | Stick |
| **TS80C32X2**-VCC | ROMLess | 5V ±10% | Commercial | 60 MHz[3] | PQFP44 | Tray |
| **TS80C32X2**-VCE | ROMLess | 5V ±10% | Commercial | 60 MHz[3] | VQFP44 | Tray |
| **TS80C32X2**-MIA | ROMLess | 5V ±10% | Industrial | 40 MHz[1] | PDIL40 | Stick |
| **TS80C32X2**-MIB | ROMLess | 5V ±10% | Industrial | 40 MHz[1] | PLCC44 | Stick |
| **TS80C32X2**-MIC | ROMLess | 5V ±10% | Industrial | 40 MHz[1] | PQFP44 | Tray |
| **TS80C32X2**-MIE | ROMLess | 5V ±10% | Industrial | 40 MHz[1] | VQFP44 | Tray |
| **TS80C32X2**-LIA | ROMLess | 2.7 to 5.5V | Industrial | 30 MHz[1] | PDIL40 | Stick |
| **TS80C32X2**-LIB | ROMLess | 2.7 to 5.5V | Industrial | 30 MHz[1] | PLCC44 | Stick |
| **TS80C32X2**-LIC | ROMLess | 2.7 to 5.5V | Industrial | 30 MHz[1] | PQFP44 | Tray |
| **TS80C32X2**-LIE | ROMLess | 2.7 to 5.5V | Industrial | 30 MHz[1] | VQFP44 | Tray |
| **TS80C32X2**-VIA | ROMLess | 5V ±10% | Industrial | 60 MHz[3] | PDIL40 | Stick |
| **TS80C32X2**-VIB | ROMLess | 5V ±10% | Industrial | 60 MHz[3] | PLCC44 | Stick |
| **TS80C32X2**-VIC | ROMLess | 5V ±10% | Industrial | 60 MHz[3] | PQFP44 | Tray |
| **TS80C32X2**-VIE | ROMLess | 5V ±10% | Industrial | 60 MHz[3] | VQFP44 | Tray |
| | | | | | | |
| **AT80C32X2**-3CSUM | ROMLess | 5V ±10% | Industrial & Green | 40 MHz[1] | PDIL40 | Stick |
| **AT80C32X2**-SLSUM | ROMLess | 5V ±10% | Industrial & Green | 40 MHz[1] | PLCC44 | Stick |
| **AT80C32X2**-RLTUM | ROMLess | 5V ±10% | Industrial & Green | 40 MHz[1] | VQFP44 | Tray |
| **AT80C32X2**-RLTUM | ROMLess | 5V ±10% | Industrial & Green | 40 MHz[1] | VQFP44 | Tape & Reel |
| **AT80C32X2**-3CSUL | ROMLess | 2.7 to 5.5V | Industrial & Green | 30 MHz[1] | PDIL40 | Stick |
| **AT80C32X2**-SLSUL | ROMLess | 2.7 to 5.5V | Industrial & Green | 30 MHz[1] | PLCC44 | Stick |

**Table 37.** Possible Ordering Entries (Continued)

| Part Number[3] | Memory Size | Supply Voltage | Temperature Range | Max Frequency | Package | Packing |
|---|---|---|---|---|---|---|
| **AT80C32X2**-RLTUL | ROMLess | 2.7 to 5.5V | Industrial & Green | 30 MHz[1] | VQFP44 | Tray |
| **AT80C32X2**-3CSUV | ROMLess | 5V ±10% | Industrial & Green | 60 MHz[3] | PDIL40 | Stick |
| **AT80C32X2**-SLSUV | ROMLess | 5V ±10% | Industrial & Green | 60 MHz[3] | PLCC44 | Stick |
| **AT80C32X2**-RLTUV | ROMLess | 5V ±10% | Industrial & Green | 60 MHz[3] | VQFP44 | Tray |
| | | | | | | |
| **TS80C52X2zzz**-MCA | 8K ROM | 2.7 to 5.5V | Commercial | 40 MHz[1] | PDIL40 | Stick |
| **TS80C52X2zzz**-MCB | 8K ROM | 2.7 to 5.5V | Commercial | 40 MHz[1] | PLCC44 | Stick |
| **TS80C52X2zzz**-MCC | 8K ROM | 2.7 to 5.5V | Commercial | 40 MHz[1] | PQFP44 | Tray |
| **TS80C52X2zzz**-MCE | 8K ROM | 2.7 to 5.5V | Commercial | 40 MHz[1] | VQFP44 | Tray |
| **TS80C52X2zzz**-LCA | 8K ROM | 2.7 to 5.5V | Commercial | 30 MHz[1] | PDIL40 | Stick |
| **TS80C52X2zzz**-LCB | 8K ROM | 2.7 to 5.5V | Commercial | 30 MHz[1] | PLCC44 | Stick |
| **TS80C52X2zzz**-LCC | 8K ROM | 2.7 to 5.5V | Commercial | 30 MHz[1] | PQFP44 | Tray |
| **TS80C52X2zzz**-LCE | 8K ROM | 2.7 to 5.5V | Commercial | 30 MHz[1] | VQFP44 | Tray |
| **TS80C52X2zzz**-VCA | 8K ROM | 5V ±10% | Commercial | 60 MHz[3] | PDIL40 | Stick |
| **TS80C52X2zzz**-VCB | 8K ROM | 5V ±10% | Commercial | 60 MHz[3] | PLCC44 | Stick |
| **TS80C52X2zzz**-VCC | 8K ROM | 5V ±10% | Commercial | 60 MHz[3] | PQFP44 | Tray |
| **TS80C52X2zzz**-VCE | 8K ROM | 5V ±10% | Commercial | 60 MHz[3] | VQFP44 | Tray |
| **TS80C52X2zzz**-MIA | 8K ROM | 5V ±10% | Industrial | 40 MHz[1] | PDIL40 | Stick |
| **TS80C52X2zzz**-MIB | 8K ROM | 5V ±10% | Industrial | 40 MHz[1] | PLCC44 | Stick |
| **TS80C52X2zzz**-MIC | 8K ROM | 5V ±10% | Industrial | 40 MHz[1] | PQFP44 | Tray |
| **TS80C52X2zzz**-MIE | 8K ROM | 5V ±10% | Industrial | 40 MHz[1] | VQFP44 | Tray |
| **TS80C52X2zzz**-LIA | 8K ROM | 2.7 to 5.5V | Industrial | 30 MHz[1] | PDIL40 | Stick |
| **TS80C52X2zzz**-LIB | 8K ROM | 2.7 to 5.5V | Industrial | 30 MHz[1] | PLCC44 | Stick |
| **TS80C52X2zzz**-LIC | 8K ROM | 2.7 to 5.5V | Industrial | 30 MHz[1] | PQFP44 | Tray |
| **TS80C52X2zzz**-LIE | 8K ROM | 2.7 to 5.5V | Industrial | 30 MHz[1] | VQFP44 | Tray |
| **TS80C52X2zzz**-VIA | 8K ROM | 5V ±10% | Industrial | 60 MHz[3] | PDIL40 | Stick |
| **TS80C52X2zzz**-VIB | 8K ROM | 5V ±10% | Industrial | 60 MHz[3] | PLCC44 | Stick |
| **TS80C52X2zzz**-VIC | 8K ROM | 5V ±10% | Industrial | 60 MHz[3] | PQFP44 | Tray |
| **TS80C52X2zzz**-VIE | 8K ROM | 5V ±10% | Industrial | 60 MHz[3] | VQFP44 | Tray |
| | | | | | | |
| **AT80C52X2zzz**-3CSUM | 8K ROM | 5V ±10% | Industrial & Green | 40 MHz[1] | PDIL40 | Stick |
| **AT80C52X2zzz**-SLSUM | 8K ROM | 5V ±10% | Industrial & Green | 40 MHz[1] | PLCC44 | Stick |
| **AT80C52X2zzz**-RLTUM | 8K ROM | 5V ±10% | Industrial & Green | 40 MHz[1] | VQFP44 | Tray |

**Table 37.** Possible Ordering Entries (Continued)

| Part Number[3] | Memory Size | Supply Voltage | Temperature Range | Max Frequency | Package | Packing |
|---|---|---|---|---|---|---|
| **AT80C52X2zzz**-3CSUL | 8K ROM | 2.7 to 5.5V | Industrial & Green | 30 MHz[1] | PDIL40 | Stick |
| **AT80C52X2zzz**-SLSUL | 8K ROM | 2.7 to 5.5V | Industrial & Green | 30 MHz[1] | PLCC44 | Stick |
| **AT80C52X2zzz**-RLTUL | 8K ROM | 2.7 to 5.5V | Industrial & Green | 30 MHz[1] | VQFP44 | Tray |
| **AT80C52X2zzz**-3CSUV | 8K ROM | 5V ±10% | Industrial & Green | 60 MHz[3] | PDIL40 | Stick |
| **AT80C52X2zzz**-SLSUV | 8K ROM | 5V ±10% | Industrial & Green | 60 MHz[3] | PLCC44 | Stick |
| **AT80C52X2zzz**-RLTUV | 8K ROM | 5V ±10% | Industrial & Green | 60 MHz[3] | VQFP44 | Tray |
| | | | | | | |
| **TS87C52X2**-MCA | 8K OTP | 5V ±10% | Commercial | 40 MHz[1] | PDIL40 | Stick |
| **TS87C52X2**-MCB | 8K OTP | 5V ±10% | Commercial | 40 MHz[1] | PLCC44 | Stick |
| **TS87C52X2**-MCC | 8K OTP | 5V ±10% | Commercial | 40 MHz[1] | PQFP44 | Tray |
| **TS87C52X2**-MCE | 8K OTP | 5V ±10% | Commercial | 40 MHz[1] | VQFP44 | Tray |
| **TS87C52X2**-LCA | 8K OTP | 2.7 to 5.5V | Commercial | 30 MHz[1] | PDIL40 | Stick |
| **TS87C52X2**-LCB | 8K OTP | 2.7 to 5.5V | Commercial | 30 MHz[1] | PLC44 | Stick |
| **TS87C52X2**-LCC | 8K OTP | 2.7 to 5.5V | Commercial | 30 MHz[1] | PQFP44 | Tray |
| **TS87C52X2**-LCE | 8K OTP | 2.7 to 5.5V | Commercial | 30 MHz[1] | VQFP44 | Tray |
| **TS87C52X2**-VCA | 8K OTP | 5V ±10% | Commercial | 60 MHz[3] | PDIL40 | Stick |
| **TS87C52X2**-VCB | 8K OTP | 5V ±10% | Commercial | 60 MHz[3] | PLCC44 | Stick |
| **TS87C52X2**-VCC | 8K OTP | 5V ±10% | Commercial | 60 MHz[3] | PQFP44 | Tray |
| **TS87C52X2**-VCE | 8K OTP | 5V ±10% | Commercial | 60 MHz[3] | VQFP44 | Tray |
| **TS87C52X2**-MIA | 8K OTP | 5V ±10% | Industrial | 40 MHz[1] | PDIL40 | Stick |
| **TS87C52X2**-MIB | 8K OTP | 5V ±10% | Industrial | 40 MHz[1] | PLCC44 | Stick |
| **TS87C52X2**-MIC | 8K OTP | 5V ±10% | Industrial | 40 MHz[1] | PQFP44 | Tray |
| **TS87C52X2**-MIE | 8K OTP | 5V ±10% | Industrial | 40 MHz[1] | VQFP44 | Tray |
| **TS87C52X2**-LIA | 8K OTP | 2.7 to 5.5V | Industrial | 30 MHz[1] | PDIL40 | Stick |
| **TS87C52X2**-LIB | 8K OTP | 2.7 to 5.5V | Industrial | 30 MHz[1] | PLCC44 | Stick |
| **TS87C52X2**-LIC | 8K OTP | 2.7 to 5.5V | Industrial | 30 MHz[1] | PQFP44 | Tray |
| **TS87C52X2**-LIE | 8K OTP | 2.7 to 5.5V | Industrial | 30 MHz[1] | VQFP44 | Tray |
| **TS87C52X2**-VIA | 8K OTP | 5V ±10% | Industrial | 60 MHz[3] | PDIL40 | Stick |
| **TS87C52X2**-VIB | 8K OTP | 5V ±10% | Industrial | 60 MHz[3] | PLCC44 | Stick |
| **TS87C52X2**-VIC | 8K OTP | 5V ±10% | Industrial | 60 MHz[3] | PQFP44 | Tray |
| **TS87C52X2**-VIE | 8K OTP | 5V ±10% | Industrial | 60 MHz[3] | VQFP44 | Tray |
| | | | | | | |
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