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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	40/20MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-PQFP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/ts87c52x2-mic">https://www.e-xfl.com/product-detail/microchip-technology/ts87c52x2-mic</a>

**Table 2.** All SFRs with their address and their reset value

	Bit Addressable	Non Bit Addressable							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h									FFh
F0h	B 0000 0000								F7h
E8h									EFh
E0h	ACC 0000 0000								E7h
D8 h									DFh
D0 h	PSW 0000 0000								D7h
C8 h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0 h									C7h
B8h	IP XX00 0000	SADEN 0000 0000							BFh
B0h	P3 1111 1111							IPH XX00 0000	B7h
A8h	IE 0X00 0000	SADDR 0000 0000							AFh
A0h	P2 1111 1111		AUXR1 XXXX XXX0						A7h
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXXXXXX0	CKCON XXXX XXX0	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Reserved 

## TS80C52X2 Enhanced Features

In comparison to the original 80C52, the TS80C52X2 implements some new features, which are:

- The X2 option
- The Dual Data Pointer
- The 4 level interrupt priority system
- The power-off flag
- The ONCE mode
- The ALE disabling
- Some enhanced features are also located in the UART and the Timer 2

### X2 Feature

The TS80C52X2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

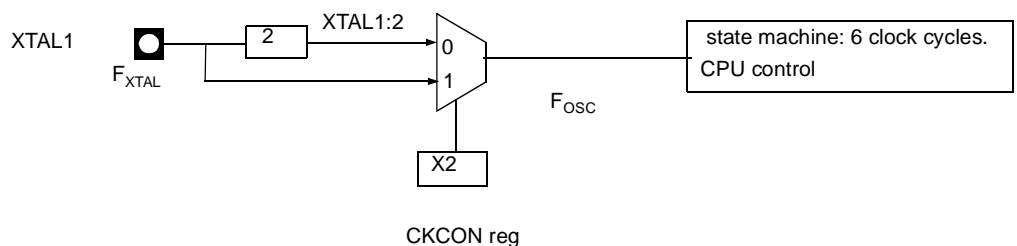
- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power
- Save power consumption while keeping same CPU power (oscillator power saving)
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes
- Increase CPU power by 2 while keeping same crystal frequency

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

### Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 1. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 2 shows the mode switching waveforms.

**Figure 1.** Clock Generation Diagram



## Application

Software can take advantage of the additional data pointers to both increase speed and reduce code size, for example, block operations (copy, compare, search ...) are well served by using one data pointer as a 'source' pointer and the other one as a "destination" pointer.

### ASSEMBLY LANGUAGE

```

; Block move using dual data pointers
; Destroys DPTR0, DPTR1, A and PSW
; note: DPS exits opposite of entry state
; unless an extra INC AUXR1 is added
;
00A2  AUXR1 EQU 0A2H
;
0000 909000 MOV DPTR,#SOURCE ; address of SOURCE
0003 05A2 INC AUXR1 ; switch data pointers
0005 90A000 MOV DPTR,#DEST ; address of DEST
0008  LOOP:
0008 05A2 INC AUXR1 ; switch data pointers
000A E0 MOVX A,atDPTR ; get a byte from SOURCE
000B A3 INC DPTR ; increment SOURCE address
000C 05A2 INC AUXR1 ; switch data pointers
000E F0 MOVX atDPTR,A ; write the byte to DEST
000F A3 INC DPTR ; increment DEST address
0010 70F6JNZ LOOP ; check for 0 terminator
0012 05A2 INC AUXR1 ; (optional) restore DPS

```

INC is a short (2 bytes) and fast (12 clocks) way to manipulate the DPS bit in the AUXR1 SFR. However, note that the INC instruction does not directly force the DPS bit to a particular state, but simply toggles it. In simple routines, such as the block move example, only the fact that DPS is toggled in the proper sequence matters, not its actual value. In other words, the block move routine works the same whether DPS is '0' or '1' on entry. Observe that without the last instruction (INC AUXR1), the routine will exit with DPS in the opposite state.

## Timer 2

The timer 2 in the TS80C52X2 is compatible with the timer 2 in the 80C52.

It is a 16-bit timer/counter: the count is maintained by two eight-bit timer registers, TH2 and TL2, connected in cascade. It is controlled by T2CON register (See Table 5) and T2MOD register (See Table 6). Timer 2 operation is similar to Timer 0 and Timer 1. C/T2 selects  $F_{OSC}/12$  (timer operation) or external pin T2 (counter operation) as the timer clock input. Setting TR2 allows TL2 to be incremented by the selected input.

Timer 2 has 3 operating modes: capture, autoreload and Baud Rate Generator. These modes are selected by the combination of RCLK, TCLK and CP/RL2 (T2CON), as described in the Atmel 8-bit Microcontroller Hardware description.

Refer to the Atmel 8-bit Microcontroller Hardware description for the description of Capture and Baud Rate Generator Modes.

In TS80C52X2 Timer 2 includes the following enhancements:

- Auto-reload mode with up or down counter
- Programmable clock-output

### Auto-reload Mode

The Auto-reload mode configures timer 2 as a 16-bit timer or event counter with automatic reload. If DCEN bit in T2MOD is cleared, timer 2 behaves as in 80C52 (refer to the Atmel 8-bit Microcontroller Hardware description). If DCEN bit is set, timer 2 acts as an Up/down timer/counter as shown in Figure 4. In this mode the T2EX pin controls the direction of count.

When T2EX is high, timer 2 counts up. Timer overflow occurs at FFFFh which sets the TF2 flag and generates an interrupt request. The overflow also causes the 16-bit value in RCAP2H and RCAP2L registers to be loaded into the timer registers TH2 and TL2.

When T2EX is low, timer 2 counts down. Timer underflow occurs when the count in the timer registers TH2 and TL2 equals the value stored in RCAP2H and RCAP2L registers. The underflow sets TF2 flag and reloads FFFFh into the timer registers.

The EXF2 bit toggles when timer 2 overflows or underflows according to the the direction of the count. EXF2 does not generate any interrupt. This bit can be used to provide 17-bit resolution.

**Table 5. T2CON Register**  
T2CON - Timer 2 Control Register (C8h)

7	6	5	4	3	2	1	0
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#
Bit Number	Bit Mnemonic	Description					
7	TF2	<b>Timer 2 overflow Flag</b> Must be cleared by software. Set by hardware on timer 2 overflow, if RCLK = 0 and TCLK = 0.					
6	EXF2	<b>Timer 2 External Flag</b> Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. When set, causes the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled. Must be cleared by software. EXF2 doesn't cause an interrupt in Up/down counter mode (DCEN = 1)					
5	RCLK	<b>Receive Clock bit</b> Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3. Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3.					
4	TCLK	<b>Transmit Clock bit</b> Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3. Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3.					
3	EXEN2	<b>Timer 2 External Enable bit</b> Clear to ignore events on T2EX pin for timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port.					
2	TR2	<b>Timer 2 Run control bit</b> Clear to turn off timer 2. Set to turn on timer 2.					
1	C/T2#	<b>Timer/Counter 2 select bit</b> Clear for timer operation (input from internal clock system: $F_{OSC}$ ). Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode.					
0	CP/RL2#	<b>Timer 2 Capture/Reload bit</b> If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to Auto-reload on timer 2 overflow. Clear to Auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1. Set to capture on negative transitions on T2EX pin if EXEN2=1.					

Reset Value = 0000 0000b

Bit addressable

## TS80C52X2 Serial I/O Port

The serial I/O port in the TS80C52X2 is compatible with the serial I/O port in the 80C52. It provides both synchronous and asynchronous communication modes. It operates as an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simultaneously and at different baud rates

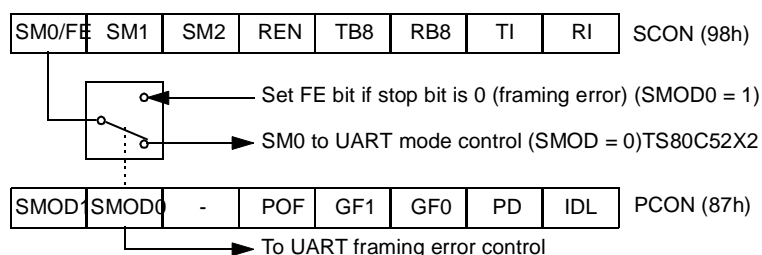
Serial I/O port includes the following enhancements:

- Framing error detection
- Automatic address recognition

### Framing Error Detection

Framing bit error detection is provided for the three asynchronous modes (modes 1, 2 and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON register (See Figure 6).

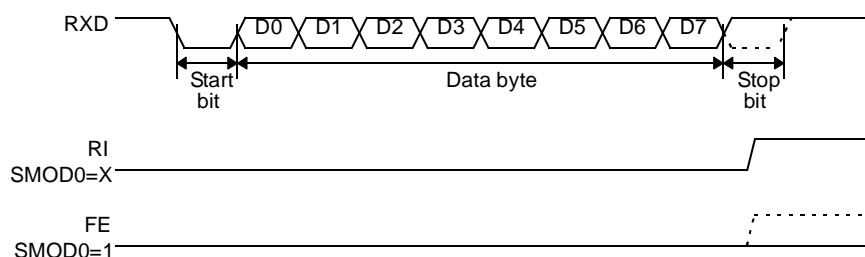
**Figure 6.** Framing Error Block Diagram



When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 9.) bit is set.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 7. and Figure 8.).

**Figure 7.** UART Timings in Mode 1



1111 0000b).

For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).

To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

## Broadcast Address

A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

```
SADDR 0101 0110b
SADEN 1111 1100b
Broadcast =SADDR OR SADEN1111 111Xb
```

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

```
Slave A:SADDR1111 0001b
      SADEN1111 1010b
Broadcast1111 1X11b,
```

```
Slave B:SADDR1111 0011b
      SADEN1111 1001b
Broadcast1111 1X11b,
```

```
Slave C:SADDR=1111 0010b
      SADEN1111 1101b
Broadcast1111 1111b
```

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send an address FBh.

## Reset Addresses

On reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and broadcast addresses are XXXX XXXXb (all don't-care bits). This ensures that the serial port will reply to any address, and so, that it is backwards compatible with the 80C51 microcontrollers that do not support automatic address recognition.

**Table 7. SADEN Register**  
SADEN - Slave Address Mask Register (B9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Not bit addressable

**Table 8. SADDR Register**  
SADDR - Slave Address Register (A9h)

7	6	5	4	3	2	1	0

Reset Value = 0000 0000b

Not bit addressable





**Table 10.** PCON Register  
PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	SMOD0	-	POF	GF1	GF0	PD	IDL

Bit Number	Bit Mnemonic	Description
7	SMOD1	<b>Serial port Mode bit 1</b> Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	<b>Serial port Mode bit 0</b> Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
4	POF	<b>Power-off Flag</b> Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	<b>General purpose Flag</b> Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	<b>Power-down mode bit</b> Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	<b>Idle mode bit</b> Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b

Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

**Table 13.** IP Register  
IP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	-	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.
5	PT2	<b>Timer 2 overflow interrupt Priority bit</b> Refer to PT2H for priority level.
4	PS	<b>Serial port Priority bit</b> Refer to PSH for priority level.
3	PT1	<b>Timer 1 overflow interrupt Priority bit</b> Refer to PT1H for priority level.
2	PX1	<b>External interrupt 1 Priority bit</b> Refer to PX1H for priority level.
1	PT0	<b>Timer 0 overflow interrupt Priority bit</b> Refer to PT0H for priority level.
0	PX0	<b>External interrupt 0 Priority bit</b> Refer to PX0H for priority level.

Reset Value = XX00 0000b  
Bit addressable

**Table 14.** IPH Register  
IPH - Interrupt Priority High Register (B7h)

7	6	5	4	3	2	1	0
-	-	PT2H	PSH	PT1H	PX1H	PT0H	PX0H

Bit Number	Bit Mnemonic	Description															
7	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.															
6	-	<b>Reserved</b> The value read from this bit is indeterminate. Do not set this bit.															
5	PT2H	<b>Timer 2 overflow interrupt Priority High bit</b> <table> <tr> <th>PT2H</th><th>PT2</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PT2H	PT2	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT2H	PT2	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
4	PSH	<b>Serial port Priority High bit</b> <table> <tr> <th>PSH</th><th>PS</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PSH	PS	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PSH	PS	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
3	PT1H	<b>Timer 1 overflow interrupt Priority High bit</b> <table> <tr> <th>PT1H</th><th>PT1</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PT1H	PT1	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT1H	PT1	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
2	PX1H	<b>External interrupt 1 Priority High bit</b> <table> <tr> <th>PX1H</th><th>PX1</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PX1H	PX1	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PX1H	PX1	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
1	PT0H	<b>Timer 0 overflow interrupt Priority High bit</b> <table> <tr> <th>PT0H</th><th>PT0</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PT0H	PT0	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PT0H	PT0	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															
0	PX0H	<b>External interrupt 0 Priority High bit</b> <table> <tr> <th>PX0H</th><th>PX0</th><th>Priority Level</th></tr> <tr> <td>0</td><td>0</td><td>Lowest</td></tr> <tr> <td>0</td><td>1</td><td></td></tr> <tr> <td>1</td><td>0</td><td></td></tr> <tr> <td>1</td><td>1</td><td>Highest</td></tr> </table>	PX0H	PX0	Priority Level	0	0	Lowest	0	1		1	0		1	1	Highest
PX0H	PX0	Priority Level															
0	0	Lowest															
0	1																
1	0																
1	1	Highest															

Reset Value = XX00 0000b  
Not bit addressable

Exit from power-down by reset redefines all the SFRs, exit from power-down by external interrupt does not affect the SFRs.

Exit from power-down by either reset or external interrupt does not affect the internal RAM content.

Note: If idle mode is activated with power-down mode (IDL and PD bits set), the exit sequence is unchanged, when execution is vectored to interrupt, PD and IDL bits are cleared and idle mode is not entered.

**Table 15.** The State of Ports During Idle and Power-down Modes

Mode	Program Memory	ALE	PSEN	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Port Data <sup>(1)</sup>	Port Data	Port Data	Port Data
Idle	External	1	1	Floating	Port Data	Address	Port Data
Power Down	Internal	0	0	Port Data <sup>(1)</sup>	Port Data	Port Data	Port Data
Power Down	External	0	0	Floating	Port Data	Port Data	Port Data

Note: 1. Port 0 can force a "zero" level. A "one" will leave port floating.

## ONCE™ Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS80C52X2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C52X2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and  $\overline{\text{PSEN}}$  is high.
- Hold ALE low as RST is deactivated.

While the TS80C52X2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 26. shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

**Table 16.** External Pin Status during ONCE Mode

ALE	PSEN	Port 0	Port 1	Port 2	Port 3	XTAL1/2
Weak pull-up	Weak pull-up	Float	Weak pull-up	Weak pull-up	Weak pull-up	Active

## EPROM Structure

The TS87C52X2 is divided in two different arrays:

- the code array: 8 Kbytes
- the encryption array: 64 bytes

In addition a third non programmable array is implemented:

- the signature array: 4 bytes

## EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

### Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

### Program Lock Bits

The three lock bits, when programmed according to Table 1., will provide different level of protection for the on-chip code and data.

Program Lock Bits				Protection Description
Security level	LB1	LB2	LB3	
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	P	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset, and further programming of the EPROM is disabled.
3	U	P	U	Same as 2, also verify is disabled.
4	U	U	P	Same as 3, also external execution is disabled.

U: unprogrammed

P: programmed

**WARNING:** Security level 2 and 3 should only be programmed after EPROM and Core verification.

### Signature Bytes

The TS80/87C52X2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 9.

## EPROM Programming

### Set-up modes

In order to program and verify the EPROM or to read the signature bytes, the TS87C52X2 is placed in specific set-up modes (See Figure 11.).

## Electrical Characteristics

### Absolute Maximum Ratings<sup>(1)</sup>

Ambient Temperature Under Bias:

C = commercial.....0°C to 70°C  
 I = industrial .....-40°C to 85°C  
 Storage Temperature ..... -65°C to + 150°C  
 Voltage on V<sub>CC</sub> to V<sub>SS</sub>.....-0.5V to + 7 V  
 Voltage on V<sub>PP</sub> to V<sub>SS</sub>.....-0.5V to + 13 V  
 Voltage on Any Pin to V<sub>SS</sub>.....-0.5V to V<sub>CC</sub> + 0.5V  
 Power Dissipation ..... 1 W<sup>(2)</sup>

- Notes: 1. Stresses at or above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

### Power Consumption Measurement

Since the introduction of the first C51 devices, every manufacturer made operating I<sub>cc</sub> measurements under reset, which made sense for the designs where the CPU was running under reset. In Atmel new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That's why, while keeping measurements under Reset, Atmel presents a new way to measure the operating I<sub>cc</sub>:

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = V<sub>CC</sub>, RST = V<sub>SS</sub>, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating I<sub>cc</sub>.

### DC Parameters for Standard Voltage

T<sub>A</sub> = 0°C to +70°C; V<sub>SS</sub> = 0 V; V<sub>CC</sub> = 5V ± 10%; F = 0 to 40 MHz.  
 T<sub>A</sub> = -40°C to +85°C; V<sub>SS</sub> = 0 V; V<sub>CC</sub> = 5V ± 10%; F = 0 to 40 MHz.

**Table 22.** DC Parameters in Standard Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V <sub>IL</sub>	Input Low Voltage	-0.5		0.2 V <sub>CC</sub> - 0.1	V	
V <sub>IH</sub>	Input High Voltage except XTAL1, RST	0.2 V <sub>CC</sub> + 0.9		V <sub>CC</sub> + 0.5	V	
V <sub>IH1</sub>	Input High Voltage, XTAL1, RST	0.7 V <sub>CC</sub>		V <sub>CC</sub> + 0.5	V	
V <sub>OL</sub>	Output Low Voltage, ports 1, 2, 3 <sup>(6)</sup>			0.3	V	I <sub>OL</sub> = 100 μA <sup>(4)</sup>
				0.45	V	I <sub>OL</sub> = 1.6 mA <sup>(4)</sup>
				1.0	V	I <sub>OL</sub> = 3.5 mA <sup>(4)</sup>
V <sub>OL1</sub>	Output Low Voltage, port 0 <sup>(6)</sup>			0.3	V	I <sub>OL</sub> = 200 μA <sup>(4)</sup>
				0.45	V	I <sub>OL</sub> = 3.2 mA <sup>(4)</sup>
				1.0	V	I <sub>OL</sub> = 7.0 mA <sup>(4)</sup>
V <sub>OL2</sub>	Output Low Voltage, ALE, $\overline{\text{PSEN}}$			0.3	V	I <sub>OL</sub> = 100 μA <sup>(4)</sup>
				0.45	V	I <sub>OL</sub> = 1.6 mA <sup>(4)</sup>
				1.0	V	I <sub>OL</sub> = 3.5 mA <sup>(4)</sup>

Table 28., Table 31. and Table 34. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

**Table 25.** Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
<b>Freq (MHz)</b>	40	20	40	30	30	20
<b>T (ns)</b>	25	50	25	33.3	33.3	50

Example:

$T_{LLIV}$  in X2 mode for a -V part at 20 MHz ( $T = 1/20^{E6} = 50$  ns):

x= 22 (Table 28.)

T= 50ns

$T_{LLIV} = 2T - x = 2 \times 50 - 22 = 78$ ns

## External Program Memory Characteristics

**Table 26.** Symbol Description

Symbol	Parameter
T	Oscillator clock period
$T_{LHLL}$	ALE pulse width
$T_{AVLL}$	Address Valid to ALE
$T_{LLAX}$	Address Hold After ALE
$T_{LLIV}$	ALE to Valid Instruction In
$T_{LLPL}$	ALE to $\overline{PSEN}$
$T_{PLPH}$	$\overline{PSEN}$ Pulse Width
$T_{PLIV}$	$\overline{PSEN}$ to Valid Instruction In
$T_{PXIX}$	Input Instruction Hold After $\overline{PSEN}$
$T_{PXIZ}$	Input Instruction FloatAfter $\overline{PSEN}$
$T_{PXAV}$	$\overline{PSEN}$ to Address Valid
$T_{AVIV}$	Address to Valid Instruction In
$T_{PLAZ}$	$\overline{PSEN}$ Low to Address Float



**Table 27. AC Parameters for Fix Clock**

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
T	25		33		25		50		33		ns
T <sub>LHLL</sub>	40		25		42		35		52		ns
T <sub>AVLL</sub>	10		4		12		5		13		ns
T <sub>LLAX</sub>	10		4		12		5		13		ns
T <sub>LLIV</sub>		70		45		78		65		98	ns
T <sub>LLPL</sub>	15		9		17		10		18		ns
T <sub>PLPH</sub>	55		35		60		50		75		ns
T <sub>PLIV</sub>		35		25		50		30		55	ns
T <sub>PXIX</sub>	0		0		0		0		0		ns
T <sub>PXIZ</sub>		18		12		20		10		18	ns
T <sub>AVIV</sub>		85		53		95		80		122	ns
T <sub>PLAZ</sub>		10		10		10		10		10	ns

**Table 28. AC Parameters for a Variable Clock: derating formula**

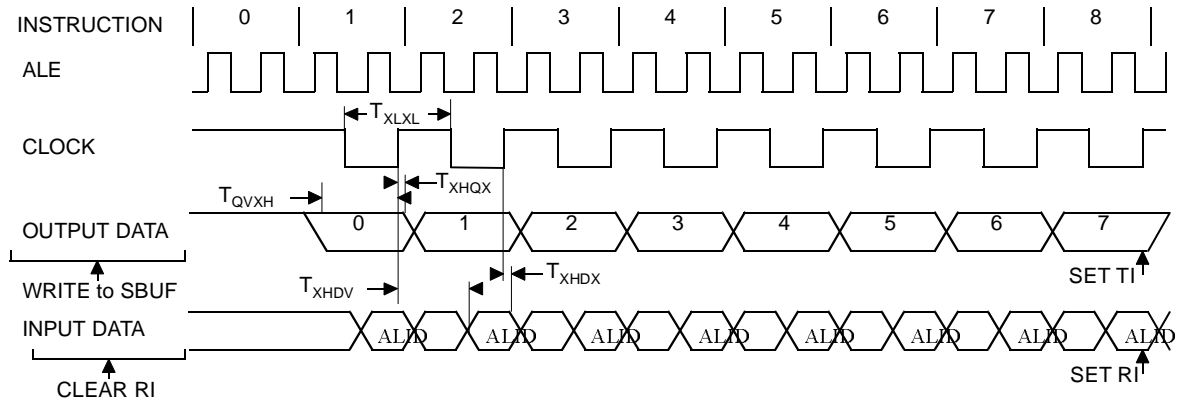
Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T <sub>LHLL</sub>	Min	2 T - x	T - x	10	8	15	ns
T <sub>AVLL</sub>	Min	T - x	0.5 T - x	15	13	20	ns
T <sub>LLAX</sub>	Min	T - x	0.5 T - x	15	13	20	ns
T <sub>LLIV</sub>	Max	4 T - x	2 T - x	30	22	35	ns
T <sub>LLPL</sub>	Min	T - x	0.5 T - x	10	8	15	ns
T <sub>PLPH</sub>	Min	3 T - x	1.5 T - x	20	15	25	ns
T <sub>PLIV</sub>	Max	3 T - x	1.5 T - x	40	25	45	ns
T <sub>PXIX</sub>	Min	x	x	0	0	0	ns
T <sub>PXIZ</sub>	Max	T - x	0.5 T - x	7	5	15	ns
T <sub>AVIV</sub>	Max	5 T - x	2.5 T - x	40	30	45	ns
T <sub>PLAZ</sub>	Max	x	x	10	10	10	ns

**Table 34.** AC Parameters for a Variable Clock: Derating Formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
$T_{XLXL}$	Min	12 T	6 T				ns
$T_{QVHX}$	Min	10 T - x	5 T - x	50	50	50	ns
$T_{XHGX}$	Min	2 T - x	T - x	20	20	20	ns
$T_{XHDX}$	Min	x	x	0	0	0	ns
$T_{XHDV}$	Max	10 T - x	5 T - x	133	133	133	ns

## Shift Register Timing Waveforms

**Figure 21.** Shift Register Timing Waveforms



## EPROM Programming and Verification Characteristics

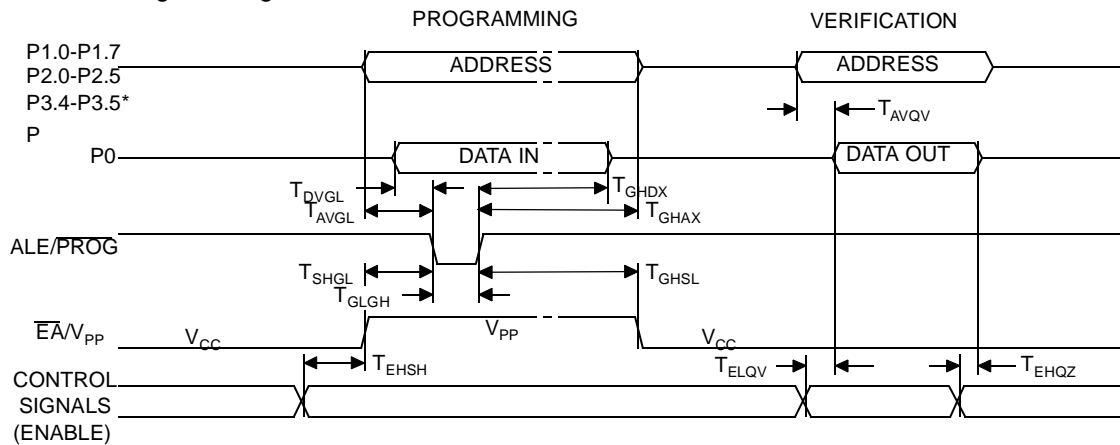
$T_A = 21^{\circ}\text{C}$  to  $27^{\circ}\text{C}$ ;  $V_{SS} = 0\text{V}$ ;  $V_{CC} = 5\text{V} \pm 10\%$  while programming.  $V_{CC}$  = operating range while verifying.

**Table 35.** EPROM Programming Parameters

Symbol	Parameter	Min	Max	Units
$V_{PP}$	Programming Supply Voltage	12.5	13	V
$I_{PP}$	Programming Supply Current		75	mA
$1/T_{CLCL}$	Oscillator Frequency	4	6	MHz
$T_{AVGL}$	Address Setup to $\overline{\text{PROG}}$ Low	$48 T_{CLCL}$		
$T_{GHAX}$	Address Hold after $\overline{\text{PROG}}$	$48 T_{CLCL}$		
$T_{DVGL}$	Data Setup to $\overline{\text{PROG}}$ Low	$48 T_{CLCL}$		
$T_{GHDX}$	Data Hold after $\overline{\text{PROG}}$	$48 T_{CLCL}$		
$T_{EHS}$	(Enable) High to $V_{PP}$	$48 T_{CLCL}$		
$T_{SHGL}$	$V_{PP}$ Setup to $\overline{\text{PROG}}$ Low	10		$\mu\text{s}$
$T_{GHSL}$	$V_{PP}$ Hold after $\overline{\text{PROG}}$	10		$\mu\text{s}$
$T_{GLGH}$	$\overline{\text{PROG}}$ Width	90	110	$\mu\text{s}$
$T_{AVQV}$	Address to Valid Data		$48 T_{CLCL}$	
$T_{ELQV}$	ENABLE Low to Data Valid		$48 T_{CLCL}$	
$T_{EHQZ}$	Data Float after ENABLE	0	$48 T_{CLCL}$	

## EPROM Programming and Verification Waveforms

**Figure 22.** EPROM Programming and Verification Waveforms



\* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

## Ordering Information

**Table 37. Possible Ordering Entries**

Part Number <sup>(3)</sup>	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
<b>TS80C32X2-MCA</b>	ROMLess	5V $\pm$ 10%	Commercial	40 MHz <sup>(1)</sup>	PDIL40	Stick
<b>TS80C32X2-MCB</b>	ROMLess	5V $\pm$ 10%	Commercial	40 MHz <sup>(1)</sup>	PLCC44	Stick
<b>TS80C32X2-MCC</b>	ROMLess	5V $\pm$ 10%	Commercial	40 MHz <sup>(1)</sup>	PQFP44	Tray
<b>TS80C32X2-MCE</b>	ROMLess	5V $\pm$ 10%	Commercial	40 MHz <sup>(1)</sup>	VQFP44	Tray
<b>TS80C32X2-LCA</b>	ROMLess	2.7 to 5.5V	Commercial	30 MHz <sup>(1)</sup>	PDIL40	Stick
<b>TS80C32X2-LCB</b>	ROMLess	2.7 to 5.5V	Commercial	30 MHz <sup>(1)</sup>	PLCC44	Stick
<b>TS80C32X2-LCC</b>	ROMLess	2.7 to 5.5V	Commercial	30 MHz <sup>(1)</sup>	PQFP44	Tray
<b>TS80C32X2-LCE</b>	ROMLess	2.7 to 5.5V	Commercial	30 MHz <sup>(1)</sup>	VQFP44	Tray
<b>TS80C32X2-VCA</b>	ROMLess	5V $\pm$ 10%	Commercial	60 MHz <sup>(3)</sup>	PDIL40	Stick
<b>TS80C32X2-VCB</b>	ROMLess	5V $\pm$ 10%	Commercial	60 MHz <sup>(3)</sup>	PLCC44	Stick
<b>TS80C32X2-VCC</b>	ROMLess	5V $\pm$ 10%	Commercial	60 MHz <sup>(3)</sup>	PQFP44	Tray
<b>TS80C32X2-VCE</b>	ROMLess	5V $\pm$ 10%	Commercial	60 MHz <sup>(3)</sup>	VQFP44	Tray
<b>TS80C32X2-MIA</b>	ROMLess	5V $\pm$ 10%	Industrial	40 MHz <sup>(1)</sup>	PDIL40	Stick
<b>TS80C32X2-MIB</b>	ROMLess	5V $\pm$ 10%	Industrial	40 MHz <sup>(1)</sup>	PLCC44	Stick
<b>TS80C32X2-MIC</b>	ROMLess	5V $\pm$ 10%	Industrial	40 MHz <sup>(1)</sup>	PQFP44	Tray
<b>TS80C32X2-MIE</b>	ROMLess	5V $\pm$ 10%	Industrial	40 MHz <sup>(1)</sup>	VQFP44	Tray
<b>TS80C32X2-LIA</b>	ROMLess	2.7 to 5.5V	Industrial	30 MHz <sup>(1)</sup>	PDIL40	Stick
<b>TS80C32X2-LIB</b>	ROMLess	2.7 to 5.5V	Industrial	30 MHz <sup>(1)</sup>	PLCC44	Stick
<b>TS80C32X2-LIC</b>	ROMLess	2.7 to 5.5V	Industrial	30 MHz <sup>(1)</sup>	PQFP44	Tray
<b>TS80C32X2-LIE</b>	ROMLess	2.7 to 5.5V	Industrial	30 MHz <sup>(1)</sup>	VQFP44	Tray
<b>TS80C32X2-VIA</b>	ROMLess	5V $\pm$ 10%	Industrial	60 MHz <sup>(3)</sup>	PDIL40	Stick
<b>TS80C32X2-VIB</b>	ROMLess	5V $\pm$ 10%	Industrial	60 MHz <sup>(3)</sup>	PLCC44	Stick
<b>TS80C32X2-VIC</b>	ROMLess	5V $\pm$ 10%	Industrial	60 MHz <sup>(3)</sup>	PQFP44	Tray
<b>TS80C32X2-VIE</b>	ROMLess	5V $\pm$ 10%	Industrial	60 MHz <sup>(3)</sup>	VQFP44	Tray
<b>AT80C32X2-3CSUM</b>	ROMLess	5V $\pm$ 10%	Industrial & Green	40 MHz <sup>(1)</sup>	PDIL40	Stick
<b>AT80C32X2-SLSUM</b>	ROMLess	5V $\pm$ 10%	Industrial & Green	40 MHz <sup>(1)</sup>	PLCC44	Stick
<b>AT80C32X2-RLTUM</b>	ROMLess	5V $\pm$ 10%	Industrial & Green	40 MHz <sup>(1)</sup>	VQFP44	Tray
<b>AT80C32X2-RLTUM</b>	ROMLess	5V $\pm$ 10%	Industrial & Green	40 MHz <sup>(1)</sup>	VQFP44	Tape & Reel
<b>AT80C32X2-3CSUL</b>	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz <sup>(1)</sup>	PDIL40	Stick
<b>AT80C32X2-SLSUL</b>	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz <sup>(1)</sup>	PLCC44	Stick



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