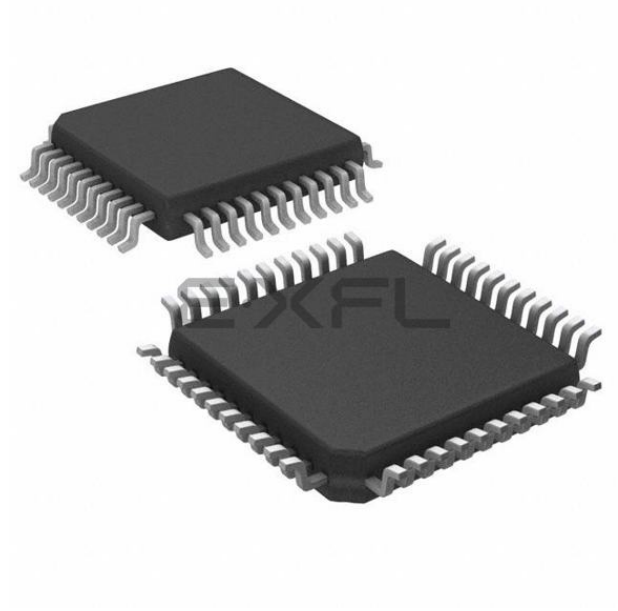


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	60/30MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	OTP
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-QFP
Supplier Device Package	44-PQFP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c52x2-vcc

TS80C52X2 Enhanced Features

In comparison to the original 80C52, the TS80C52X2 implements some new features, which are:

- The X2 option
- The Dual Data Pointer
- The 4 level interrupt priority system
- The power-off flag
- The ONCE mode
- The ALE disabling
- Some enhanced features are also located in the UART and the Timer 2

X2 Feature

The TS80C52X2 core needs only 6 clock periods per machine cycle. This feature called "X2" provides the following advantages:

- Divide frequency crystals by 2 (cheaper crystals) while keeping same CPU power
- Save power consumption while keeping same CPU power (oscillator power saving)
- Save power consumption by dividing dynamically operating frequency by 2 in operating and idle modes
- Increase CPU power by 2 while keeping same crystal frequency

In order to keep the original C51 compatibility, a divider by 2 is inserted between the XTAL1 signal and the main clock input of the core (phase generator). This divider may be disabled by software.

Description

The clock for the whole circuit and peripheral is first divided by two before being used by the CPU core and peripherals. This allows any cyclic ratio to be accepted on XTAL1 input. In X2 mode, as this divider is bypassed, the signals on XTAL1 must have a cyclic ratio between 40 to 60%. Figure 1. shows the clock generation block diagram. X2 bit is validated on XTAL1÷2 rising edge to avoid glitches when switching from X2 to STD mode. Figure 2 shows the mode switching waveforms.

Figure 1. Clock Generation Diagram

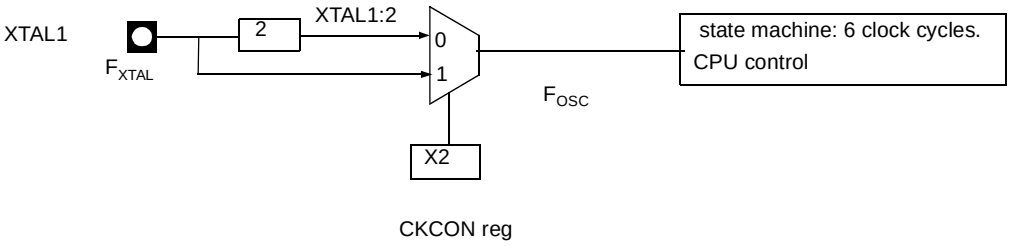


Table 6. T2MOD Register

T2MOD - Timer 2 Mode Control Register (C9h)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	T2OE	DCEN

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	T2OE	**Timer 2 Output Enable bit** Clear to program P1.0/T2 as clock input or I/O port. Set to program P1.0/T2 as clock output.
0	DCEN	**Down Counter Enable bit** Clear to disable timer 2 as up/down counter. Set to enable timer 2 as up/down counter.

Reset Value = XXXX XX00b

Not bit addressable

Table 10. PCON Register

PCON - Power Control Register (87h)

7	6	5	4	3	2	1	0
SMOD1	**SMOD0**	**-**	**POF**	**GF1**	**GF0**	**PD**	**IDL**

Bit Number	Bit Mnemonic	Description
7	SMOD1	**Serial port Mode bit 1** Set to select double baud rate in mode 1, 2 or 3.
6	SMOD0	**Serial port Mode bit 0** Clear to select SM0 bit in SCON register. Set to to select FE bit in SCON register.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	POF	**Power-off Flag** Clear to recognize next reset type. Set by hardware when VCC rises from 0 to its nominal voltage. Can also be set by software.
3	GF1	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
2	GF0	**General purpose Flag** Cleared by user for general purpose usage. Set by user for general purpose usage.
1	PD	**Power-down mode bit** Cleared by hardware when reset occurs. Set to enter power-down mode.
0	IDL	**Idle mode bit** Clear by hardware when interrupt or reset occurs. Set to enter idle mode.

Reset Value = 00X1 0000b
Not bit addressable

Power-off flag reset value will be 1 only after a power on (cold reset). A warm reset doesn't affect the value of this bit.

are received simultaneously, an internal polling sequence determines which request is serviced. Thus within each priority level there is a second priority structure determined by the polling sequence.

Table 12. IE Register

IE - Interrupt Enable Register (A8h)

7	6	5	4	3	2	1	0
EA	**-**	**ET2**	**ES**	**ET1**	**EX1**	**ET0**	**EX0**

Bit Number	Bit Mnemonic	Description
7	EA	**Enable All interrupt bit** Clear to disable all interrupts. Set to enable all interrupts. If EA=1, each interrupt source is individually enabled or disabled by setting or clearing its own interrupt enable bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	ET2	**Timer 2 overflow interrupt Enable bit** Clear to disable timer 2 overflow interrupt. Set to enable timer 2 overflow interrupt.
4	ES	**Serial port Enable bit** Clear to disable serial port interrupt. Set to enable serial port interrupt.
3	ET1	**Timer 1 overflow interrupt Enable bit** Clear to disable timer 1 overflow interrupt. Set to enable timer 1 overflow interrupt.
2	EX1	**External interrupt 1 Enable bit** Clear to disable external interrupt 1. Set to enable external interrupt 1.
1	ET0	**Timer 0 overflow interrupt Enable bit** Clear to disable timer 0 overflow interrupt. Set to enable timer 0 overflow interrupt.
0	EX0	**External interrupt 0 Enable bit** Clear to disable external interrupt 0. Set to enable external interrupt 0.

Reset Value = 0X00 0000b

Bit addressable

Table 13. IP Register

IP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0
-	-	PT2	PS	PT1	PX1	PT0	PX0

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	PT2	**Timer 2 overflow interrupt Priority bit** Refer to PT2H for priority level.
4	PS	**Serial port Priority bit** Refer to PSH for priority level.
3	PT1	**Timer 1 overflow interrupt Priority bit** Refer to PT1H for priority level.
2	PX1	**External interrupt 1 Priority bit** Refer to PX1H for priority level.
1	PT0	**Timer 0 overflow interrupt Priority bit** Refer to PT0H for priority level.
0	PX0	**External interrupt 0 Priority bit** Refer to PX0H for priority level.

Reset Value = XX00 0000b

Bit addressable

Idle mode

An instruction that sets PCON.0 causes that to be the last instruction executed before going into the Idle mode. In the Idle mode, the internal clock signal is gated off to the CPU, but not to the interrupt, Timer, and Serial Port functions. The CPU status is preserved in its entirely : the Stack Pointer, Program Counter, Program Status Word, Accumulator and all other registers maintain their data during Idle. The port pins hold the logical states they had at the time Idle was activated. ALE and PSEN hold at logic high levels.

There are two ways to terminate the Idle. Activation of any enabled interrupt will cause PCON.0 to be cleared by hardware, terminating the Idle mode. The interrupt will be serviced, and following RETI the next instruction to be executed will be the one following the instruction that put the device into idle.

The flag bits GF0 and GF1 can be used to give an indication if an interrupt occured during normal operation or during an Idle. For example, an instruction that activates Idle can also set one or both flag bits. When Idle is terminated by an interrupt, the interrupt service routine can examine the flag bits.

The other way of terminating the Idle mode is with a hardware reset. Since the clock oscillator is still running, the hardware reset needs to be held active for only two machine cycles (24 oscillator periods) to complete the reset.

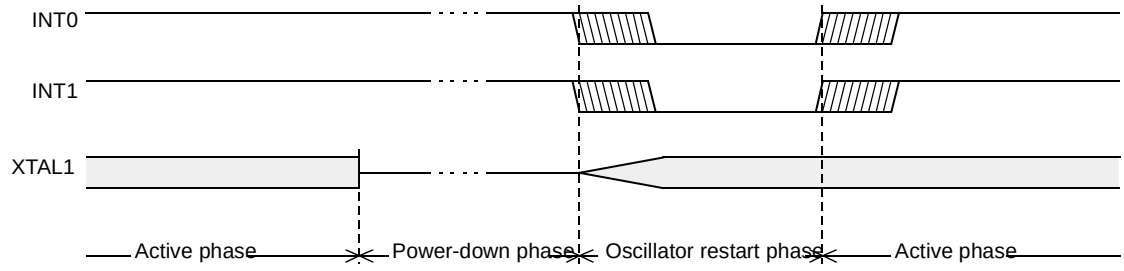
Power-down Mode

To save maximum power, a power-down mode can be invoked by software (Refer to Table 10., PCON register).

In power-down mode, the oscillator is stopped and the instruction that invoked power-down mode is the last instruction executed. The internal RAM and SFRs retain their value until the power-down mode is terminated. V_{CC} can be lowered to save further power. Either a hardware reset or an external interrupt can cause an exit from power-down. To properly terminate power-down, the reset or external interrupt should not be executed before V_{CC} is restored to its normal operating level and must be held active long enough for the oscillator to restart and stabilize.

Only external interrupts $\overline{INT0}$ and $\overline{INT1}$ are useful to exit from power-down. For that, interrupt must be enabled and configured as level or edge sensitive interrupt input.
Holding the pin low restarts the oscillator but bringing the pin high completes the exit as detailed in Figure 10. When both interrupts are enabled, the oscillator restarts as soon as one of the two inputs is held low and power down exit will be completed when the first input will be released. In this case the higher priority interrupt service routine is executed.
Once the interrupt is serviced, the next instruction to be executed after RETI will be the one following the instruction that put TS80C52X2 into power-down mode.

Figure 10. Power-down Exit Waveform



ONCE™ Mode (ON Chip Emulation)

The ONCE mode facilitates testing and debugging of systems using TS80C52X2 without removing the circuit from the board. The ONCE mode is invoked by driving certain pins of the TS80C52X2; the following sequence must be exercised:

- Pull ALE low while the device is in reset (RST high) and $\overline{\text{PSEN}}$ is high.
- Hold ALE low as RST is deactivated.

While the TS80C52X2 is in ONCE mode, an emulator or test CPU can be used to drive the circuit Table 26. shows the status of the port pins during ONCE mode.

Normal operation is restored when normal reset is applied.

Table 16. External Pin Status during ONCE Mode

ALE	PSEN	Port 0	Port 1	Port 2	Port 3	XTAL1/2
Weak pull-up	Weak pull-up	Float	Weak pull-up	Weak pull-up	Weak pull-up	Active

Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 18. AUXR Register

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	AO

Bit Number	Bit Mnemonic	Description
7	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
6	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
5	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
4	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
3	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
2	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
1	-	**Reserved** The value read from this bit is indeterminate. Do not set this bit.
0	AO	**ALE Output bit** Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.

Reset Value = XXXX XXX0b

Not bit addressable

EPROM Structure

The TS87C52X2 is divided in two different arrays:

- the code array: 8 Kbytes
- the encryption array: 64 bytes

In addition a third non programmable array is implemented:

- the signature array: 4 bytes

EPROM Lock System

The program Lock system, when programmed, protects the on-chip program against software piracy.

Encryption Array

Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

Program Lock Bits

The three lock bits, when programmed according to Table 1., will provide different level of protection for the on-chip code and data.

Program Lock Bits				
Security level	**LB1**	**LB2**	**LB3**	**Protection Description**
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	P	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the EPROM is disabled.
3	U	P	U	Same as 2, also verify is disabled.
4	U	U	P	Same as 3, also external execution is disabled.

U: unprogrammed
P: programmed

WARNING: Security level 2 and 3 should only be programmed after EPROM and Core verification.

Signature Bytes

The TS80/87C52X2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 9.

EPROM Programming

Set-up modes

In order to program and verify the EPROM or to read the signature bytes, the TS87C52X2 is placed in specific set-up modes (See Figure 11.).

Control and program signals must be held at the levels indicated in Table 35.

Definition of terms

Address Lines: P1.0-P1.7, P2.0-P2.4 respectively for A0-A12

Data Lines: P0.0-P0.7 for D0-D7

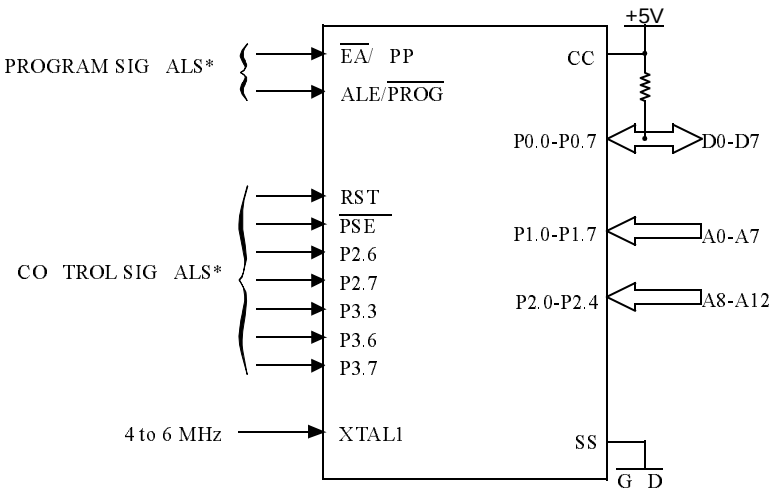
Control Signals: RST, $\overline{\text{PSEN}}$, P2.6, P2.7, P3.3, P3.6, P3.7.

Program Signals: ALE/$\overline{\text{PROG}}$, $\overline{\text{EA}}$/VPP.

Table 20. EPROM Set-up Modes

Mode	RST	PSEN	ALE/$\overline{\text{PROG}}$	$\overline{\text{EA}}$/VPP	P2.6	P2.7	P3.3	P3.6	P3.7
Program Code data	1	0	⊓	12.75V	0	1	1	1	1
Verify Code data	1	0	1	1	0	⊓	0	1	1
Program Encryption Array Address 0-3Fh	1	0	⊓	12.75V	0	1	1	0	1
Read Signature Bytes	1	0	1	1	0	⊓	0	0	0
Program Lock bit 1	1	0	⊓	12.75V	1	1	1	1	1
Program Lock bit 2	1	0	⊓	12.75V	1	1	1	0	0
Program Lock bit 3	1	0	⊓	12.75V	1	0	1	1	0

Figure 11. Set-Up Modes Configuration



* See Table 31. for proper value on these inputs

Programming Algorithm

The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.

To program the TS87C52X2 the following sequence must be exercised:

- Step 1: Activate the combination of control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Input the appropriate data on the data lines.
- Step 4: Raise $\overline{EA}$/VPP from VCC to VPP (typical 12.75V).
- Step 5: Pulse ALE/$\overline{PROG}$ once.
- Step 6: Lower $\overline{EA}$/VPP from VPP to VCC

Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 12.).

Verify Algorithm

Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C52X2.

P 2.7 is used to enable data output.

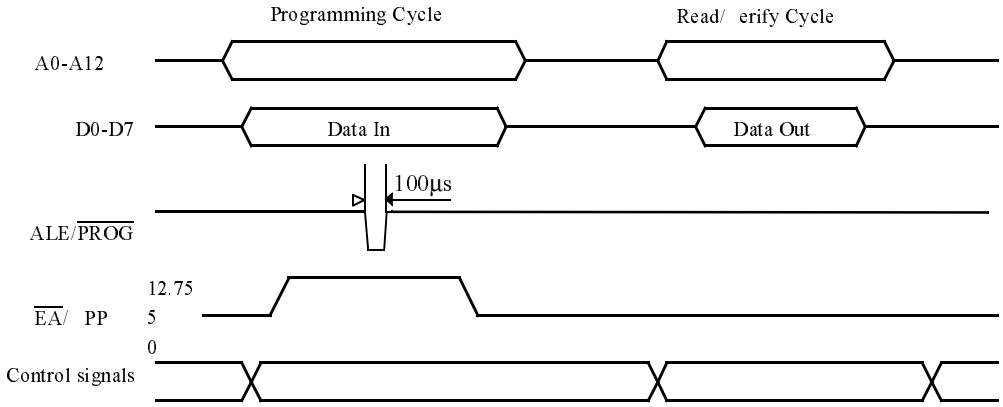
To verify the TS87C52X2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 12.)

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.

Figure 12. Programming and Verification Signal's Waveform



EPROM Erasure (Windowed Packages Only)

Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

Erasure Characteristics

The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm^2. Exposing the EPROM to an ultraviolet lamp of

Electrical Characteristics

Absolute Maximum Ratings[1]

Ambiant Temperature Under Bias:
C = commercial.....0°C to 70°C
I = industrial .....-40°C to 85°C
Storage Temperature ..... -65°C to + 150°C
Voltage on V_{CC} to V_{SS}.....-0.5V to + 7 V
Voltage on V_{PP} to V_{SS} .....-0.5V to + 13 V
Voltage on Any Pin to V_{SS}.....-0.5V to V_{CC} + 0.5V
Power Dissipation ..... 1 W[2]

Notes:
1. Stresses at or above those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.
2. This value is based on the maximum allowable die temperature and the thermal resistance of the package.

Power Consumption Measurement

Since the introduction of the first C51 devices, every manufacturer made operating Icc measurements under reset, which made sense for the designs were the CPU was running under reset. In Atmel new devices, the CPU is no more active during reset, so the power consumption is very low but is not really representative of what will happen in the customer system. That's why, while keeping measurements under Reset, Atmel presents a new way to measure the operating Icc:

Using an internal test ROM, the following code is executed:

Label: SJMP Label (80 FE)

Ports 1, 2, 3 are disconnected, Port 0 is tied to FFh, EA = Vcc, RST = Vss, XTAL2 is not connected and XTAL1 is driven by the clock.

This is much more representative of the real operating Icc.

DC Parameters for Standard Voltage

T_A = 0°C to +70°C; V_{SS} = 0 V; V_{CC} = 5V ± 10%; F = 0 to 40 MHz.
T_A = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 5V ± 10%; F = 0 to 40 MHz.

Table 22. DC Parameters in Standard Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage except XTAL1, RST	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, XTAL1, RST	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage, ports 1, 2, 3 [6]			0.3 0.45 1.0	V V V	I_{OL} = 100 µA[4] I_{OL} = 1.6 mA[4] I_{OL} = 3.5 mA[4]
V_{OL1}	Output Low Voltage, port 0 [6]			0.3 0.45 1.0	V V V	I_{OL} = 200 µA[4] I_{OL} = 3.2 mA[4] I_{OL} = 7.0 mA[4]
V_{OL2}	Output Low Voltage, ALE, $\overline{PSEN}$			0.3 0.45 1.0	V V V	I_{OL} = 100 µA[4] I_{OL} = 1.6 mA[4] I_{OL} = 3.5 mA[4]

DC Parameters for Low Voltage

T_A = 0°C to +70°C; V_{SS} = 0 V; V_{CC} = 2.7 V to 5.5V ; F = 0 to 30 MHz.
T_A = -40°C to +85°C; V_{SS} = 0 V; V_{CC} = 2.7 V to 5.5V ; F = 0 to 30 MHz.

Table 23. DC Parameters for Low Voltage

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5		0.2 V_{CC} - 0.1	V	
V_{IH}	Input High Voltage except XTAL1, RST	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage, XTAL1, RST	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage, ports 1, 2, 3 (6)			0.45	V	I_{OL} = 0.8 mA(4)
V_{OL1}	Output Low Voltage, port 0, ALE, $\overline{PSEN}$ (6)			0.45	V	I_{OL} = 1.6 mA(4)
V_{OH}	Output High Voltage, ports 1, 2, 3	0.9 V_{CC}			V	I_{OH} = -10 µA
V_{OH1}	Output High Voltage, port 0, ALE, $\overline{PSEN}$	0.9 V_{CC}			V	I_{OH} = -40 µA
I_{IL}	Logical 0 Input Current ports 1, 2 and 3			-50	µA	Vin = 0.45V
I_{LI}	Input Leakage Current			±10	µA	0.45V < Vin < V_{CC}
I_{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	µA	Vin = 2.0 V
R_{RST}	RST Pulldown Resistor	50	90 (5)	200	kΩ	
CIO	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz T_A = 25°C
I_{PD}	Power Down Current		20 (5) 10 (5)	50 30	µA	V_{CC} = 2.0 V to 5.5V(3) V_{CC} = 2.0 V to 3.3 V(3)
I_{CC} under RESET	Power Supply Current Maximum values, X1 mode: (7)			1 + 0.2 Freq (MHz) at12MHz 3.4 at16MHz 4.2	mA	V_{CC} = 3.3 V(1)
I_{CC} operating	Power Supply Current Maximum values, X1 mode: (7)			1 + 0.3 Freq (MHz) at12MHz 4.6 at16MHz 5.8	mA	V_{CC} = 3.3 V(8)
I_{CC} idle	Power Supply Current Maximum values, X1 mode: (7)			0.15 Freq (MHz) + 0.2 at12MHz 2 at16MHz 2.6	mA	V_{CC} = 3.3 V(2)

Notes:
1. I_{CC} under reset is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 17.), V_{IL} = V_{SS} + 0.5V,
   V_{IH} = V_{CC} - 0.5V; XTAL2 N.C.; $\overline{EA}$ = RST = Port 0 = V_{CC}. I_{CC} would be slightly higher if a crystal oscillator used..
2. Idle I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns, V_{IL} = V_{SS} + 0.5V, V_{IH} = V_{CC} - 0.5V; XTAL2 N.C; Port 0 = V_{CC}; $\overline{EA}$ = RST = V_{SS} (see Figure 15.).
3. Power Down I_{CC} is measured with all output pins disconnected; $\overline{EA}$ = V_{SS}, PORT 0 = V_{CC}; XTAL2 NC.; RST = V_{SS} (see Figure 16.).
4. Capacitance loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1 to 0 transitions during bus operation. In the worst cases (capacitive loading 100pF), the noise pulse on the ALE line may exceed 0.45V with maxi V_{OL} peak 0.6V. A Schmitt Trigger use is not necessary.
5. Typicals are based on a limited number of samples and are not guaranteed. The values listed are at room temperature and 5V.
6. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port:

Table 28., Table 31. and Table 34. give the frequency derating formula of the AC parameter. To calculate each AC symbols, take the x value corresponding to the speed grade you need (-M, -V or -L) and replace this value in the formula. Values of the frequency must be limited to the corresponding speed grade:

Table 25. Max frequency for derating formula regarding the speed grade

	-M X1 mode	-M X2 mode	-V X1 mode	-V X2 mode	-L X1 mode	-L X2 mode
Freq (MHz)	40	20	40	30	30	20
T (ns)	25	50	25	33.3	33.3	50

Example:

T_{LLIV} in X2 mode for a -V part at 20 MHz (T = $1/20^{E6}$ = 50 ns):

x= 22 (Table 28.)

T= 50ns

T_{LLIV}= 2T - x = 2 x 50 - 22 = 78ns

External Program Memory Characteristics

Table 26. Symbol Description

Symbol	Parameter
T	Oscillator clock period
T_{LHLL}	ALE pulse width
T_{AVLL}	Address Valid to ALE
T_{LLAX}	Address Hold After ALE
T_{LLIV}	ALE to Valid Instruction In
T_{LLPL}	ALE to $\overline{PSEN}$
T_{PLPH}	$\overline{PSEN}$ Pulse Width
T_{PLIV}	$\overline{PSEN}$ to Valid Instruction In
T_{PXIX}	Input Instruction Hold After $\overline{PSEN}$
T_{PXIZ}	Input Instruction FloatAfter $\overline{PSEN}$
T_{PXAV}	$\overline{PSEN}$ to Address Valid
T_{AVIV}	Address to Valid Instruction In
T_{PLAZ}	$\overline{PSEN}$ Low to Address Float

Table 27. AC Parameters for Fix Clock

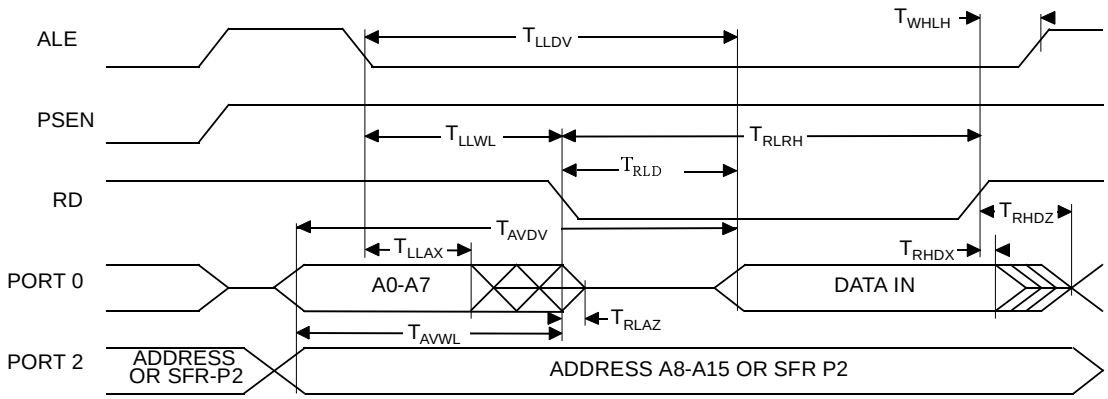
Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
T	25		33		25		50		33		ns
T_{LHLL}	40		25		42		35		52		ns
T_{AVLL}	10		4		12		5		13		ns
T_{LLAX}	10		4		12		5		13		ns
T_{LLIV}		70		45		78		65		98	ns
T_{LLPL}	15		9		17		10		18		ns
T_{PLPH}	55		35		60		50		75		ns
T_{PLIV}		35		25		50		30		55	ns
T_{PXIX}	0		0		0		0		0		ns
T_{PXIZ}		18		12		20		10		18	ns
T_{AVIV}		85		53		95		80		122	ns
T_{PLAZ}		10		10		10		10		10	ns

Table 28. AC Parameters for a Variable Clock: derating formula

Symbol	Type	Standard Clock	X2 Clock	-M	-V	-L	Units
T_{LHLL}	Min	2 T - x	T - x	10	8	15	ns
T_{AVLL}	Min	T - x	0.5 T - x	15	13	20	ns
T_{LLAX}	Min	T - x	0.5 T - x	15	13	20	ns
T_{LLIV}	Max	4 T - x	2 T - x	30	22	35	ns
T_{LLPL}	Min	T - x	0.5 T - x	10	8	15	ns
T_{PLPH}	Min	3 T - x	1.5 T - x	20	15	25	ns
T_{PLIV}	Max	3 T - x	1.5 T - x	40	25	45	ns
T_{PXIX}	Min	x	x	0	0	0	ns
T_{PXIZ}	Max	T - x	0.5 T - x	7	5	15	ns
T_{AVIV}	Max	5 T - x	2.5 T - x	40	30	45	ns
T_{PLAZ}	Max	x	x	10	10	10	ns

External Data Memory Read Cycle

Figure 20. External Data Memory Read Cycle



Serial Port Timing - Shift Register Mode

Table 32. Symbol Description

Symbol	Parameter
T_{XLXL}	Serial port clock cycle time
T_{QVHX}	Output data set-up to clock rising edge
T_{XHQX}	Output data hold after clock rising edge
T_{XHDX}	Input data hold after clock rising edge
T_{XHDV}	Clock rising edge to input data valid

Table 33. AC Parameters for a Fix Clock

Speed	-M 40 MHz		-V X2 mode 30 MHz 60 MHz equiv.		-V standard mode 40 MHz		-L X2 mode 20 MHz 40 MHz equiv.		-L standard mode 30 MHz		Units
Symbol	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
T_{XLXL}	300		200		300		300		400		ns
T_{QVHX}	200		117		200		200		283		ns
T_{XHQX}	30		13		30		30		47		ns
T_{XHDX}	0		0		0		0		0		ns
T_{XHDV}		117		34		117		117		200	ns

EPROM Programming and Verification Characteristics

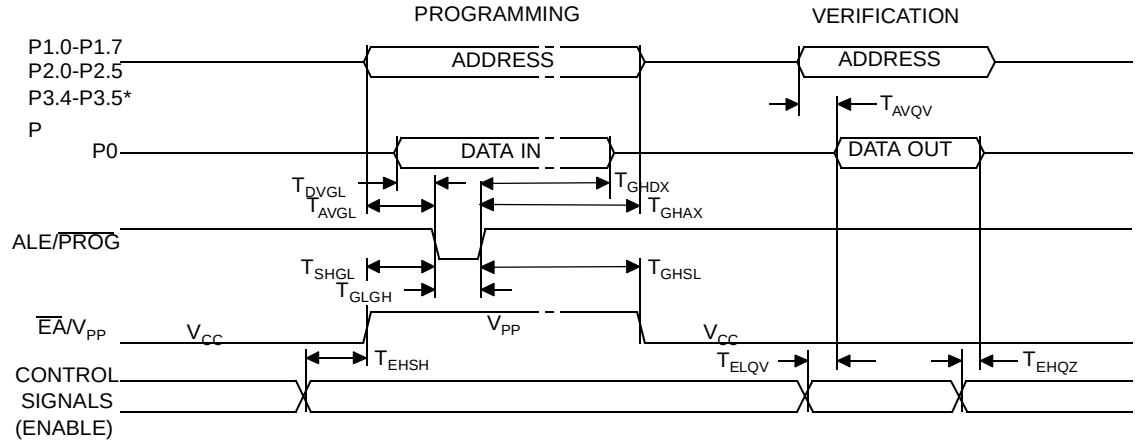
T_A = 21°C to 27°C; V_{SS} = 0V; V_{CC} = 5V ± 10% while programming. V_{CC} = operating range while verifying.

Table 35. EPROM Programming Parameters

Symbol	Parameter	Min	Max	Units
V_{PP}	Programming Supply Voltage	12.5	13	V
I_{PP}	Programming Supply Current		75	mA
$1/T_{CLCL}$	Oscillator Frquency	4	6	MHz
T_{AVGL}	Address Setup to $\overline{PROG}$ Low	48 T_{CLCL}		
T_{GHAX}	Adress Hold after $\overline{PROG}$	48 T_{CLCL}		
T_{DVGL}	Data Setup to $\overline{PROG}$ Low	48 T_{CLCL}		
T_{GHDX}	Data Hold after $\overline{PROG}$	48 T_{CLCL}		
T_{EHSH}	(Enable) High to V_{PP}	48 T_{CLCL}		
T_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
T_{GHSL}	V_{PP} Hold after $\overline{PROG}$	10		µs
T_{GLGH}	$\overline{PROG}$ Width	90	110	µs
T_{AVQV}	Address to Valid Data		48 T_{CLCL}	
T_{ELQV}	ENABLE Low to Data Valid		48 T_{CLCL}	
T_{EHQZ}	Data Float after ENABLE	0	48 T_{CLCL}	

EPROM Programming and Verification Waveforms

Figure 22. EPROM Programming and Verification Waveforms



* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

Table 37. Possible Ordering Entries (Continued)

Part Number[3]	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT80C32X2-RLTUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz[1]	VQFP44	Tray
AT80C32X2-3CSUV	ROMLess	5V ±10%	Industrial & Green	60 MHz[3]	PDIL40	Stick
AT80C32X2-SLSUV	ROMLess	5V ±10%	Industrial & Green	60 MHz[3]	PLCC44	Stick
AT80C32X2-RLTUV	ROMLess	5V ±10%	Industrial & Green	60 MHz[3]	VQFP44	Tray
TS80C52X2zzz-MCA	8K ROM	2.7 to 5.5V	Commercial	40 MHz[1]	PDIL40	Stick
TS80C52X2zzz-MCB	8K ROM	2.7 to 5.5V	Commercial	40 MHz[1]	PLCC44	Stick
TS80C52X2zzz-MCC	8K ROM	2.7 to 5.5V	Commercial	40 MHz[1]	PQFP44	Tray
TS80C52X2zzz-MCE	8K ROM	2.7 to 5.5V	Commercial	40 MHz[1]	VQFP44	Tray
TS80C52X2zzz-LCA	8K ROM	2.7 to 5.5V	Commercial	30 MHz[1]	PDIL40	Stick
TS80C52X2zzz-LCB	8K ROM	2.7 to 5.5V	Commercial	30 MHz[1]	PLCC44	Stick
TS80C52X2zzz-LCC	8K ROM	2.7 to 5.5V	Commercial	30 MHz[1]	PQFP44	Tray
TS80C52X2zzz-LCE	8K ROM	2.7 to 5.5V	Commercial	30 MHz[1]	VQFP44	Tray
TS80C52X2zzz-VCA	8K ROM	5V ±10%	Commercial	60 MHz[3]	PDIL40	Stick
TS80C52X2zzz-VCB	8K ROM	5V ±10%	Commercial	60 MHz[3]	PLCC44	Stick
TS80C52X2zzz-VCC	8K ROM	5V ±10%	Commercial	60 MHz[3]	PQFP44	Tray
TS80C52X2zzz-VCE	8K ROM	5V ±10%	Commercial	60 MHz[3]	VQFP44	Tray
TS80C52X2zzz-MIA	8K ROM	5V ±10%	Industrial	40 MHz[1]	PDIL40	Stick
TS80C52X2zzz-MIB	8K ROM	5V ±10%	Industrial	40 MHz[1]	PLCC44	Stick
TS80C52X2zzz-MIC	8K ROM	5V ±10%	Industrial	40 MHz[1]	PQFP44	Tray
TS80C52X2zzz-MIE	8K ROM	5V ±10%	Industrial	40 MHz[1]	VQFP44	Tray
TS80C52X2zzz-LIA	8K ROM	2.7 to 5.5V	Industrial	30 MHz[1]	PDIL40	Stick
TS80C52X2zzz-LIB	8K ROM	2.7 to 5.5V	Industrial	30 MHz[1]	PLCC44	Stick
TS80C52X2zzz-LIC	8K ROM	2.7 to 5.5V	Industrial	30 MHz[1]	PQFP44	Tray
TS80C52X2zzz-LIE	8K ROM	2.7 to 5.5V	Industrial	30 MHz[1]	VQFP44	Tray
TS80C52X2zzz-VIA	8K ROM	5V ±10%	Industrial	60 MHz[3]	PDIL40	Stick
TS80C52X2zzz-VIB	8K ROM	5V ±10%	Industrial	60 MHz[3]	PLCC44	Stick
TS80C52X2zzz-VIC	8K ROM	5V ±10%	Industrial	60 MHz[3]	PQFP44	Tray
TS80C52X2zzz-VIE	8K ROM	5V ±10%	Industrial	60 MHz[3]	VQFP44	Tray
AT80C52X2zzz-3CSUM	8K ROM	5V ±10%	Industrial & Green	40 MHz[1]	PDIL40	Stick
AT80C52X2zzz-SLSUM	8K ROM	5V ±10%	Industrial & Green	40 MHz[1]	PLCC44	Stick
AT80C52X2zzz-RLTUM	8K ROM	5V ±10%	Industrial & Green	40 MHz[1]	VQFP44	Tray

Table 37. Possible Ordering Entries (Continued)

Part Number[3]	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT80C52X2zzz-3CSUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz[1]	PDIL40	Stick
AT80C52X2zzz-SLSUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz[1]	PLCC44	Stick
AT80C52X2zzz-RLTUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz[1]	VQFP44	Tray
AT80C52X2zzz-3CSUV	8K ROM	5V ±10%	Industrial & Green	60 MHz[3]	PDIL40	Stick
AT80C52X2zzz-SLSUV	8K ROM	5V ±10%	Industrial & Green	60 MHz[3]	PLCC44	Stick
AT80C52X2zzz-RLTUV	8K ROM	5V ±10%	Industrial & Green	60 MHz[3]	VQFP44	Tray
TS87C52X2-MCA	8K OTP	5V ±10%	Commercial	40 MHz[1]	PDIL40	Stick
TS87C52X2-MCB	8K OTP	5V ±10%	Commercial	40 MHz[1]	PLCC44	Stick
TS87C52X2-MCC	8K OTP	5V ±10%	Commercial	40 MHz[1]	PQFP44	Tray
TS87C52X2-MCE	8K OTP	5V ±10%	Commercial	40 MHz[1]	VQFP44	Tray
TS87C52X2-LCA	8K OTP	2.7 to 5.5V	Commercial	30 MHz[1]	PDIL40	Stick
TS87C52X2-LCB	8K OTP	2.7 to 5.5V	Commercial	30 MHz[1]	PLC44	Stick
TS87C52X2-LCC	8K OTP	2.7 to 5.5V	Commercial	30 MHz[1]	PQFP44	Tray
TS87C52X2-LCE	8K OTP	2.7 to 5.5V	Commercial	30 MHz[1]	VQFP44	Tray
TS87C52X2-VCA	8K OTP	5V ±10%	Commercial	60 MHz[3]	PDIL40	Stick
TS87C52X2-VCB	8K OTP	5V ±10%	Commercial	60 MHz[3]	PLCC44	Stick
TS87C52X2-VCC	8K OTP	5V ±10%	Commercial	60 MHz[3]	PQFP44	Tray
TS87C52X2-VCE	8K OTP	5V ±10%	Commercial	60 MHz[3]	VQFP44	Tray
TS87C52X2-MIA	8K OTP	5V ±10%	Industrial	40 MHz[1]	PDIL40	Stick
TS87C52X2-MIB	8K OTP	5V ±10%	Industrial	40 MHz[1]	PLCC44	Stick
TS87C52X2-MIC	8K OTP	5V ±10%	Industrial	40 MHz[1]	PQFP44	Tray
TS87C52X2-MIE	8K OTP	5V ±10%	Industrial	40 MHz[1]	VQFP44	Tray
TS87C52X2-LIA	8K OTP	2.7 to 5.5V	Industrial	30 MHz[1]	PDIL40	Stick
TS87C52X2-LIB	8K OTP	2.7 to 5.5V	Industrial	30 MHz[1]	PLCC44	Stick
TS87C52X2-LIC	8K OTP	2.7 to 5.5V	Industrial	30 MHz[1]	PQFP44	Tray
TS87C52X2-LIE	8K OTP	2.7 to 5.5V	Industrial	30 MHz[1]	VQFP44	Tray
TS87C52X2-VIA	8K OTP	5V ±10%	Industrial	60 MHz[3]	PDIL40	Stick
TS87C52X2-VIB	8K OTP	5V ±10%	Industrial	60 MHz[3]	PLCC44	Stick
TS87C52X2-VIC	8K OTP	5V ±10%	Industrial	60 MHz[3]	PQFP44	Tray
TS87C52X2-VIE	8K OTP	5V ±10%	Industrial	60 MHz[3]	VQFP44	Tray

Table 37. Possible Ordering Entries (Continued)

Part Number[3]	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT87C52X2-3CSUM	8K OTP	5V ±10%	Industrial & Green	40 MHz[1]	PDIL40	Stick
AT87C52X2-SLSUM	8K OTP	5V ±10%	Industrial & Green	40 MHz[1]	PLCC44	Stick
AT87C52X2-RLTUM	8K OTP	5V ±10%	Industrial & Green	40 MHz[1]	VQFP44	Tray
AT87C52X2-3CSUL	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz[1]	PDIL40	Stick
AT87C52X2-SLSUL	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz[1]	PLCC44	Stick
AT87C52X2-RLTUL	8K OTP	2.7 to 5.5V	Industrial & Green	30 MHz[1]	VQFP44	Tray
AT87C52X2-3CSUV	8K OTP	5V ±10%	Industrial & Green	60 MHz[3]	PDIL40	Stick
AT87C52X2-SLSUV	8K OTP	5V ±10%	Industrial & Green	60 MHz[3]	PLCC44	Stick
AT87C52X2-RLTUV	8K OTP	5V ±10%	Industrial & Green	60 MHz[3]	VQFP44	Tray

Notes: 1. 20 MHz in X2 Mode.
2. Tape and Reel available for SL, PQFP and RL packages
3. 30 MHz in X2 Mode.