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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Obsolete
Core Processor	80C51
Core Size	8-Bit
Speed	60/30MHz
Connectivity	UART/USART
Peripherals	POR
Number of I/O	32
Program Memory Size	8KB (8K x 8)
Program Memory Type	ОТР
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIL
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/ts87c52x2-via

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Table 1. Memory Size

	ROM (bytes)	EPROM (bytes)	TOTAL RAM (bytes)
TS80C32X2	0	0	256
TS80C52X2	8k	0	256
TS87C52X2	0	8k	256

Block Diagram



2. Alternate function of Port 3

2



Table 2. All SFRs with their address and their reset value

	Bit Addressable	Non Bit Addressable							
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
F8h									FFh
F0h	B 0000 0000								F7h
E8h									EFh
E0h	ACC 0000 0000								E7h
D8 h									DFh
D0 h	PSW 0000 0000								D7h
C8 h	T2CON 0000 0000	T2MOD XXXX XX00	RCAP2L 0000 0000	RCAP2H 0000 0000	TL2 0000 0000	TH2 0000 0000			CFh
C0 h									C7h
B8h	IP XX00 0000	SADEN 0000 0000							BFh
B0h	P3 1111 1111							IPH XX00 0000	B7h
A8h	IE 0X00 0000	SADDR 0000 0000							AFh
A0h	P2 1111 1111		AUXR1 XXXX XXX0						A7h
98h	SCON 0000 0000	SBUF XXXX XXXX							9Fh
90h	P1 1111 1111								97h
88h	TCON 0000 0000	TMOD 0000 0000	TL0 0000 0000	TL1 0000 0000	TH0 0000 0000	TH1 0000 0000	AUXR XXXXXXX0	CKCON XXXX XXX0	8Fh
80h	P0 1111 1111	SP 0000 0111	DPL 0000 0000	DPH 0000 0000				PCON 00X1 0000	87h
	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	

Reserved



Dual Data Pointer Register (Ddptr)

The additional data pointer can be used to speed up code execution and reduce code size in a number of ways.

The dual DPTR structure is a way by which the chip will specify the address of an external data memory location. There are two 16-bit DPTR registers that address the external memory, and a single bit called

DPS = AUXR1/bit0 (See Table 5.) that allows the program code to switch between them (Refer to Figure 3).

Figure 3. Use of Dual Pointer



Table 4. AUXR1: Auxiliary Register 1

7	6	5	4	3	2	1	0		
-	-	-	-	GF3	0	-	DPS		
Bit Number	Bit Mnemonic	Descriptior	n						
7	-	Reserved The value re	eserved The value read from this bit is indeterminate. Do not set this bit.						
6	-	Reserved The value re	teserved The value read from this bit is indeterminate. Do not set this bit.						
5	-	Reserved The value re	Reserved The value read from this bit is indeterminate. Do not set this bit.						
4	-	Reserved The value re	Reserved The value read from this bit is indeterminate. Do not set this bit.						
3	GF3	This bit is a	general purpo	ose user flag					
2	0	Reserved Always stud	Reserved Always stuck at 0						
1	-	Reserved The value re	Reserved The value read from this bit is indeterminate. Do not set this bit.						
0	DPS	Data Pointe Clear to sele Set to selec	Data Pointer Selection Clear to select DPTR0. Set to select DPTR1.						

Reset Value = XXXX XXX0 Not bit addressable

Table 5	. T2CON	l Register
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T2CON - Timer 2 Control Register (C8h)

7	6	5	4	3	2	1	0	
TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C/T2#	CP/RL2#	
Bit Number	Bit Mnemonic	Description						
7	TF2	Timer 2 overf Must be cleare Set by hardwa	low Flag ed by software re on timer 2	e. overflow, if RC	CLK = 0 and T	CLK = 0.		
6	EXF2	Timer 2 Exter Set when a ca EXEN2=1. When set, cau interrupt is ena Must be cleare mode (DCEN	Timer 2 External Flag Set when a capture or a reload is caused by a negative transition on T2EX pin if EXEN2=1. When set, causes the CPU to vector to timer 2 interrupt routine when timer 2 interrupt is enabled. Must be cleared by software. EXF2 doesn't cause an interrupt in Up/down counter mode (DCEN = 1)					
5	RCLK	Receive Clock Clear to use time Set to use time	Receive Clock bit Clear to use timer 1 overflow as receive clock for serial port in mode 1 or 3. Set to use timer 2 overflow as receive clock for serial port in mode 1 or 3.					
4	TCLK	Transmit Cloc Clear to use tin Set to use time	Transmit Clock bit Clear to use timer 1 overflow as transmit clock for serial port in mode 1 or 3. Set to use timer 2 overflow as transmit clock for serial port in mode 1 or 3.					
3	EXEN2	Timer 2 Exter Clear to ignore Set to cause a detected, if tim	Timer 2 External Enable bit Clear to ignore events on T2EX pin for timer 2 operation. Set to cause a capture or reload when a negative transition on T2EX pin is detected, if timer 2 is not used to clock the serial port.					
2	TR2	Timer 2 Run of Clear to turn of Set to turn on	Timer 2 Run control bit Clear to turn off timer 2. Set to turn on timer 2.					
1	C/T2#	Timer/Counte Clear for timer Set for counter for clock out m	Timer/Counter 2 select bit Clear for timer operation (input from internal clock system: F _{OSC}). Set for counter operation (input from T2 input pin, falling edge trigger). Must be 0 for clock out mode.					
0	CP/RL2#	Timer 2 Capture/Reload bit If RCLK=1 or TCLK=1, CP/RL2# is ignored and timer is forced to Auto-reload on timer 2 overflow. Clear to Auto-reload on timer 2 overflows or negative transitions on T2EX pin if EXEN2=1. Set to capture on negative transitions on T2EX pin if EXEN2=1.						

Reset Value = 0000 0000b Bit addressable



TS80C52X2 Serial I/O
PortThe serial I/O port in the TS80C52X2 is compatible with the serial I/O port in the 80C52.
It provides both synchronous and asynchronous communication modes. It operates as
an Universal Asynchronous Receiver and Transmitter (UART) in three full-duplex
modes (Modes 1, 2 and 3). Asynchronous transmission and reception can occur simul-
taneously and at different baud rates
Serial I/O port includes the following enhancements:
 Framing error detectionAutomatic address recognitionFraming bit error detection is provided for the three asynchronous modes (modes 1, 2
and 3). To enable the framing bit error detection feature, set SMOD0 bit in PCON regis-
ter (See Figure 6).

Figure 6. Framing Error Block Diagram



When this feature is enabled, the receiver checks each incoming data frame for a valid stop bit. An invalid stop bit may result from noise on the serial lines or from simultaneous transmission by two CPUs. If a valid stop bit is not found, the Framing Error bit (FE) in SCON register (See Table 9.) bit is set.

Software may examine FE bit after each reception to check for data errors. Once set, only software or a reset can clear FE bit. Subsequently received frames with valid stop bits cannot clear FE bit. When FE feature is enabled, RI rises on stop bit instead of the last data bit (See Figure 7. and Figure 8.).

Figure 7. UART Timings in Mode 1





1111 0000b).
For slave A, bit 1 is a 1; for slaves B and C, bit 1 is a don't care bit. To communicate with slaves B and C, but not slave A, the master must send an address with bits 0 and 1 both set (e.g. 1111 0011b).
To communicate with slaves A, B and C, the master must send an address with bit 0 set, bit 1 clear, and bit 2 clear (e.g. 1111 0001b).

Broadcast Address A broadcast address is formed from the logical OR of the SADDR and SADEN registers with zeros defined as don't-care bits, e.g.:

SADDR 0101 0110b SADEN 1111 1100b Broadcast =SADDR OR SADEN1111 111Xb

The use of don't-care bits provides flexibility in defining the broadcast address, however in most applications, a broadcast address is FFh. The following is an example of using broadcast addresses:

Slave A:SADDR1111 0001b <u>SADEN1111 1010b</u> Broadcast1111 1X11b, Slave B:SADDR1111 0011b <u>SADEN1111 1001b</u> Broadcast1111 1X11B,

Slave C:SADDR=1111 0010b <u>SADEN1111 1101b</u> Broadcast1111 1111b

For slaves A and B, bit 2 is a don't care bit; for slave C, bit 2 is set. To communicate with all of the slaves, the master must send an address FFh. To communicate with slaves A and B, but not slave C, the master can send and address FBh.

Reset AddressesOn reset, the SADDR and SADEN registers are initialized to 00h, i.e. the given and
broadcast addresses are XXXX XXXb (all don't-care bits). This ensures that the serial
port will reply to any address, and so, that it is backwards compatible with the 80C51
microcontrollers that do not support automatic address recognition.

 Table 7.
 SADEN Register

SADEN - Slave Address	Mask Register	(B9h)
-----------------------	---------------	-------

7	6	5	4	3	2	1	0
teset Value lot bit addr able 8. S/	e = 0000 0 essable ADDR Reg lave Addre	000b jister ess Registe	er (A9h)				
7	6	5	4	3	2	1	0
Reset Value	e = 0000 0	000b	1	1	1		

Not bit addressable





Interrupt System

The TS80C52X2 has a total of 6 interrupt vectors: two external interrupts (INT0 and INT1), three timer interrupts (timers 0, 1 and 2) and the serial port interrupt. These interrupts are shown in Figure 9.

Figure 9. Interrupt Control System



Each of the interrupt sources can be individually enabled or disabled by setting or clearing a bit in the Interrupt Enable register (See Table 12.). This register also contains a global disable bit, which must be cleared to disable all interrupts at once.

Each interrupt source can also be individually programmed to one out of four priority levels by setting or clearing a bit in the Interrupt Priority register (See Table 13.) and in the Interrupt Priority High register (See Table 14.). shows the bit values and priority levels associated with each combination.

Table 11. Priority Level Bit Values	

IPH.x	IP.x	Interrupt Level Priority
0	0	0 (Lowest)
0	1	1
1	0	2
1	1	3 (Highest)

A low-priority interrupt can be interrupted by a high priority interrupt, but not by another low-priority interrupt. A high-priority interrupt can't be interrupted by any other interrupt source.

If two interrupt requests of different priority levels are received simultaneously, the request of higher priority level is serviced. If interrupt requests of the same priority level



Table 13. IP RegisterIP - Interrupt Priority Register (B8h)

7	6	5	4	3	2	1	0		
-	-	PT2	PS	PT1	PX1	PT0	PX0		
Bit Number	Bit Mnemonic	Descriptio	Description						
7	-	Reserved The value	Reserved The value read from this bit is indeterminate. Do not set this bit.						
6	-	Reserved The value	Reserved The value read from this bit is indeterminate. Do not set this bit.						
5	PT2	Timer 2 ov Refer to PT	Timer 2 overflow interrupt Priority bit Refer to PT2H for priority level.						
4	PS	Serial port	Serial port Priority bit Refer to PSH for priority level.						
3	PT1	Timer 1 ov Refer to PT	Timer 1 overflow interrupt Priority bit Refer to PT1H for priority level.						
2	PX1	External in Refer to P	External interrupt 1 Priority bit Refer to PX1H for priority level.						
1	PT0	Timer 0 ov Refer to PT	Timer 0 overflow interrupt Priority bit Refer to PT0H for priority level.						
0	PX0	External in Refer to P	nterrupt 0 Pri (0H for priorit	i ority bit y level.					

Reset Value = XX00 0000b Bit addressable



Reduced EMI Mode

The ALE signal is used to demultiplex address and data buses on port 0 when used with external program or data memory. Nevertheless, during internal code execution, ALE signal is still generated. In order to reduce EMI, ALE signal can be disabled by setting AO bit.

The AO bit is located in AUXR register at bit location 0. As soon as AO is set, ALE is no longer output but remains active during MOVX and MOVC instructions and external fetches. During ALE disabling, ALE pin is weakly pulled high.

Table 18. AUXR Register

AUXR - Auxiliary Register (8Eh)

7	6	5	4	3	2	1	0		
-	-	-	-	-	-	-	AO		
Bit Number	Bit Mnemonic	Description							
7	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.						
6	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.						
5	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.						
4	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.						
3	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.						
2	-	Reserved The value rea	Reserved The value read from this bit is indeterminate. Do not set this bit.						
1	-	Reserved The value rea	ad from this b	it is indetermi	nate. Do not s	et this bit.			
0	AO	ALE Output Clear to resto Set to disable	ALE Output bit Clear to restore ALE operation during internal fetches. Set to disable ALE operation during internal fetches.						

Reset Value = XXXX XXX0b Not bit addressable

TS80C52X2

ROM Structure The T

The TS80C52X2 ROM memory is divided in three different arrays:

- the code array:8 Kbytes.
- the encryption array:64 bytes.
- the signature array:4 bytes.

ROM Lock System The program Lock system, when programmed, protects the on-chip program against software piracy.

Encryption Array Within the ROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

Program Lock BitsThe lock bits when programmed according to Table 19. will provide different level of pro-
tection for the on-chip code and data.

Table 19.	Program Lock	bits	
Pr			

Pi	rogram L	ock Bits		
Security level	LB1	LB2	LB3	Protection Description
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	Ρ	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, EA is sampled and latched on reset.

U: unprogrammed P: programmed

Signature bytes

The TS80C52X2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 9.

Verify Algorithm

Refer to Section "Verify Algorithm".





EPROM Structure The TS87C52X2 is divided in two different arrays:

- the code array: 8 Kbytes
- the encryption array: 64 bytes

In addition a third non programmable array is implemented:

the signature array: 4 bytes

EPROM Lock System The program Lock system, when programmed, protects the on-chip program against software piracy.

Encryption Array Within the EPROM array are 64 bytes of encryption array that are initially unprogrammed (all FF's). Every time a byte is addressed during program verify, 6 address lines are used to select a byte of the encryption array. This byte is then exclusive-NOR'ed (XNOR) with the code byte, creating an encrypted verify byte. The algorithm, with the encryption array in the unprogrammed state, will return the code in its original, unmodified form.

When using the encryption array, one important factor needs to be considered. If a byte has the value FFh, verifying the byte will produce the encryption byte value. If a large block (>64 bytes) of code is left unprogrammed, a verification routine will display the content of the encryption array. For this reason all the unused code bytes should be programmed with random values. This will ensure program protection.

Program Lock Bits The three lock bits, when programmed according to Table 1., will provide different level of protection for the on-chip code and data.

Pr	ogram Lo	ock Bits		
Security level	LB1	LB2	LB3	Protection Description
1	U	U	U	No program lock features enabled. Code verify will still be encrypted by the encryption array if programmed. MOVC instruction executed from external program memory returns non encrypted data.
2	Ρ	U	U	MOVC instruction executed from external program memory are disabled from fetching code bytes from internal memory, \overline{EA} is sampled and latched on reset, and further programming of the EPROM is disabled.
3	U	Р	U	Same as 2, also verify is disabled.
4	U	U	Р	Same as 3, also external execution is disabled.

U: unprogrammed P: programmed

WARNING: Security level 2 and 3 should only be programmed after EPROM and Core verification.

Signature Bytes The TS80/87C52X2 contains 4 factory programmed signatures bytes. To read these bytes, perform the process described in section 9.

EPROM Programming

Set-up modes

In order to program and verify the EPROM or to read the signature bytes, the TS87C52X2 is placed in specific set-up modes (See Figure 11.).

Programming Algorithm	The Improved Quick Pulse algorithm is based on the Quick Pulse algorithm and decreases the number of pulses applied during byte programming from 25 to 1.
	To program the TS87C52X2 the following sequence must be exercised:
	• Step 1: Activate the combination of control signals.
	Step 2: Input the valid address on the address lines.
	• Step 3: Input the appropriate data on the data lines.
	• Step 4: Raise EA/VPP from VCC to VPP (typical 12.75V).
	Step 5: Pulse ALE/PROG once.
	Step 6: Lower EA/VPP from VPP to VCC
	Repeat step 2 through 6 changing the address and data for the entire array or until the end of the object file is reached (See Figure 12.).

Verify Algorithm Code array verify must be done after each byte or block of bytes is programmed. In either case, a complete verify of the programmed array will ensure reliable programming of the TS87C52X2.

P 2.7 is used to enable data output.

To verify the TS87C52X2 code the following sequence must be exercised:

- Step 1: Activate the combination of program and control signals.
- Step 2: Input the valid address on the address lines.
- Step 3: Read data on the data lines.

Repeat step 2 through 3 changing the address for the entire array verification (See Figure 12.)

The encryption array cannot be directly verified. Verification of the encryption array is done by observing that the code array is well encrypted.

Figure 12. Programming and Verification Signal's Waveform



EPROM Erasure (Windowed Packages Only) Erasing the EPROM erases the code array, the encryption array and the lock bits returning the parts to full functionality.

Erasure leaves all the EPROM cells in a 1's state (FF).

Erasure Characteristics The recommended erasure procedure is exposure to ultraviolet light (at 2537 Å) to an integrated dose at least 15 W-sec/cm². Exposing the EPROM to an ultraviolet lamp of

TS8xCx2X2

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Symbol	Parameter	Min	Тур	Max	Unit	Test Conditions
V _{OH}	Output High Voltage, ports 1, 2, 3	V _{CC} - 0.3 V _{CC} - 0.7 V _{CC} - 1.5			V V V	$I_{OH} = -10 \ \mu A$ $I_{OH} = -30 \ \mu A$ $I_{OH} = -60 \ \mu A$ $V_{CC} = 5V \pm 10\%$
V _{OH1}	Output High Voltage, port 0	V _{CC} - 0.3 V _{CC} - 0.7 V _{CC} - 1.5			> > >	$I_{OH} = -200 \ \mu A$ $I_{OH} = -3.2 \ m A$ $I_{OH} = -7.0 \ m A$ $V_{CC} = 5V \pm 10\%$
V _{OH2}	Output High Voltage,ALE, PSEN	V _{CC} - 0.3 V _{CC} - 0.7 V _{CC} - 1.5			V V V	$I_{OH} = -100 \ \mu A$ $I_{OH} = -1.6 \ m A$ $I_{OH} = -3.5 \ m A$ $V_{CC} = 5V \pm 10\%$
R _{RST}	RST Pulldown Resistor	50	90 ⁽⁵⁾	200	kΩ	
I _{IL}	Logical 0 Input Current ports 1, 2 and 3			-50	μΑ	Vin = 0.45V
I _{LI}	Input Leakage Current			±10	μΑ	0.45V < Vin < V _{CC}
I _{TL}	Logical 1 to 0 Transition Current, ports 1, 2, 3			-650	μA	Vin = 2.0 V
C _{IO}	Capacitance of I/O Buffer			10	pF	Fc = 1 MHz TA = 25°C
I _{PD}	Power Down Current		20 (5)	50	μA	$2.0 \text{ V} < \text{V}_{\text{CC}} < 5.5 \text{V}^{(3)}$
I _{CC} under RESET	Power Supply Current Maximum values, X1 mode: (7)			1 + 0.4 Freq (MHz) at12MHz 5.8 at16MHz 7.4	mA	$V_{\rm CC} = 5.5 V^{(1)}$
I _{CC} operating	Power Supply Current Maximum values, X1 mode: (7)			3 + 0.6 Freq (MHz) at12MHz 10.2 at16MHz 12.6	mA	$V_{\rm CC} = 5.5 V^{(8)}$
I _{CC} idle	Power Supply Current Maximum values, X1 mode: (7)			0.25+0.3 Freq (MHz) at12MHz 3.9 at16MHz 5.1	mA	$V_{\rm CC} = 5.5 V^{(2)}$



TS8xCx2X2

Port 0: 26 mA Ports 1, 2 and 3: 15 mA Maximum total I_{OL} for all output pins: 71 mA If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

- 7. For other values, please contact your sales office.
- Operating I_{CC} is measured with all output pins disconnected; XTAL1 driven with T_{CLCH}, T_{CHCL} = 5 ns (see Figure 17.), V_{IL} = V_{SS} + 0.5V,

 $V_{IH} = V_{CC} - 0.5V$; XTAL2 N.C.; $\overline{EA} = Port 0 = V_{CC}$; RST = V_{SS} . The internal ROM runs the code 80 FE (label: SJMP label). I_{CC} would be slightly higher if a crystal oscillator is used. Measurements are made with OTP products when possible, which is the worst case.

Figure 13. I_{CC} Test Condition, under reset



All other pins are disconnected.





All other pins are disconnected.

Figure 15. I_{CC} Test Condition, Idle Mode



All other pins are disconnected.



External Program Memory Read Cycle

Figure 18. External Program Memory Read Cycle



External Data Memory Characteristics

 Table 29.
 Symbol Description

Symbol	Parameter
T _{RLRH}	RD Pulse Width
T _{WLWH}	WR Pulse Width
T _{RLDV}	RD to Valid Data In
T _{RHDX}	Data Hold After RD
T _{RHDZ}	Data Float After RD
T _{LLDV}	ALE to Valid Data In
T _{AVDV}	Address to Valid Data In
T _{LLWL}	ALE to WR or RD
T _{AVWL}	Address to WR or RD
T _{QVWX}	Data Valid to WR Transition
T _{QVWH}	Data set-up to WR High
T _{WHQX}	Data Hold After WR
T _{RLAZ}	RD Low to Address Float
T _{WHLH}	RD or WR High to ALE high



Symbol	Туре	Standard Clock	X2 Clock	-М	-V	-L	Units
T _{RLRH}	Min	6 T - x	3 T - x	20	15	25	ns
T _{WLWH}	Min	6 T - x	3 T - x	20	15	25	ns
T _{RLDV}	Max	5 T - x	2.5 T - x	25	23	30	ns
T _{RHDX}	Min	х	х	0	0	0	ns
T _{RHDZ}	Max	2 T - x	T - x	20	15	25	ns
T _{LLDV}	Max	8 T - x	4T -x	40	35	45	ns
T _{AVDV}	Max	9 T - x	4.5 T - x	60	50	65	ns
T _{LLWL}	Min	3 T - x	1.5 T - x	25	20	30	ns
T _{LLWL}	Max	3 T + x	1.5 T + x	25	20	30	ns
T _{AVWL}	Min	4 T - x	2 T - x	25	20	30	ns
T _{QVWX}	Min	T - x	0.5 T - x	15	10	20	ns
T _{QVWH}	Min	7 T - x	3.5 T - x	15	10	20	ns
T _{WHQX}	Min	T - x	0.5 T - x	10	8	15	ns
T _{RLAZ}	Max	х	х	0	0	0	ns
T _{WHLH}	Min	T - x	0.5 T - x	15	10	20	ns
T _{WHLH}	Max	T + x	0.5 T + x	15	10	20	ns

Table 31. AC Parameters for a Variable Clock: Derating Formula

External Data Memory Write Cycle







EPROM Programming and Verification Characteristics

 T_A = 21°C to 27°C; V_{SS} = 0V; $~V_{CC}$ = 5V \pm 10% while programming. V_{CC} = operating range while verifying.

 Table 35.
 EPROM Programming Parameters

Symbol	Parameter	Min	Мах	Units
V _{PP}	Programming Supply Voltage	12.5	13	V
I _{PP}	Programming Supply Current		75	mA
1/T _{CLCL}	Oscillator Frquency	4	6	MHz
T _{AVGL}	Address Setup to PROG Low	48 T _{CLCL}		
T _{GHAX}	Adress Hold after PROG	48 T _{CLCL}		
T _{DVGL}	Data Setup to PROG Low	48 T _{CLCL}		
T _{GHDX}	Data Hold after PROG	48 T _{CLCL}		
T _{EHSH}	(Enable) High to V _{PP}	48 T _{CLCL}		
T _{SHGL}	V _{PP} Setup to PROG Low	10		μs
T _{GHSL}	V _{PP} Hold after PROG	10		μs
T _{GLGH}	PROG Width	90	110	μs
T _{AVQV}	Address to Valid Data		48 T _{CLCL}	
T _{ELQV}	ENABLE Low to Data Valid		48 T _{CLCL}	
T _{EHQZ}	Data Float after ENABLE	0	48 T _{CLCL}	

EPROM Programming and Verification Waveforms

Figure 22. EPROM Programming and Verification Waveforms



* 8KB: up to P2.4, 16KB: up to P2.5, 32KB: up to P3.4, 64KB: up to P3.5

External Clock Drive Characteristics (XTAL1)

Table 36. AC Parameters

Symbol	Parameter	Min	Мах	Units
T _{CLCL}	Oscillator Period	25		ns
Т _{снсх}	High Time	5		ns
T _{CLCX}	Low Time	5		ns
T _{CLCH}	Rise Time		5	ns
T _{CHCL}	Fall Time		5	ns
T _{CHCX} /T _{CLCX}	Cyclic ratio in X2 mode	40	60	%

External Clock Drive Waveforms

Figure 23. External Clock Drive Waveforms



AC Testing Input/Output Waveforms

Figure 24. AC Testing Input/Output Waveforms

INPUT/OUTPUT



AC inputs during testing are driven at V_{CC} - 0.5 for a logic "1" and 0.45V for a logic "0". Timing measurement are made at V_{IH} min for a logic "1" and V_{IL} max for a logic "0".

Float Waveforms

Figure 25. Float Waveforms



For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \ge \pm 20$ mA.



Ordering Information

Table 37. Possible Ordering Entries

Part Number ⁽³⁾	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
TS80C32X2-MCA	ROMLess	5V <u>±</u> 10%	Commercial	40 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-MCB	ROMLess	5V <u>±</u> 10%	Commercial	40 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-MCC	ROMLess	5V <u>±</u> 10%	Commercial	40 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-MCE	ROMLess	5V <u>±</u> 10%	Commercial	40 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-LCA	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-LCB	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-LCC	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-LCE	ROMLess	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-VCA	ROMLess	5V <u>±</u> 10%	Commercial	60 MHz ⁽³⁾	PDIL40	Stick
TS80C32X2-VCB	ROMLess	5V <u>±</u> 10%	Commercial	60 MHz ⁽³⁾	PLCC44	Stick
TS80C32X2-VCC	ROMLess	5V <u>±</u> 10%	Commercial	60 MHz ⁽³⁾	PQFP44	Tray
TS80C32X2-VCE	ROMLess	5V <u>±</u> 10%	Commercial	60 MHz ⁽³⁾	VQFP44	Tray
TS80C32X2-MIA	ROMLess	5V <u>±</u> 10%	Industrial	40 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-MIB	ROMLess	5V <u>±</u> 10%	Industrial	40 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-MIC	ROMLess	5V <u>±</u> 10%	Industrial	40 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-MIE	ROMLess	5V <u>±</u> 10%	Industrial	40 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-LIA	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PDIL40	Stick
TS80C32X2-LIB	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PLCC44	Stick
TS80C32X2-LIC	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PQFP44	Tray
TS80C32X2-LIE	ROMLess	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	VQFP44	Tray
TS80C32X2-VIA	ROMLess	5V <u>±</u> 10%	Industrial	60 MHz ⁽³⁾	PDIL40	Stick
TS80C32X2-VIB	ROMLess	5V <u>±</u> 10%	Industrial	60 MHz ⁽³⁾	PLCC44	Stick
TS80C32X2-VIC	ROMLess	5V <u>±</u> 10%	Industrial	60 MHz ⁽³⁾	PQFP44	Tray
TS80C32X2-VIE	ROMLess	5V <u>±</u> 10%	Industrial	60 MHz ⁽³⁾	VQFP44	Tray
AT80C32X2-3CSUM	ROMLess	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	PDIL40	Stick
AT80C32X2-SLSUM	ROMLess	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	PLCC44	Stick
AT80C32X2-RLTUM	ROMLess	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	VQFP44	Tray
AT80C32X2-RLTUM	ROMLess	5V ±10%	Industrial & Green	40 MHz ⁽¹⁾	VQFP44	Tape & Reel
AT80C32X2-3CSUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PDIL40	Stick
AT80C32X2-SLSUL	ROMLess	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PLCC44	Stick



Table 37. Possible Ordering Entries (Continued)

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Part Number ⁽³⁾	Memory Size	Supply Voltage	Temperature Range	Max Frequency	Package	Packing
AT80C52X2zzz-3CSUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PDIL40	Stick
AT80C52X2zzz-SLSUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	PLCC44	Stick
AT80C52X2zzz-RLTUL	8K ROM	2.7 to 5.5V	Industrial & Green	30 MHz ⁽¹⁾	VQFP44	Tray
AT80C52X2zzz-3CSUV	8K ROM	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	PDIL40	Stick
AT80C52X2zzz-SLSUV	8K ROM	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	PLCC44	Stick
AT80C52X2zzz-RLTUV	8K ROM	5V ±10%	Industrial & Green	60 MHz ⁽³⁾	VQFP44	Tray
TS87C52X2-MCA	8K OTP	5V ±10%	Commercial	40 MHz ⁽¹⁾	PDIL40	Stick
TS87C52X2-MCB	8K OTP	5V ±10%	Commercial	40 MHz ⁽¹⁾	PLCC44	Stick
TS87C52X2-MCC	8K OTP	5V ±10%	Commercial	40 MHz ⁽¹⁾	PQFP44	Tray
TS87C52X2-MCE	8K OTP	5V ±10%	Commercial	40 MHz ⁽¹⁾	VQFP44	Tray
TS87C52X2-LCA	8K OTP	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PDIL40	Stick
TS87C52X2-LCB	8K OTP	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PLC44	Stick
TS87C52X2-LCC	8K OTP	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	PQFP44	Tray
TS87C52X2-LCE	8K OTP	2.7 to 5.5V	Commercial	30 MHz ⁽¹⁾	VQFP44	Tray
TS87C52X2-VCA	8K OTP	5V ±10%	Commercial	60 MHz ⁽³⁾	PDIL40	Stick
TS87C52X2-VCB	8K OTP	5V ±10%	Commercial	60 MHz ⁽³⁾	PLCC44	Stick
TS87C52X2-VCC	8K OTP	5V ±10%	Commercial	60 MHz ⁽³⁾	PQFP44	Tray
TS87C52X2-VCE	8K OTP	5V ±10%	Commercial	60 MHz ⁽³⁾	VQFP44	Tray
TS87C52X2-MIA	8K OTP	5V ±10%	Industrial	40 MHz ⁽¹⁾	PDIL40	Stick
TS87C52X2-MIB	8K OTP	5V ±10%	Industrial	40 MHz ⁽¹⁾	PLCC44	Stick
TS87C52X2-MIC	8K OTP	5V ±10%	Industrial	40 MHz ⁽¹⁾	PQFP44	Tray
TS87C52X2-MIE	8K OTP	5V ±10%	Industrial	40 MHz ⁽¹⁾	VQFP44	Tray
TS87C52X2-LIA	8K OTP	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PDIL40	Stick
TS87C52X2-LIB	8K OTP	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PLCC44	Stick
TS87C52X2-LIC	8K OTP	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	PQFP44	Tray
TS87C52X2-LIE	8K OTP	2.7 to 5.5V	Industrial	30 MHz ⁽¹⁾	VQFP44	Tray
TS87C52X2-VIA	8K OTP	5V ±10%	Industrial	60 MHz ⁽³⁾	PDIL40	Stick
TS87C52X2-VIB	8K OTP	5V ±10%	Industrial	60 MHz ⁽³⁾	PLCC44	Stick
TS87C52X2-VIC	8K OTP	5V ±10%	Industrial	60 MHz ⁽³⁾	PQFP44	Tray
TS87C52X2-VIE	8K OTP	5V ±10%	Industrial	60 MHz ⁽³⁾	VQFP44	Tray

